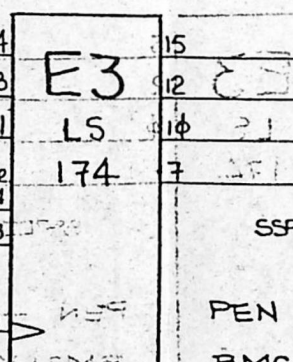
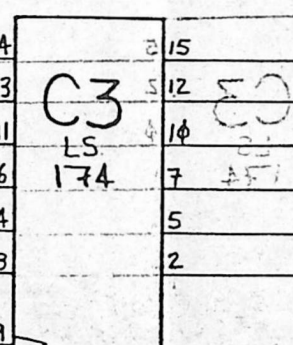
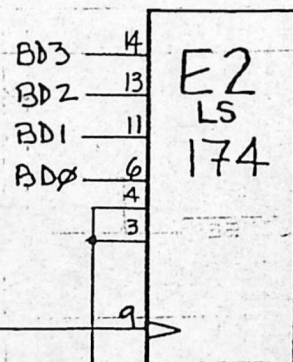
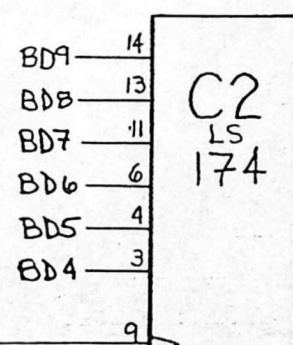
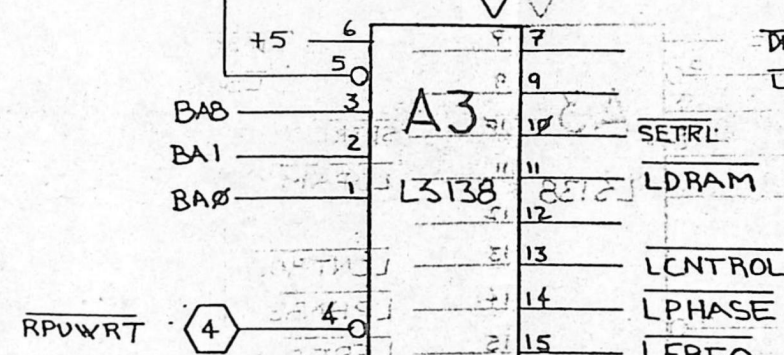
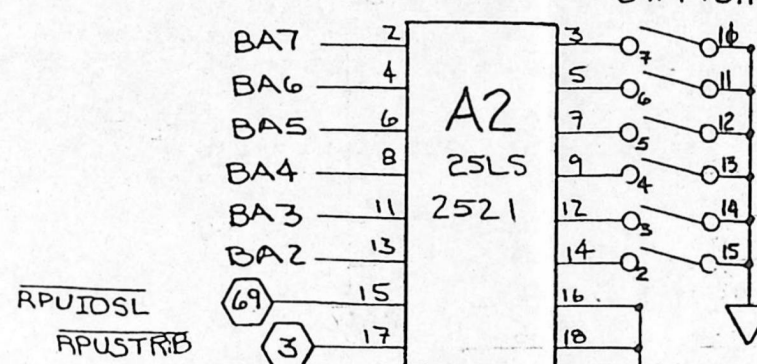
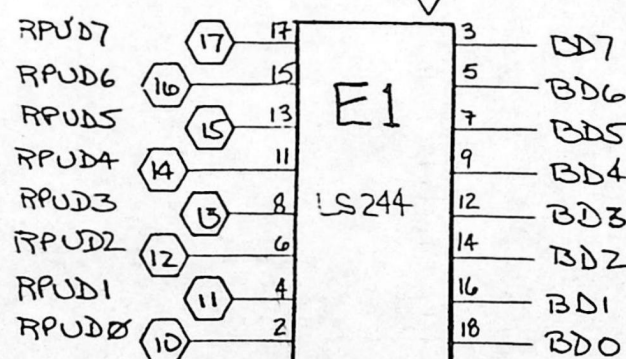
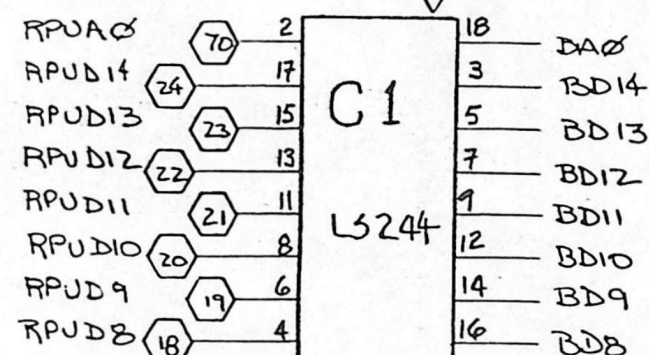
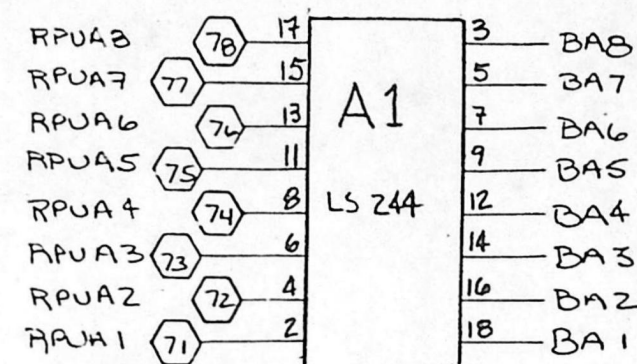


SCHEMATIC DRAWINGS

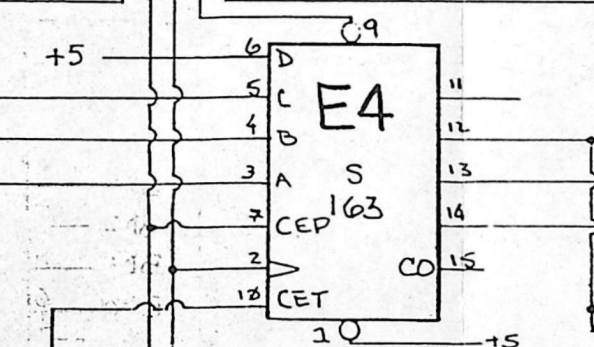
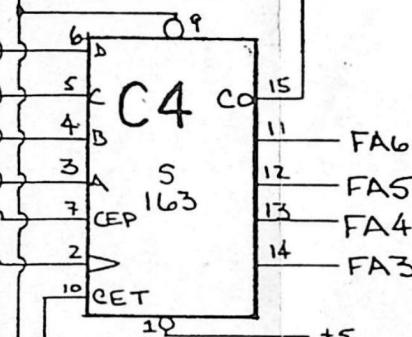
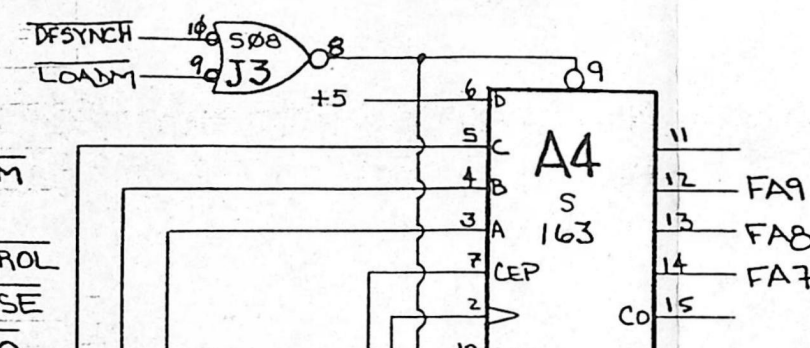
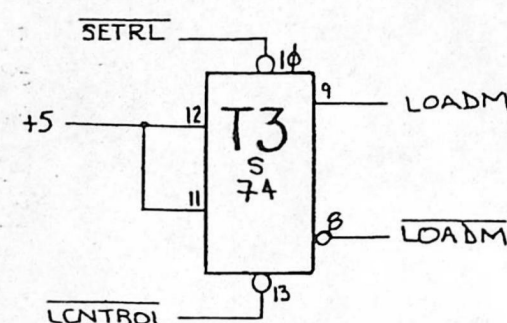
CIC-W-66	FUNCTION GENERATOR
CIC-W-67	FUNCTION GENERATOR COMBINER
CIC-W-69	ECLIPSE/RPU COMMUNICATION
CIC-W-70	AUXILARY CABLE INTERCONNECT
CIC-W-71	STANDARD BUS/CIC-6 INTERFACE
CIC-W-72	STANDARD BUS HALF NEST BACKPLANE
CIC-W-73	KEYBOARD
CIC-W-74	CRT CONTROLLER AND FIGGYBACK BOARD
CIC-W-75	ENTERPRISE 6809 MPU
CIC-W-76	REMOTE CONTROL PANEL INTERFACE
CVS-111B-1	GREY LEVEL SWITCHES
CVS-112C	VIDEO AMPS
CVS-114C-2	GREY LEVEL MULTIPLEXER
CVS-125A-1	LEVEL DETECTORS
CVS-127A	MONITOR PINCUSHION CORRECTOR
CVS-128	MONITOR YOKE COMPENSATION
CVS-134-3	INPUT AMP
CVS-134-4	INPUT AMP
CVS-135B-1	BACKGROUND KEY
CVS-136-1	COLOR COMPARATOR
CVS-138-2	CONSTANT CURRENT AMP
SM-111A	1/ 36 VOLT REGULATOR
SM-117E-1	OVERLAP YOKE DEFLECTION AMP
SM-121C	OVERLAP CAMERA HIGH VOLTAGE
SM-122D	MONITOR YOKE DEFLECTION AMP
SM-139B	MONITOR FOCUS COIL CURRENT REGULATOR
SM-143A	CRT SOCKET BOARD
SM-151	OVERLAP WRITE VIDEO AMP/SOCKET BOARD
SM-152	OVERLAP CAMERA CONTROL
WCIC-100	X-Y SCOPE SWITCHING
WCIC-101	X-Y SCOPE SWITCHING CONTROL PANEL
WCIC-102	SYSTEM 4 AC POWER SWITCHING
WCIC-103	MONITOR VIDEO PROCESSOR CONTROL PANEL WIRING
WCIC-104	SWITCHER/COLOR CONTROLLER CONTROL PANEL WIRING
WCIC-105-2	MAIN POWER SUPPLY WIRING
WCIC-106-2	SCANCONVERTER POWER SUPPLY WIRING
WCIC-107	SCANCONVERTER DRAWER #1 (MONITOR) WIRING
WCIC-108	SCANCONVERTER DRAWER #2 (CAMERA) WIRING
WCIC-109	DATA CASSETTE POWER SUPPLY WIRING
WCIC-110	LIGHT BOX CONTROL WIRING
KELTRON P720	20KV HIGH VOLTAGE SUPPLY
KELTRON P601	1KV HIGH VOLTAGE SUPPLY
TELEMATION BVH-1200	COMPUTER TERMINAL CRT
TELEMATION TCE 2000	MODIFICATION

SEMI-CONDUCTOR DATA SHEETS

wcic-119



L1
DIP
SWITCH



ATA Corp.

COMPUTER IMAGE

FUNCTION GENERATOR

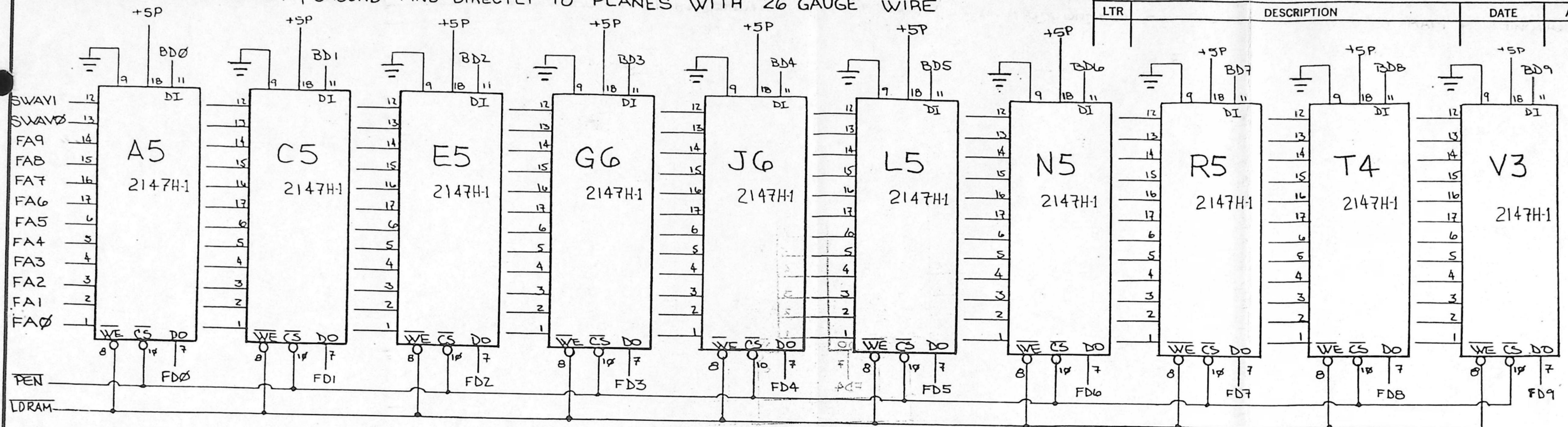
Buffers & Address Generator

APPROVALS	DATE
DRAWN SP/LD	4-21-82
CHECKED REV D	
SCALE	SIZE B
DRAWING NO.	CIC-W-66

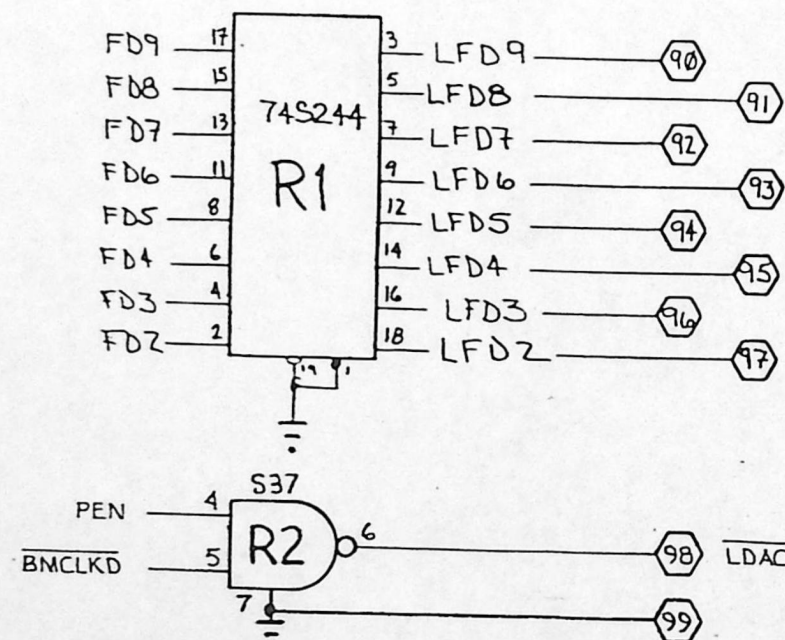
TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES
± ± ±

REV: A;B;C;D;E;
DO NOT SCALE DRAWING

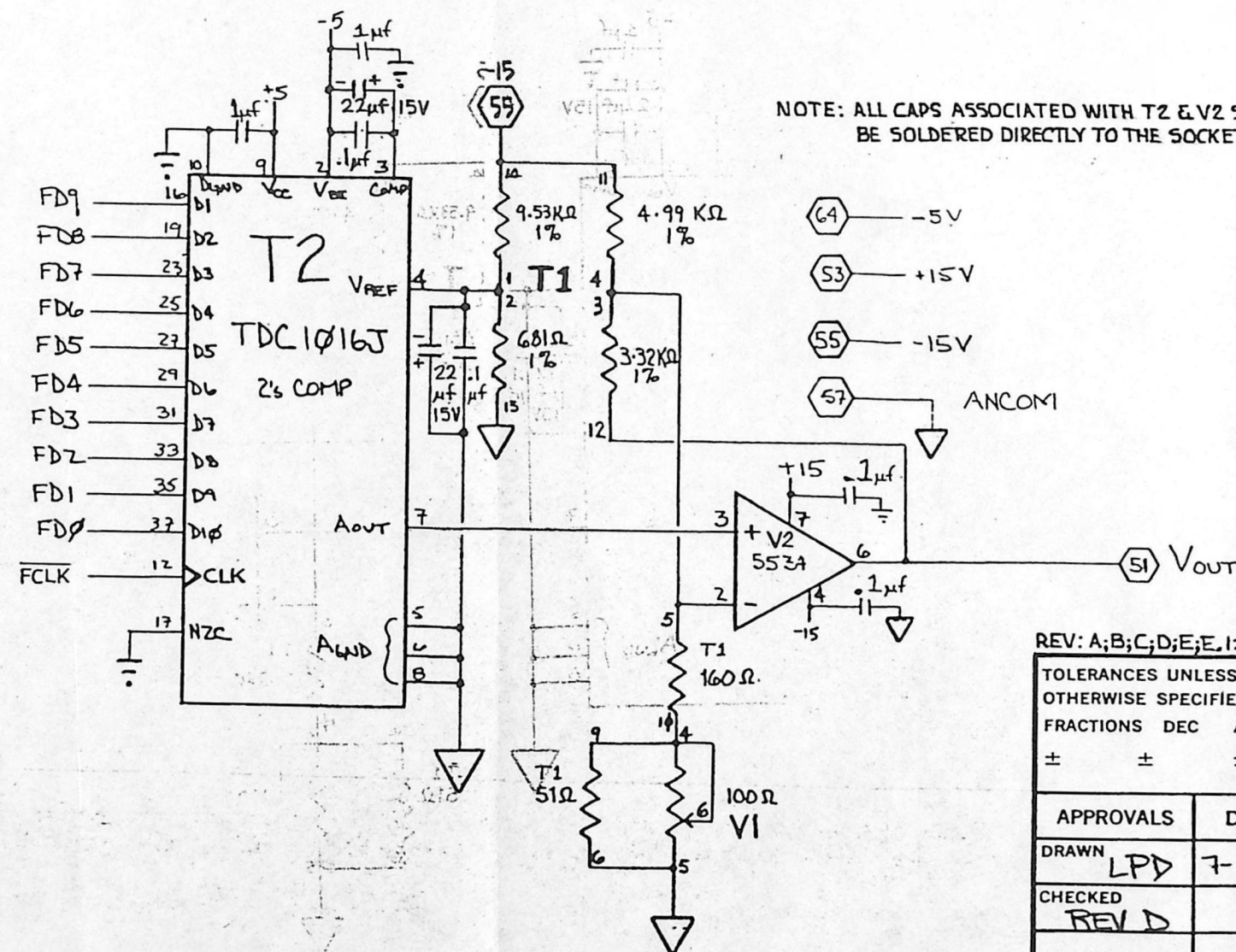
NOTE: CONNECT RAM POWER & GROUND PINS DIRECTLY TO PLANES WITH 26 GAUGE WIRE



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



NOTE: ▽ DENOTES ISOLATED ANALOG GND BETWEEN ROWS U & V.
 UNUSED: AND J3-11
 NAND G5-11, J4-3, R2-8, R2-11
 INV J1-8, G1-8



NOTE: ALL CAPS ASSOCIATED WITH T2 & V2 SHALL BE SOLDERED DIRECTLY TO THE SOCKET PINS.

T1	
1	9.53 K Ω - 1%
2	681 Ω - 1%
3	3.32 K Ω - 1%
4	4.99 K Ω - 1%
5	160 Ω - 5%
6	51 Ω - 5%
7	(N.C.)

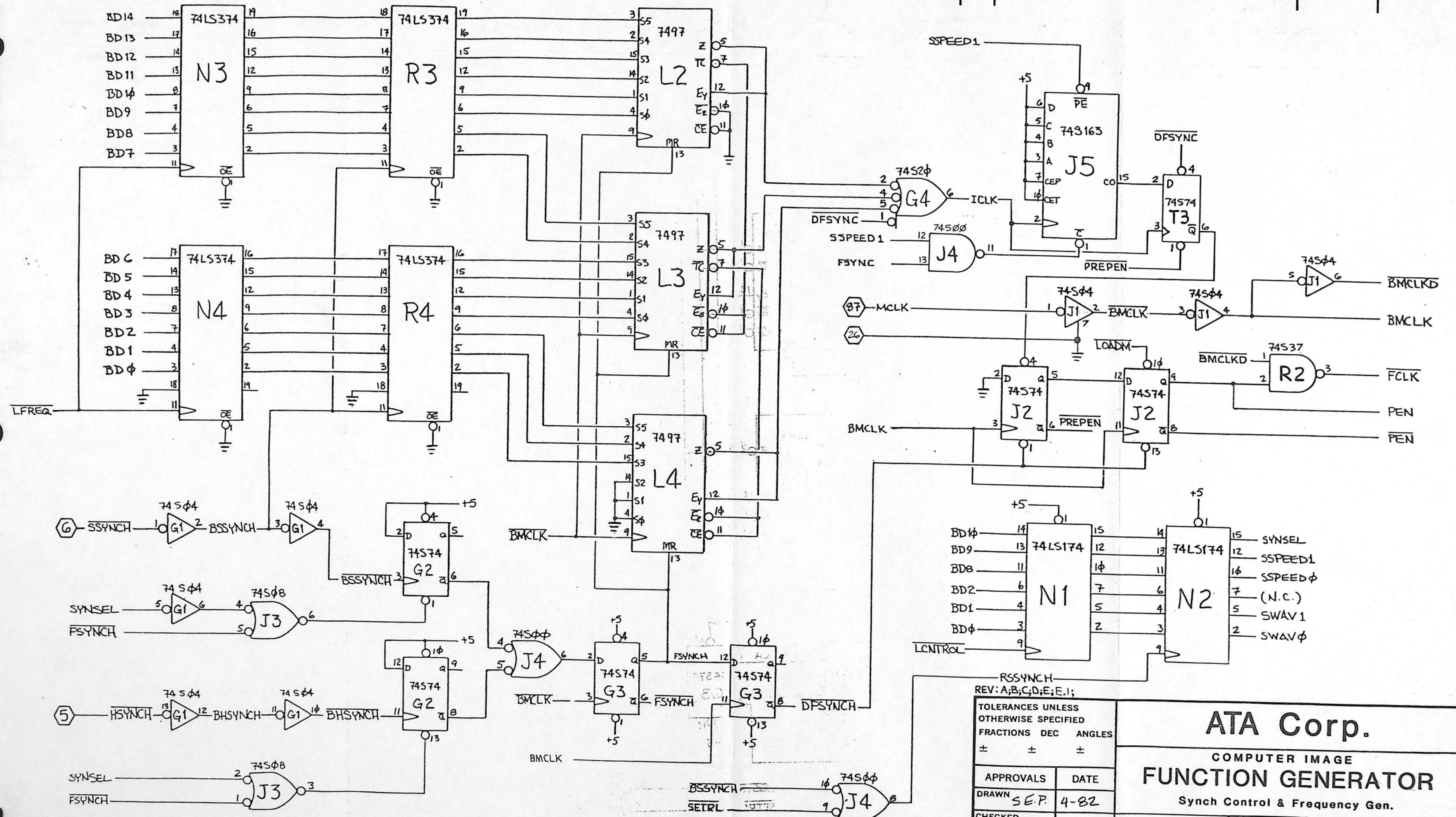
REV: A;B;C;D;E;I;

TOLERANCES UNLESS OTHERWISE SPECIFIED
 FRACTIONS DEC ANGLES
 ± ± ±

APPROVALS	DATE
DRAWN LPD	7-7-81
CHECKED REV D	

ATA Corp.			
COMPUTER IMAGE			
FUNCTION GENERATOR			
D/A Output & WFM Storage			
SCALE	SIZE B	DRAWING NO. CIC-W-66	
DO NOT SCALE DRAWING		SHEET 2 OF 3	

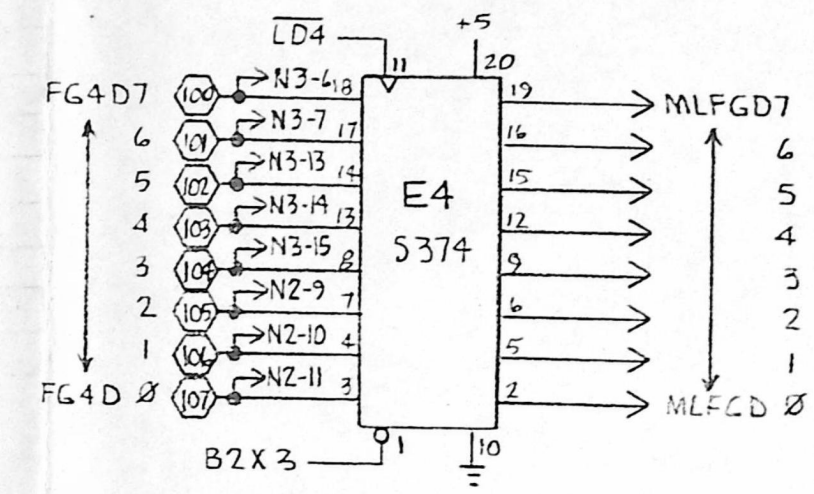
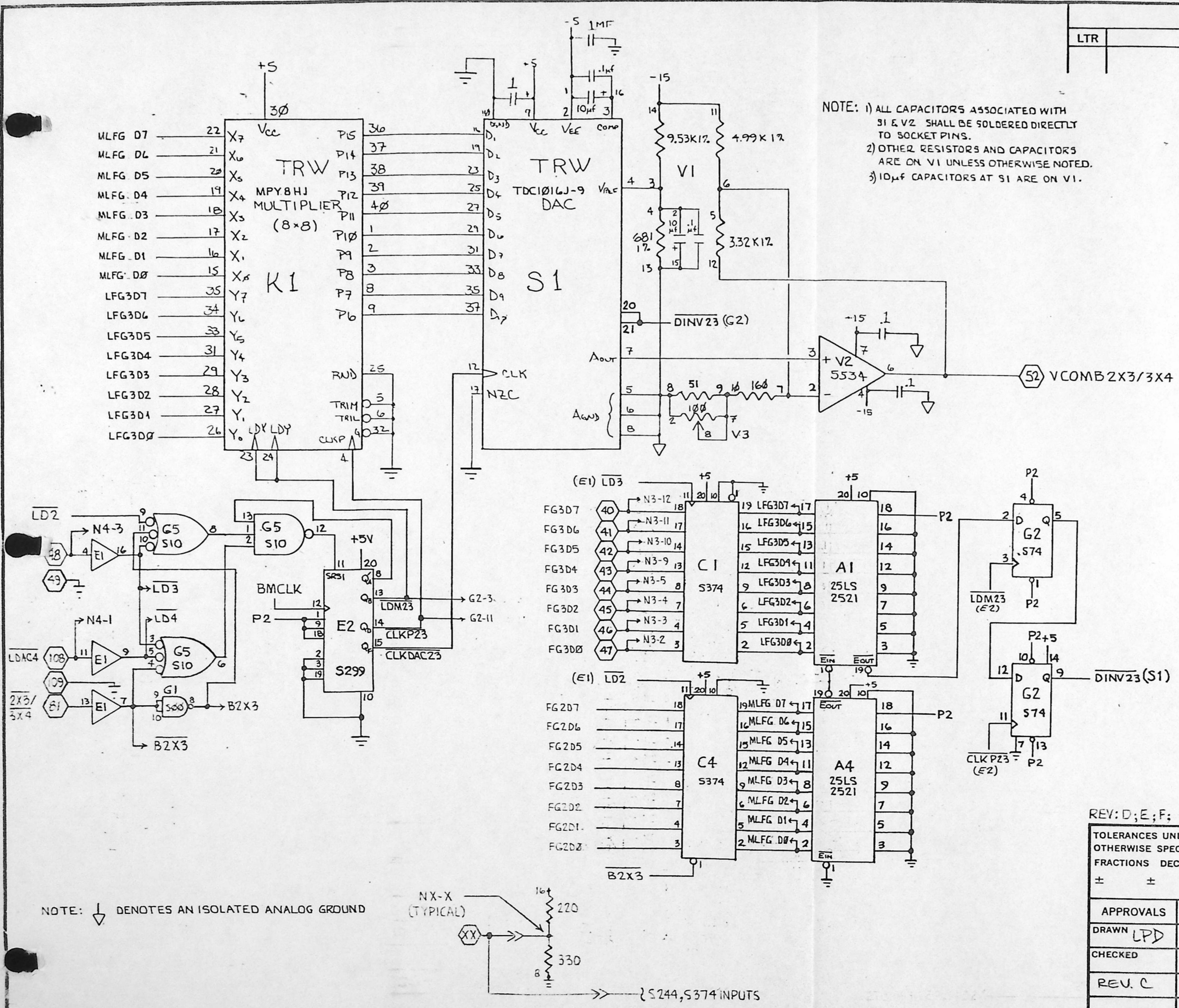
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



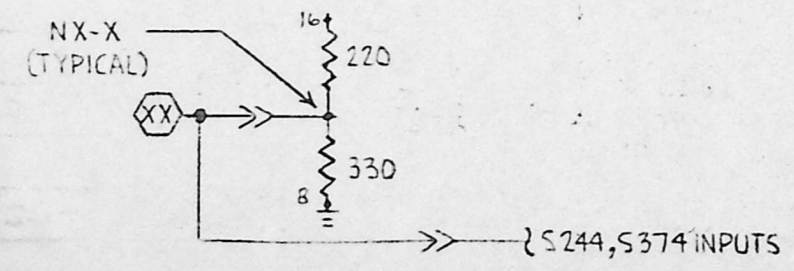
NOTE: L2, L3, L4 MUST BE SELECTED FOR RELIABLE OPERATION

ATA Corp.			
COMPUTER IMAGE			
FUNCTION GENERATOR			
Synch Control & Frequency Gen.			
APPROVALS	DATE	SCALE	SIZE
DRAWN S.E.P.	4-82		B
CHECKED REV D			
DO NOT SCALE DRAWING		DRAWING NO. CIC-W-66	
		SHEET 3 OF 3	

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



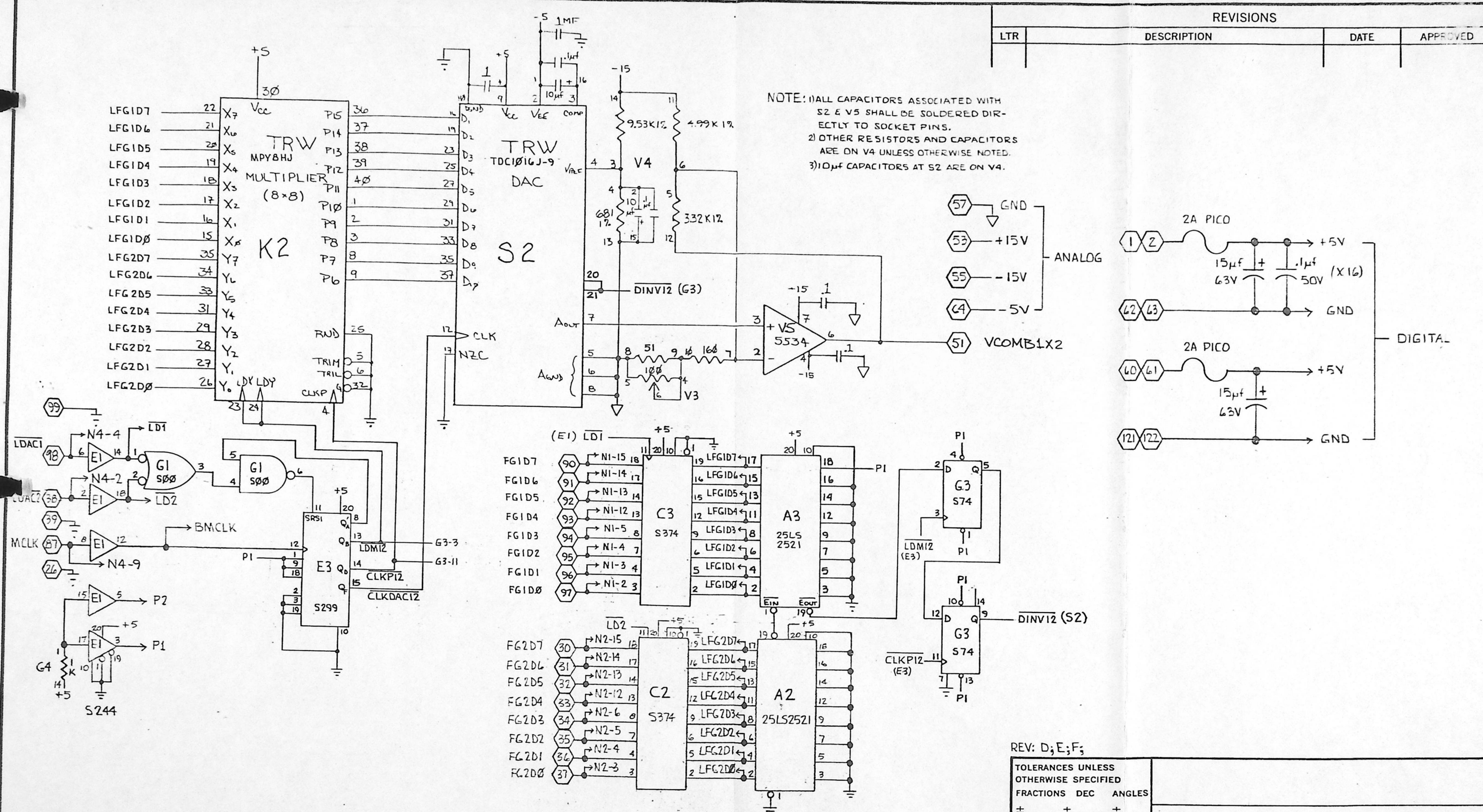
NOTE: ∇ DENOTES AN ISOLATED ANALOG GROUND



REV: D; E; F;

TOLERANCES UNLESS OTHERWISE SPECIFIED		FRACTIONS DEC ANGLES	
±	±	±	±
APPROVALS		DATE	
DRAWN LPD		7-26-81	
CHECKED		SCALE	
REV. C		4-81	
COMPUTER IMAGE		F.G. COMBINER BOARD	
FG2 x FG3 / 3X4		SIZE	
DO NOT SCALE DRAWING		DRAWING NO.	
		B	
		CIC-W-67	
		SHEET 1 OF 2	

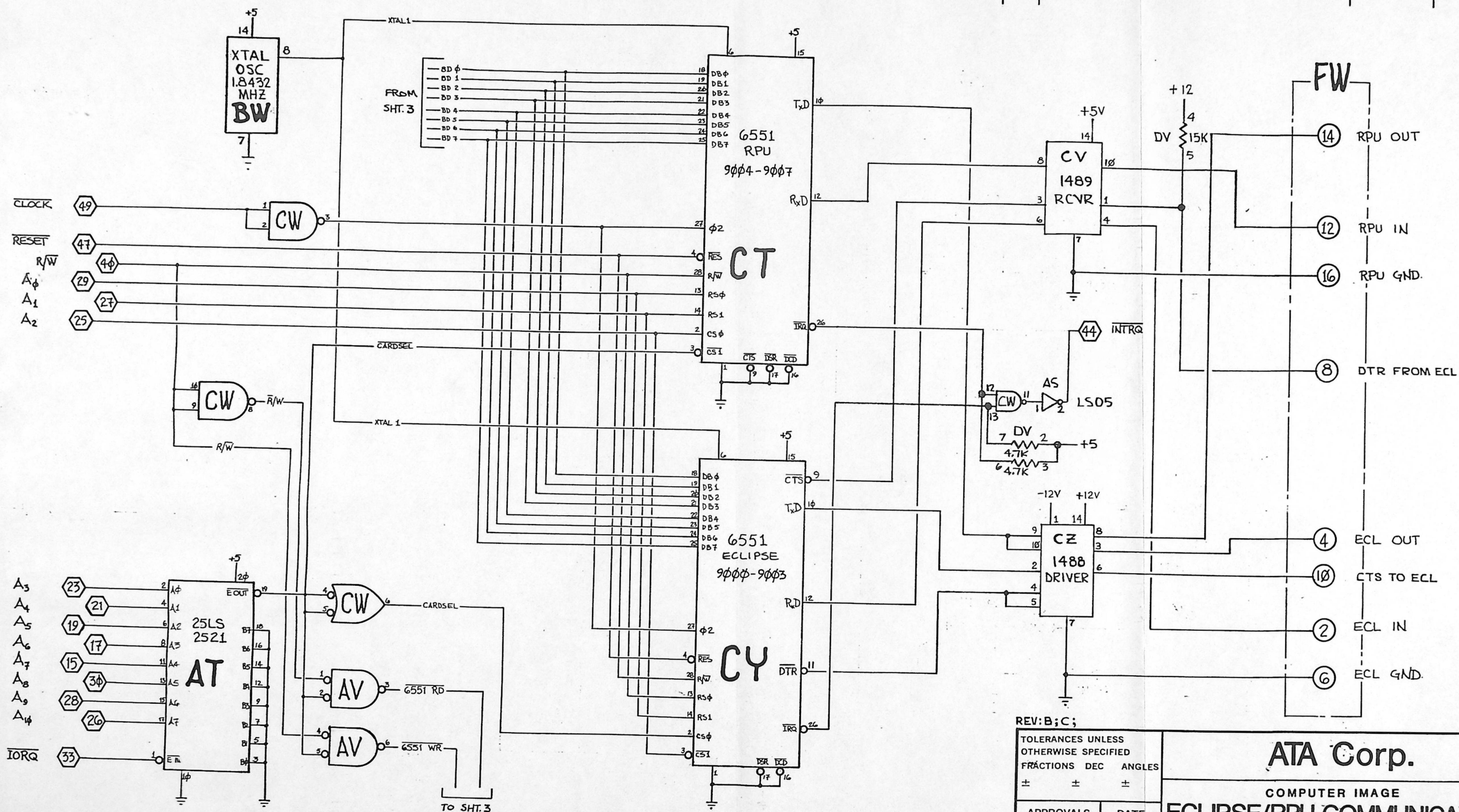
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



REV: D; E; F;

TOLERANCES UNLESS OTHERWISE SPECIFIED			COMPUTER IMAGE	
FRACTIONS	DEC	ANGLES	F.G. COMBINER BOARD	
±	±	±	FG1 x FG2 / 3x4	
APPROVALS	DATE	SCALE	SIZE	DRAWING NO.
DRAWN LPD	7-26-81		B	CIC-W-67
CHECKED				
REV. C	4-82			
DO NOT SCALE DRAWING			SHEET 2 OF 2	

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



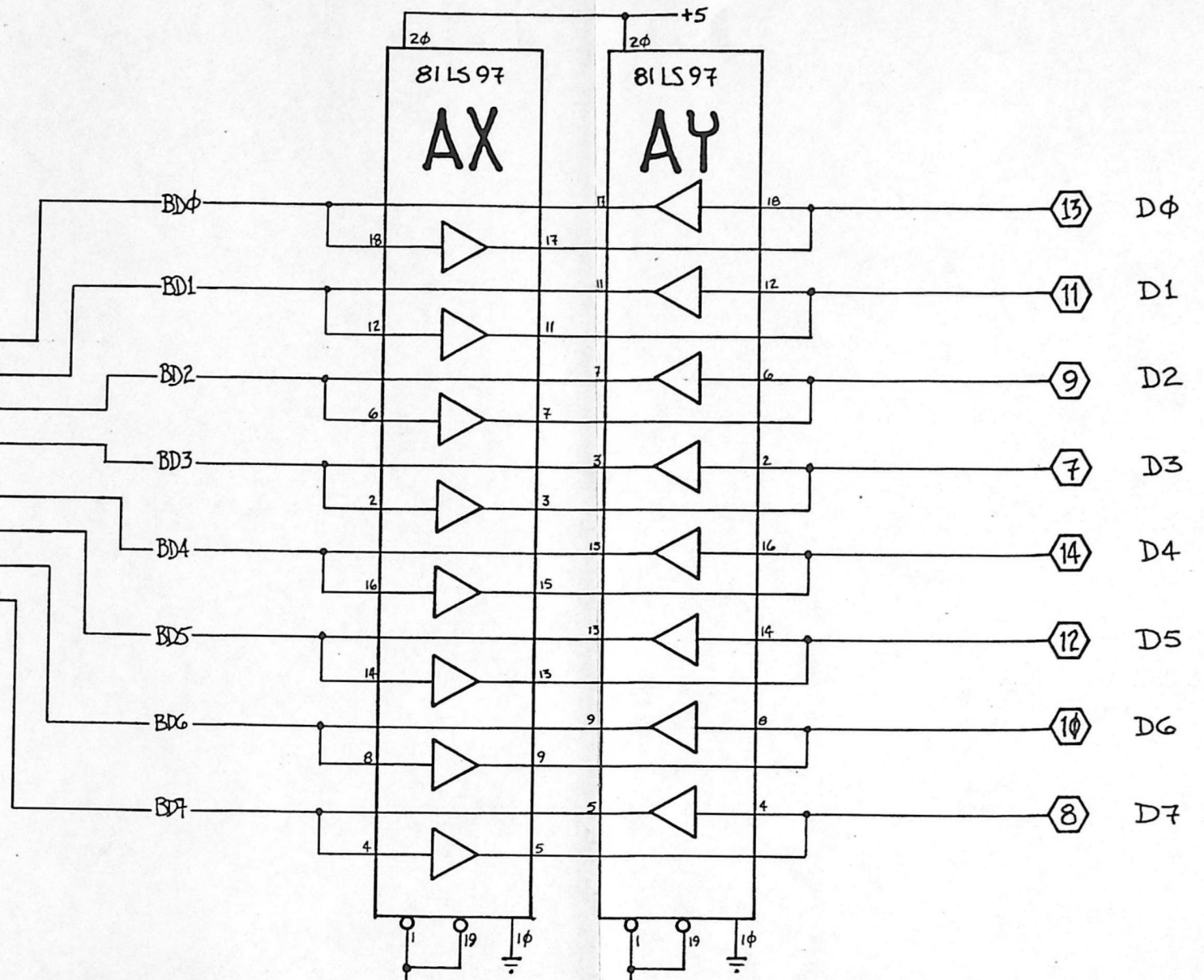
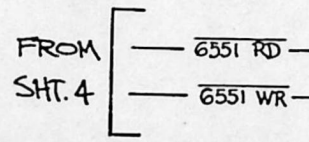
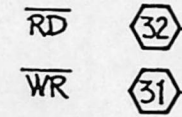
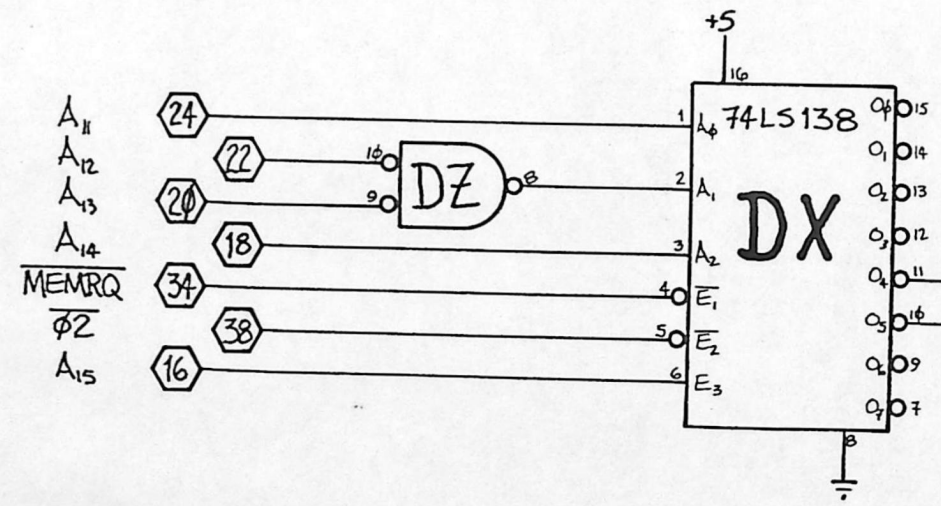
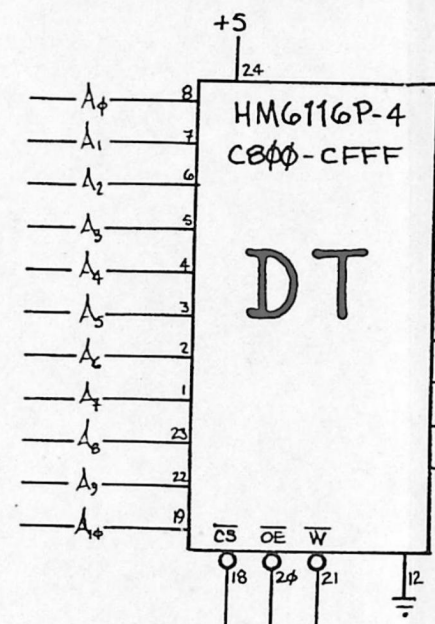
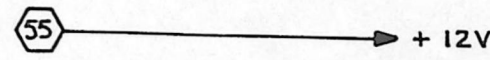
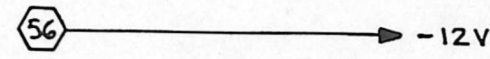
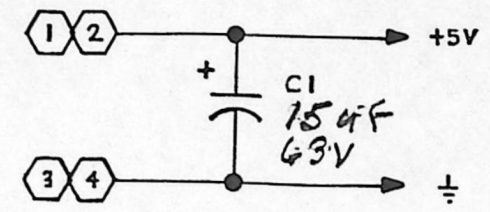
REV: B; C;

TOLERANCES UNLESS OTHERWISE SPECIFIED	FRACTIONS	DEC	ANGLES
±	±	±	±

APPROVALS	DATE
DRAWN S.E.P.	4-5-82
CHECKED	

ATA Corp.			
COMPUTER IMAGE			
ECLIPSE/RPU COMMUNICATION			
CONTROL PANEL - SYSTEM IV			
SCALE	SIZE	DRAWING NO.	
	B	CIC-W-69	
DO NOT SCALE DRAWING		SHEET 1 OF 2	

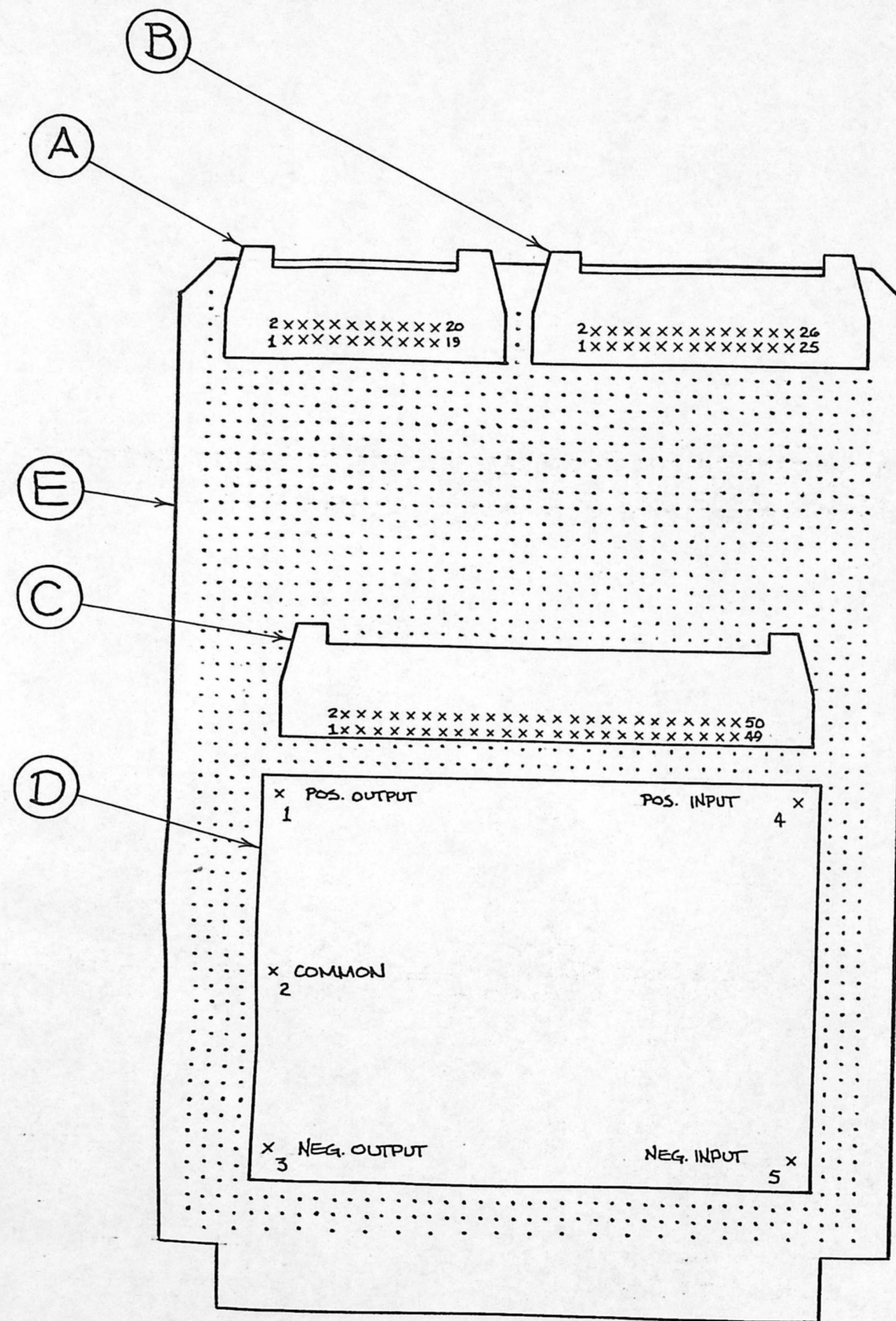
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



REV: B;C

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±
APPROVALS	DATE	
DRAWN	SEP. 4-6-82	
CHECKED		

ATA Corp.			
COMPUTER IMAGE			
ECLIPSE/RPU COMMUNICATION			
CONTROL PANEL - SYSTEM IV			
SCALE	SIZE	DRAWING NO.	
	B	CIC-W-69	
DO NOT SCALE DRAWING			SHEET 2 OF 2



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

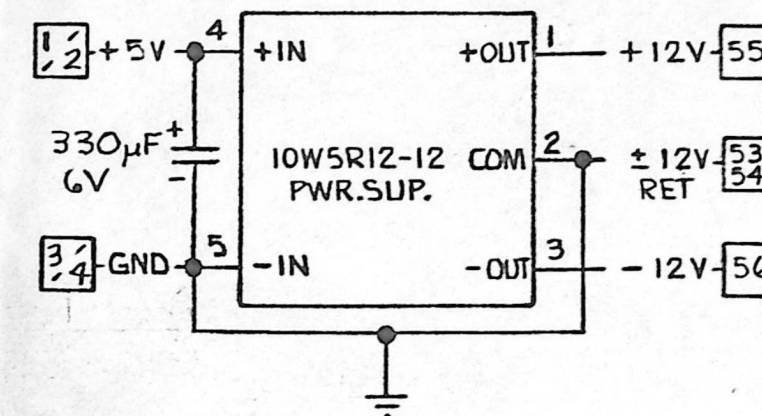
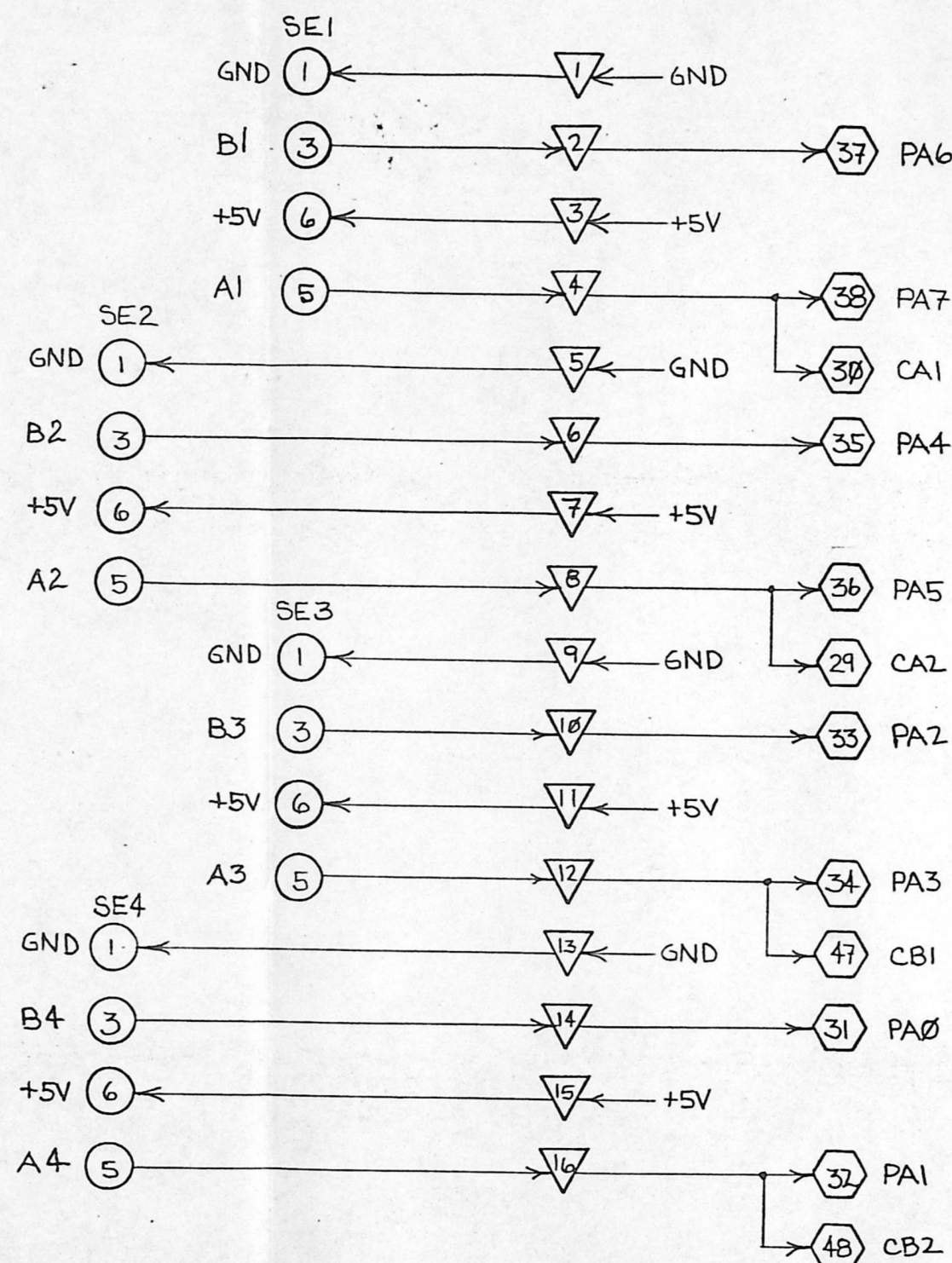
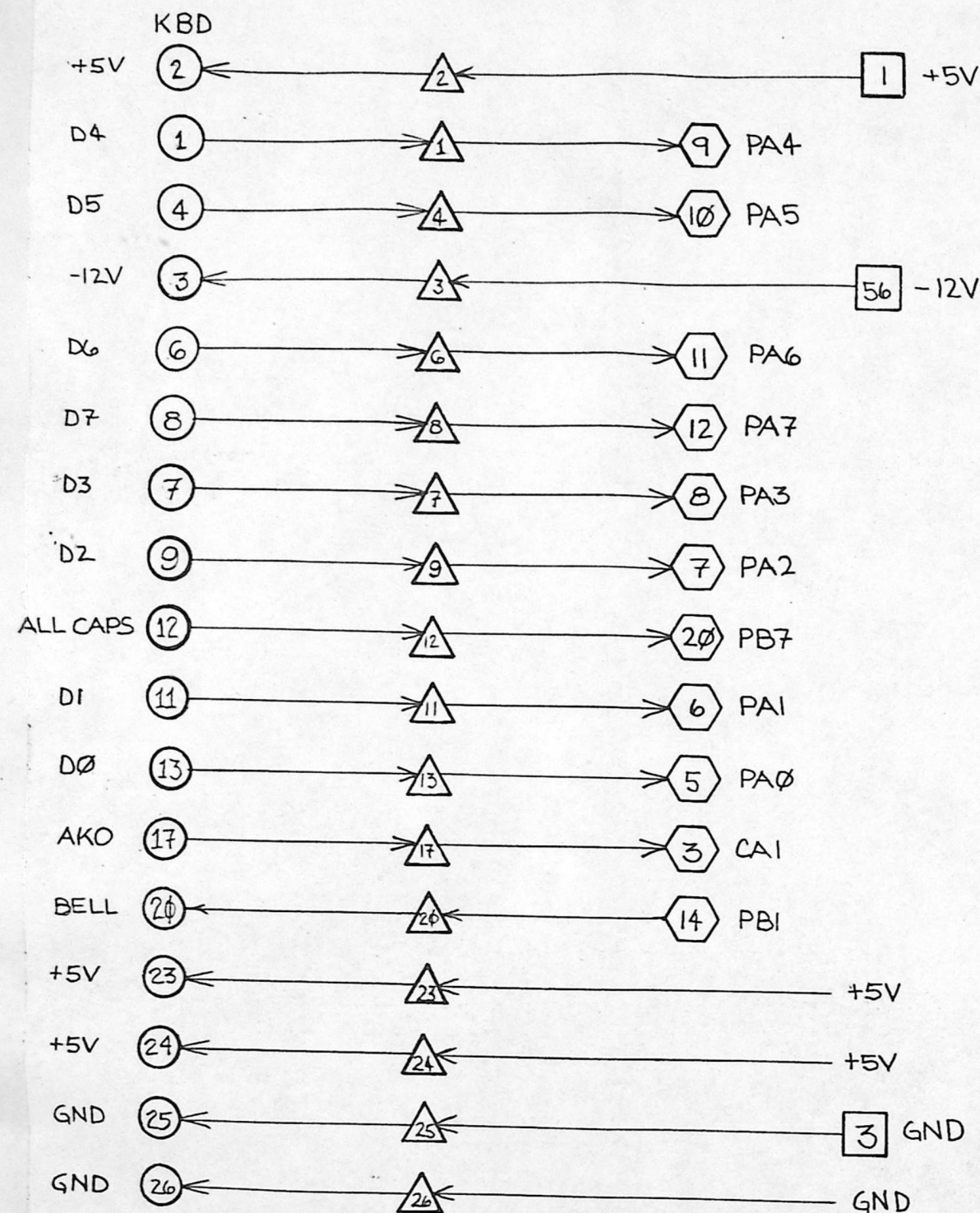
PARTS LIST (REF ONLY)

QUAN	P/N	MFG.	Description	Ref.
1	3428-3205	3M	20 Pin Header	A
1	3429-3205	3M	26 Pin Header	B
1	3433-3205	3M	50 Pin Header	C
1	10W5R12-12	Reliability	5VDC to + 12VDC Converter	D
1	4610-1	Vector	Std. Bus W.W. Board	E

REV: B;

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		ATA Corp.	
		COMPUTER IMAGE	
APPROVALS	DATE	AUX CONNECT/12V P S CONTROL PANEL - SYSTEM IV	
DRAWN S.P.	4-2-82		
CHECKED		SCALE	SIZE DRAWING NO.
			B CIC-W-70
DO NOT SCALE DRAWING		SHEET 1 OF 2	

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
B	AS PER ELO N°: 0204-02L1	4-2-82	



- ▲ 26 PIN CONNECTOR B
 ▼ 20 PIN CONNECTOR A
 ○ CONNECTORS AT KEYBOARD & SHAFT ENCODERS
 ⬡ CONNECTOR TO/FROM 6809 BOARD C
 □ STANDARD BUS PINS

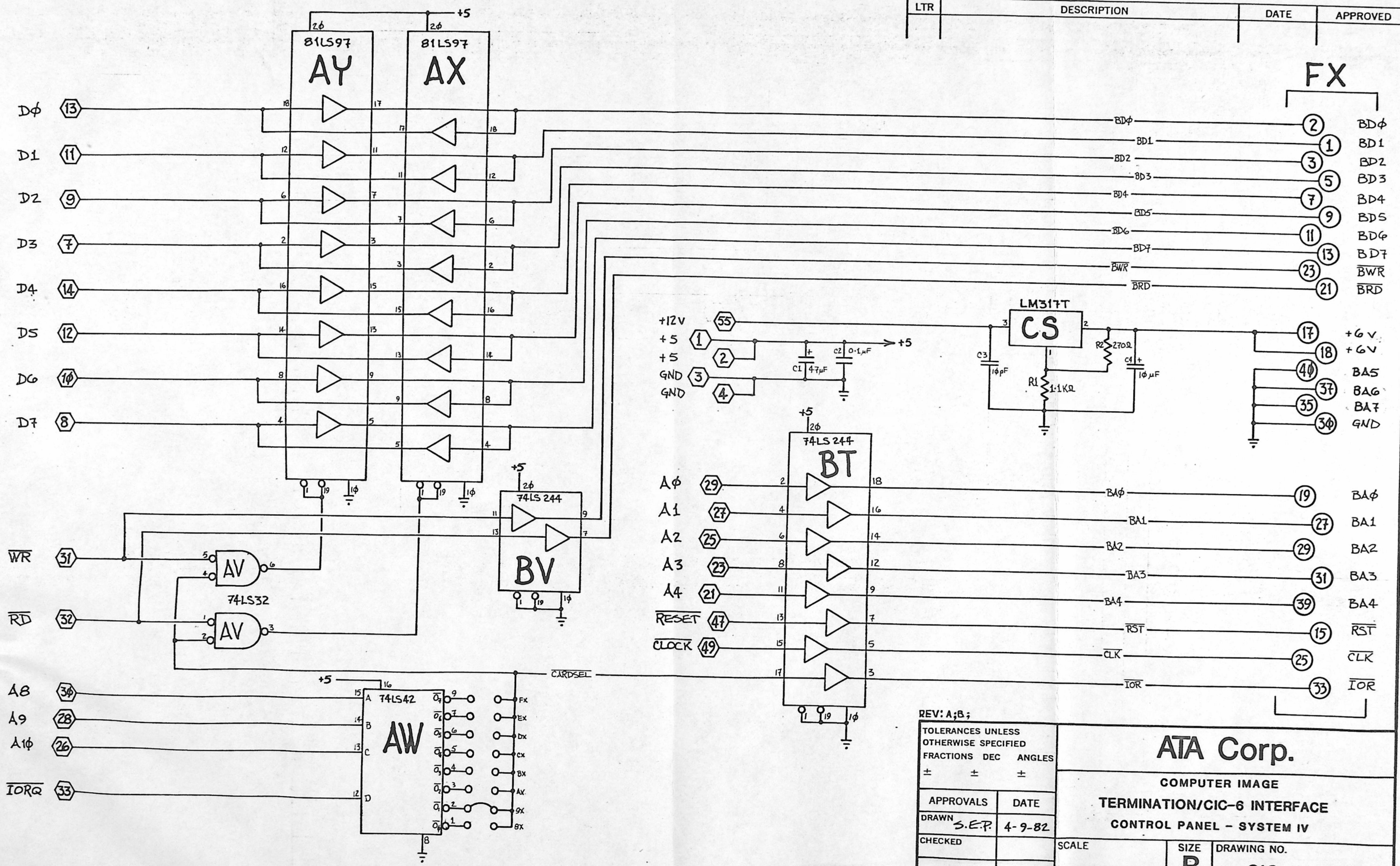
PB7 (46) to 37 VBLNK

REV: B;

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±
APPROVALS	DATE	
DRAWN LPD	9/16/81	
CHECKED		

ATA Corp.			
COMPUTER IMAGE			
AUX CONNECT/12V P S			
CONTROL PANEL - SYSTEM IV			
SCALE	SIZE	DRAWING NO.	
	B	CIC-W-70	
DO NOT SCALE DRAWING			SHEET 2 OF 2

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



REV: A;B;

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

APPROVALS	DATE
DRAWN <i>S.E.P.</i>	4-9-82
CHECKED	

ATA Corp.

COMPUTER IMAGE

TERMINATION/CIC-6 INTERFACE

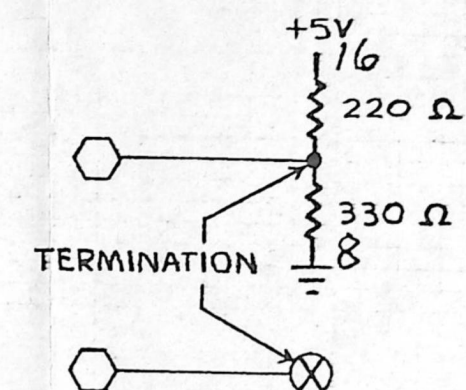
CONTROL PANEL - SYSTEM IV

SCALE	SIZE B	DRAWING NO. CIC-W-71
-------	---------------	-----------------------------

DO NOT SCALE DRAWING SHEET 1 OF 2

D3 7 — X BX-7
D2 9 — X BX-5
D1 11 — X BX-3
D0 13 — X BX-1
A7 15 — X BZ-7
A6 17 — X BZ-5
A5 19 — X BZ-3
A4 21 — X BZ-1
A3 23 — X BY-13
A2 25 — X BZ-12
A1 27 — X BZ-14
A0 29 — X BY-7
WR 31 — X BX-12
IORO 33 — X BY-9
CLOCK 49 — X BX-14

D7 8 — X BX-6
D6 10 — X BX-4
D5 12 — X BX-2
D4 14 — X BX-9
A15 16 — X BZ-6
A14 18 — X BZ-4
A13 20 — X BZ-2
A12 22 — X BZ-9
A11 24 — X BZ-11
A10 26 — X BZ-13
A9 28 — X BX-10
A8 30 — X BX-11
RD 32 — X BX-13
MCSYNC 38 — X BY-10
STATUS 0 40 — X BY-11
INTRO 44 — X BY-12
CNTRL 50 — X BX-15



REV: A; B;

APPROVALS		DATE		COMPUTER IMAGE				
				TERMINATION/CIC-6 INTERFACE				
DRAWN		EVL		4-18-83		CONTROL PANEL - SYSTEM IV		
CHECKED						SCALE	SIZE	DRAWING NO.
								CIC-W-71
						SHEET 2 OF 2		

←	→
↓	↑
{	}
[	]
⋮	CEM

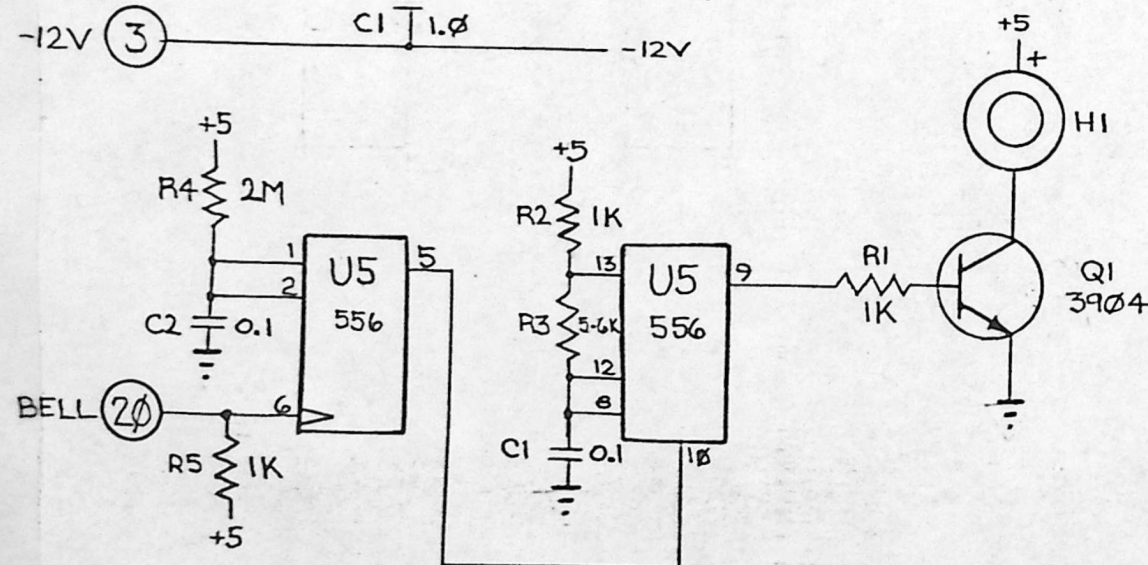
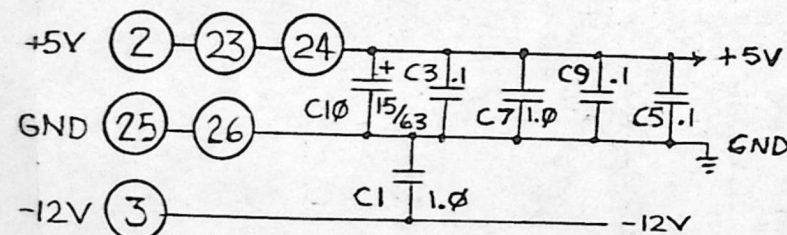
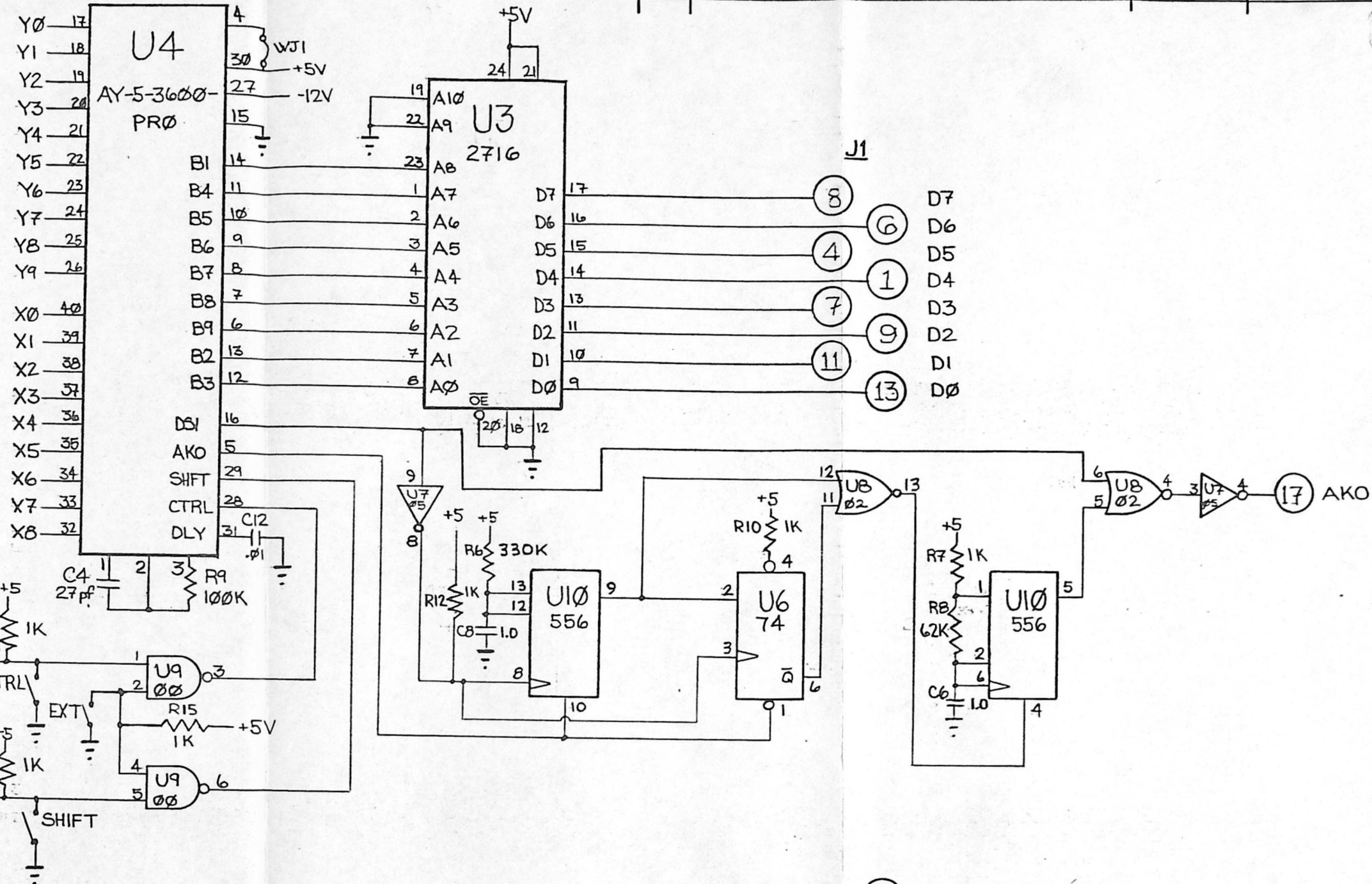
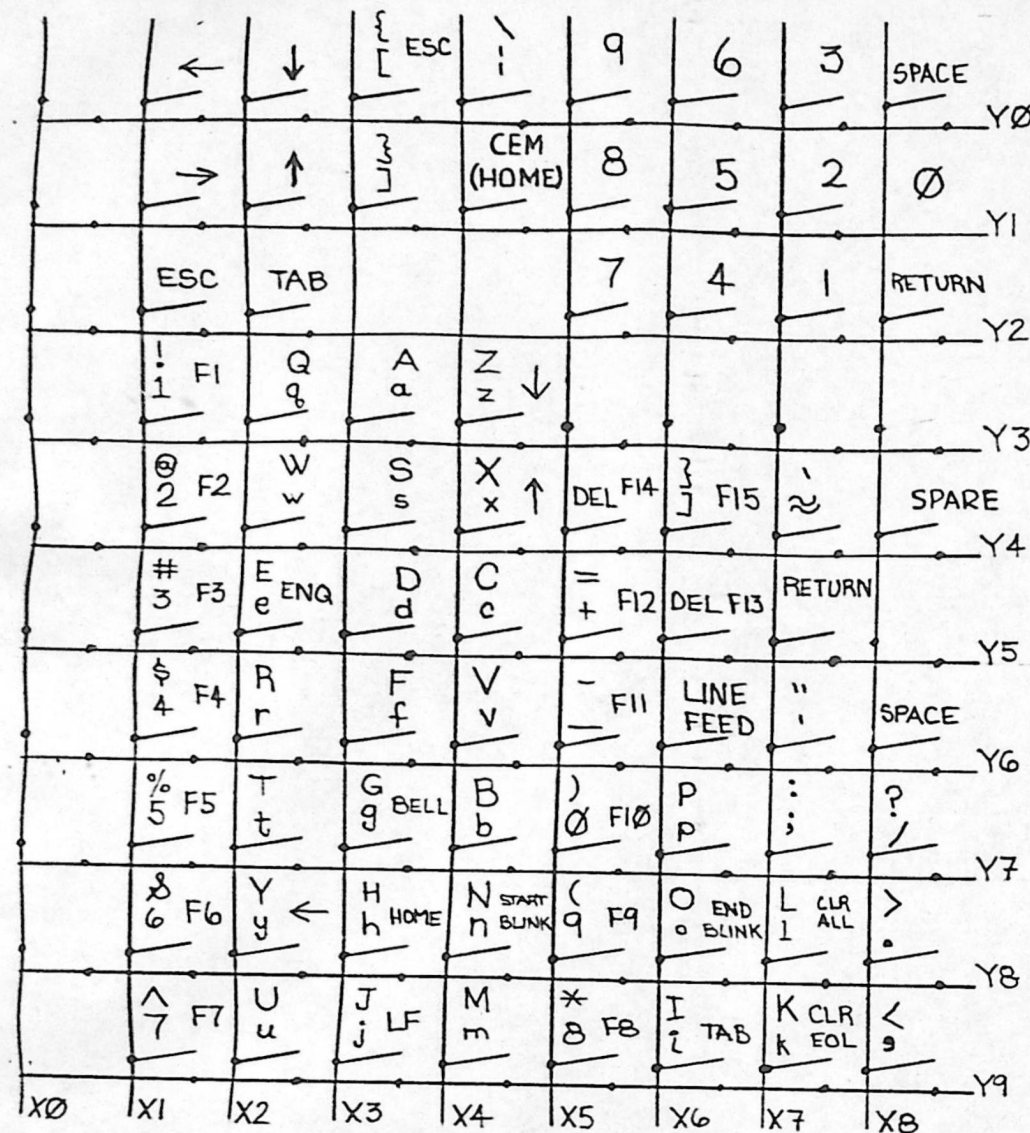
ESC	!	@	#	\$	%	&	^	*	(	)	-	=	DEL	
	1	2	3	4	5	6	7	8	9	0	-	+		
TAB	Q	W	E	R	T	Y	U	I	O	P	LINE FEED			
CAPS LOCK	A	S	D	F	G	H	J	K	L	:	"	RETURN		
											;	/		
SHIFT	Z	X	C	V	B	N	M	<	>	?	SHIFT			
EXT	CONTROL										CONTROL			

7	8	9
4	5	6
1	2	3
RET	Ø	

		COMPUTER IMAGE CORP.		DENVER, CO.	
SCALE	NONE	REVISIONS		BY	DATE
DATE	1-12-81				
DRN	BSH	CRD			
APVD					
TITLE				NO	
SYSTEM IV					
KEYBOARD				CIC-W-73	

KEYBOARD PCB SCI-PRO SP-100

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	AS PER E.C.O NO: 0204-02L1	4-2-82	

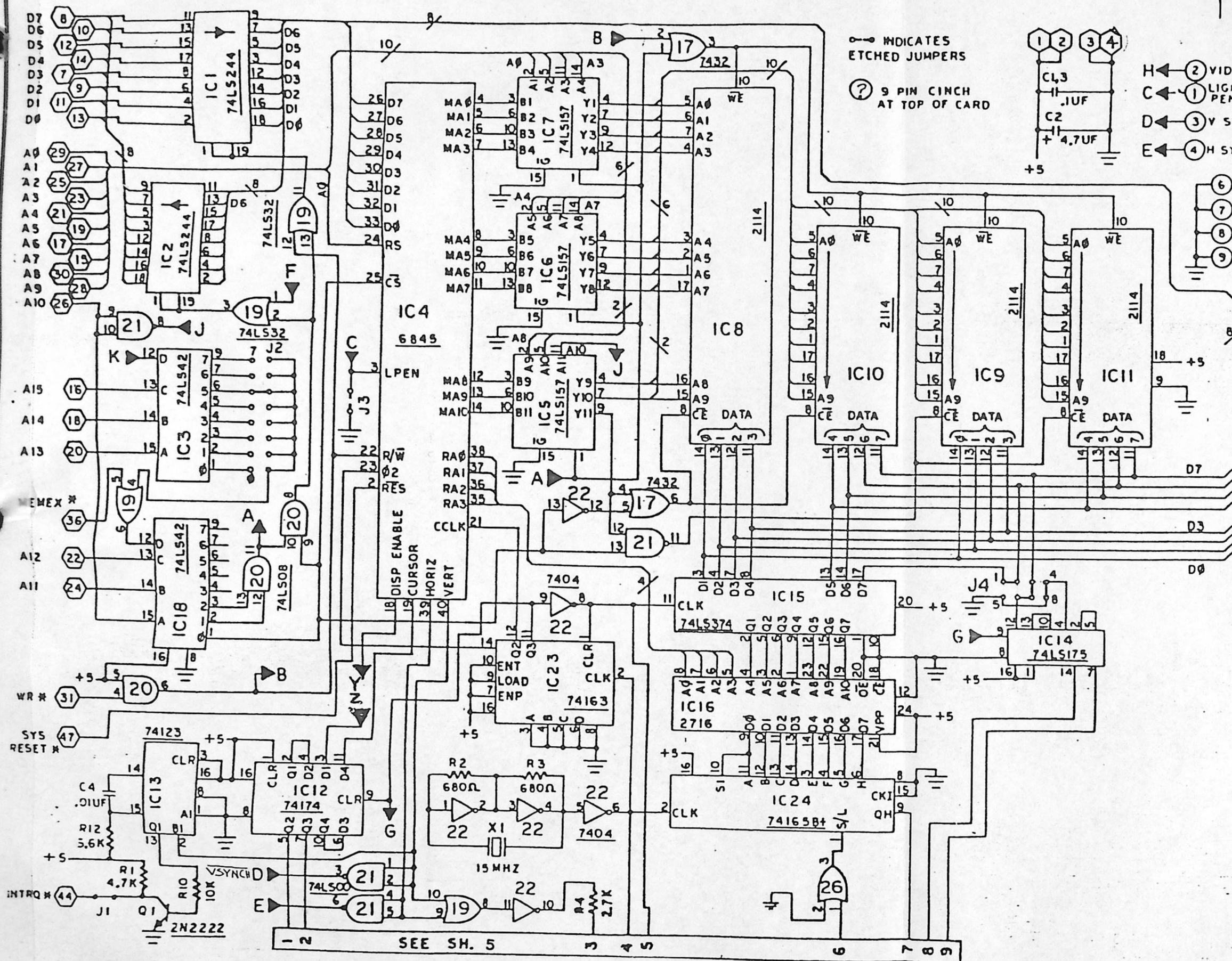


NOTE: ALL CAPACITOR VALUES IN MICROFARADS UNLESS OTHERWISE NOTED

REV: A,

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±
APPROVALS	DATE	
DRAWN LPD	9/10/81	
CHECKED		

ATA Corp.			
COMPUTER IMAGE			
TERMINAL KEYBOARD			
CONTROL PANEL - SYSTEM IV			
CIC-W-73	SIZE B	DRAWING NO.	10918L1
DO NOT SCALE DRAWING		SHEET 2 of 2	



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Microlink CRT Controller

97098

Jumper Installation

- J1 - Install Interrupt Enable
- J2 - 5 NO CHANGE (FACTORY INSTALLED)
- J3 - No change (Factory Installed)
- J4 - Character Highlighting Cut Etches:
1-5
2-6
3-4
Install Jumpers:
4-8
3-7
1-2

REV: A; B;

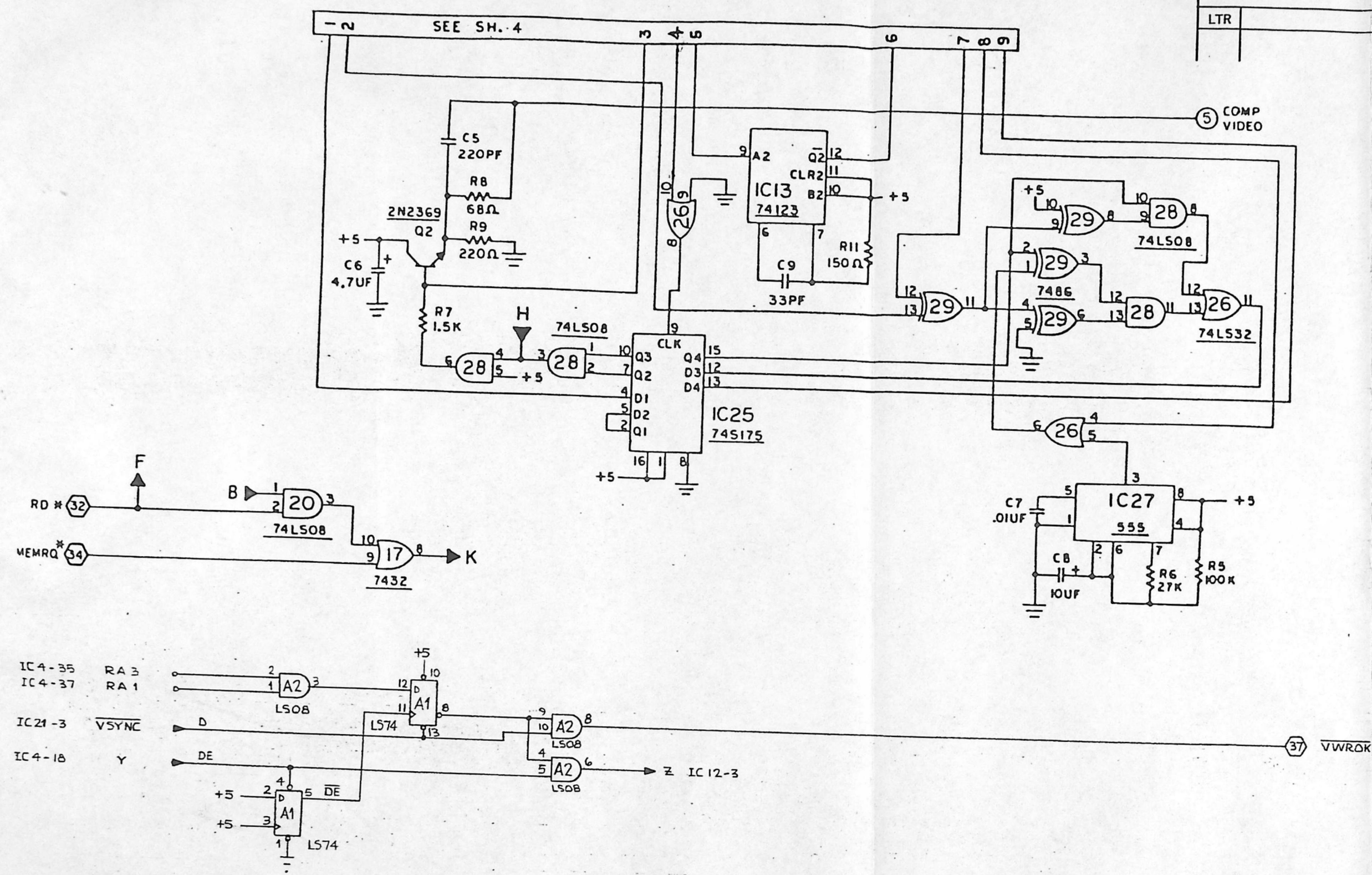
TOLERANCES UNLESS OTHERWISE SPECIFIED	
FRACTIONS	DEC ANGLES
±	±
APPROVALS	DATE
DRAWN	
CHECKED	

ATA Corp

COMPUTER IMAGE
CRT CONTROLLER
CONTROL PANEL-SYSTEM IV

SCALE	SIZE	DRAWING NO.
	B	CIC-W-74
DO NOT SCALE DRAWING		SHEET 1 OF 2

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

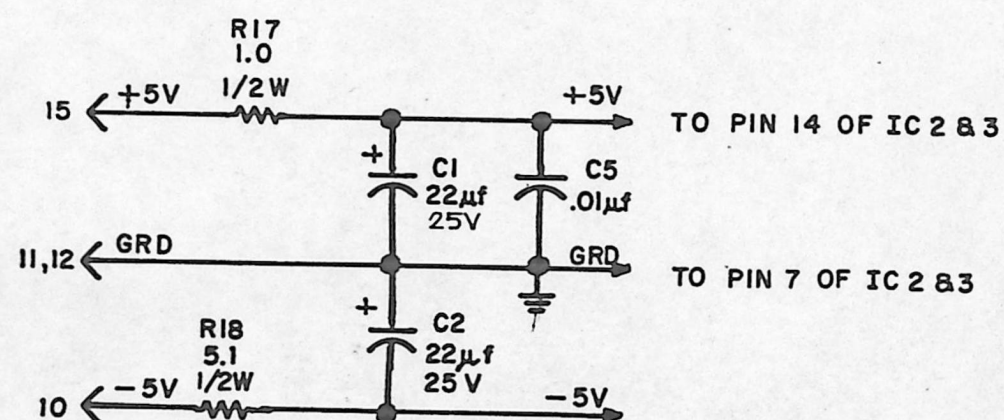
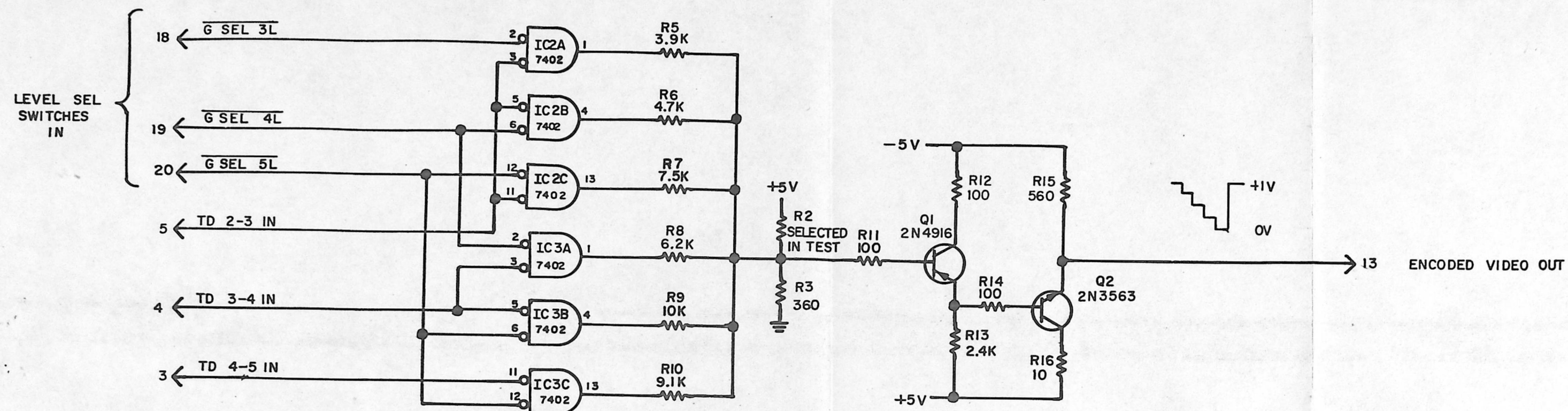


IC4-35 RA 3
 IC4-37 RA 1
 IC21-3 VSYNC
 IC4-18 Y

REV: A; B;

TOLERANCES UNLESS OTHERWISE SPECIFIED	
FRACTIONS	DEC ANGLES
±	± ±
APPROVALS	DATE
DRAWN	
CHECKED	

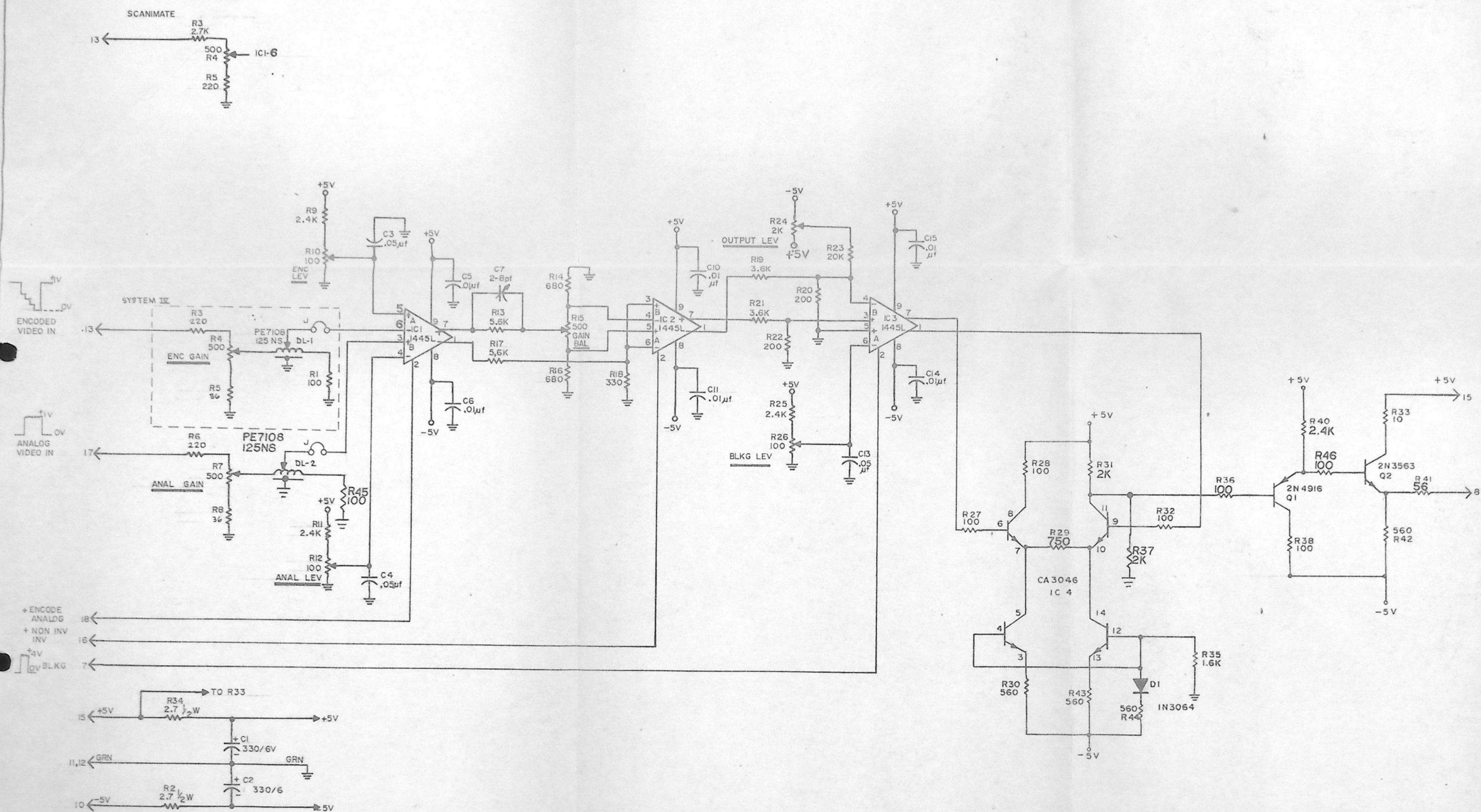
ATA Corp.	
COMPUTER IMAGE	
CRT CONTROLLER	
CONTROL PANEL-SYSTEM IV	
SCALE	SIZE B
DRAWING NO. CIC-W-74	
DO NOT SCALE DRAWING	
SHEET 2 OF 2	



NOTE
ALL RESISTORS ARE 1/4WATT $\pm 5\%$, UNLESS OTHERWISE SPECIFIED.

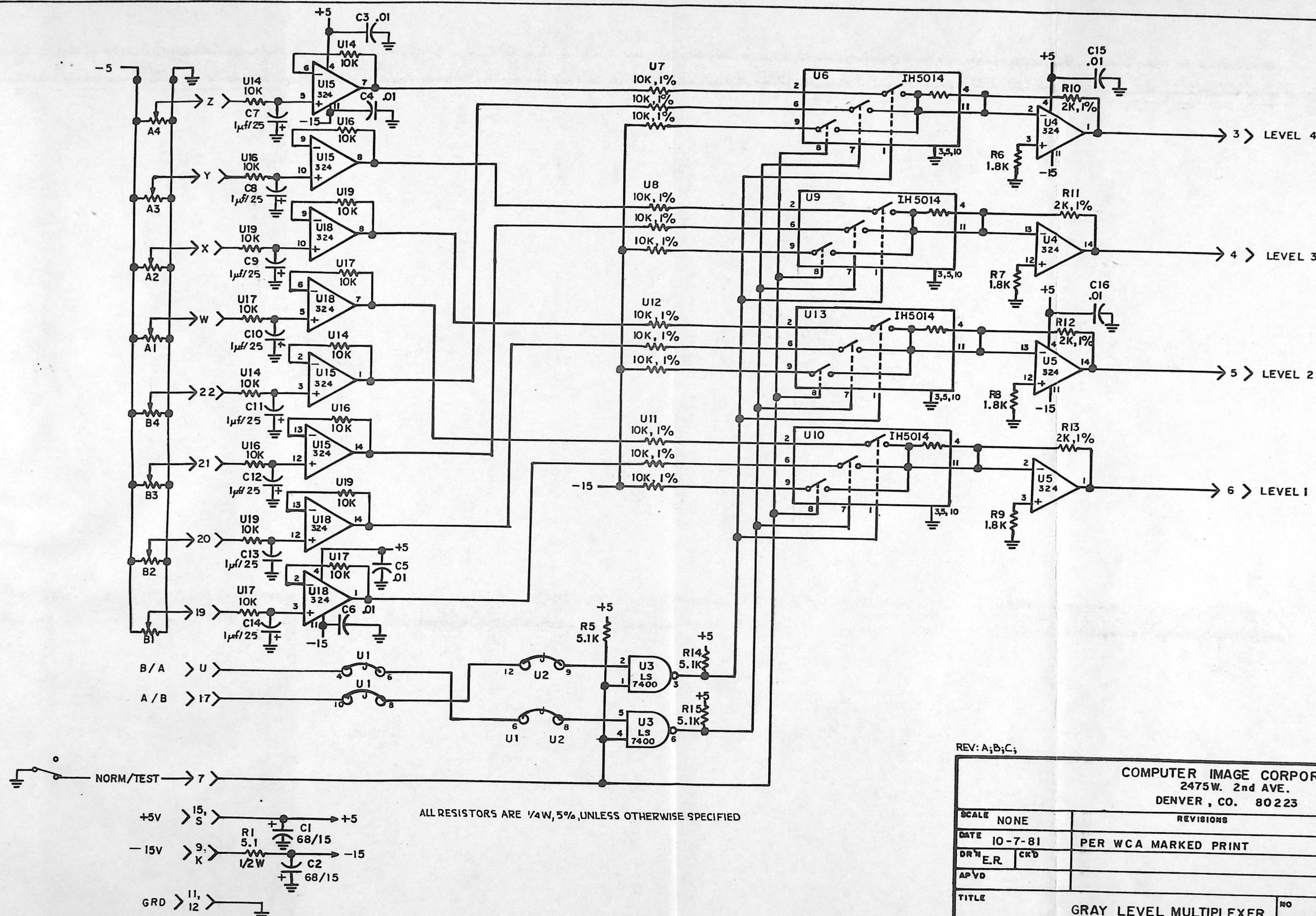
REV: A,B;

COMPUTER IMAGE CORPORATION 2475 W. 2nd AVE DENVER, CO. 80223			
SCALE NONE	REVISIONS	BY	DATE
DATE 6-19-82			
DRN E.R. CKD			
APVD			
TITLE	GRAY LEVEL SWITCHES		NO CVS-III-1 SH 1 OF 1



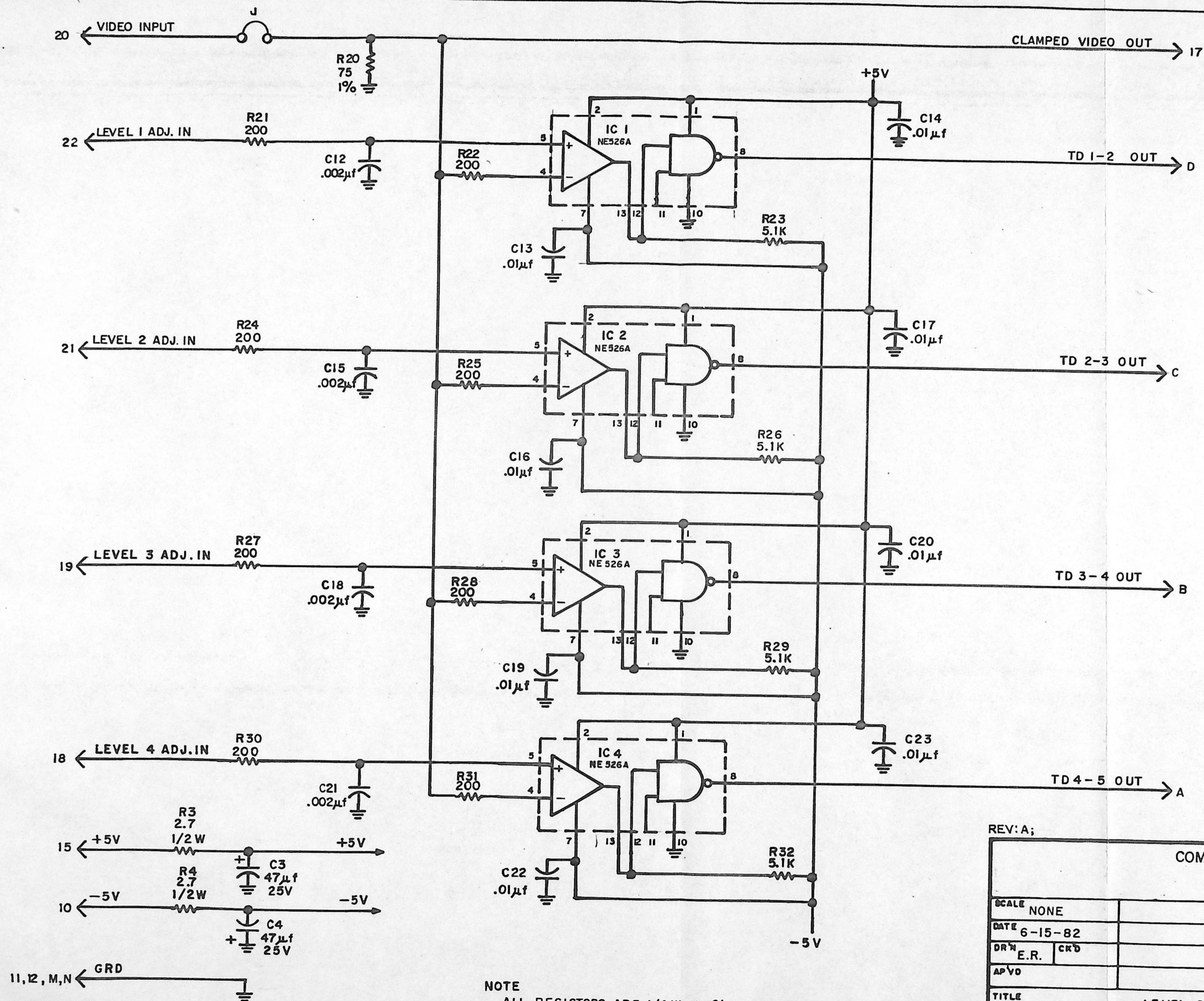
REV: A, B, C;

COMPUTER IMAGE CORPORATION		2475 W. 2nd AVE. DENVER, COLORADO 80223	
SCALE	NONE	REVISIONS	BY DATE
DATE	11/20/75	REV "B"	DM 11-16-75
DRN	ADM	REV "C"	DJR 3-11-80
APR	ED		
TITLE		CVS-112	
GRAY LEVEL ENCODER VIDEO AMPS		SH 1 OF 1	



REV: A;B;C;

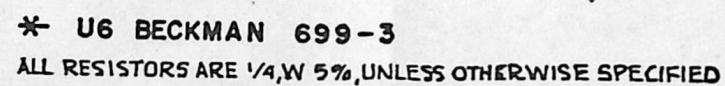
COMPUTER IMAGE CORPORATION 2475 W. 2nd AVE. DENVER, CO. 80223			
SCALE NONE	REVISIONS		BY
DATE 10-7-81	PER WCA MARKED PRINT		E.R.
DRN E.R.	CRD		
APVD			
TITLE GRAY LEVEL MULTIPLEXER			NO CVS-114-2 SH 1 OF 1



NOTE
ALL RESISTORS ARE 1/4 W, $\pm 5\%$ UNLESS OTHERWISE SPECIFIED.

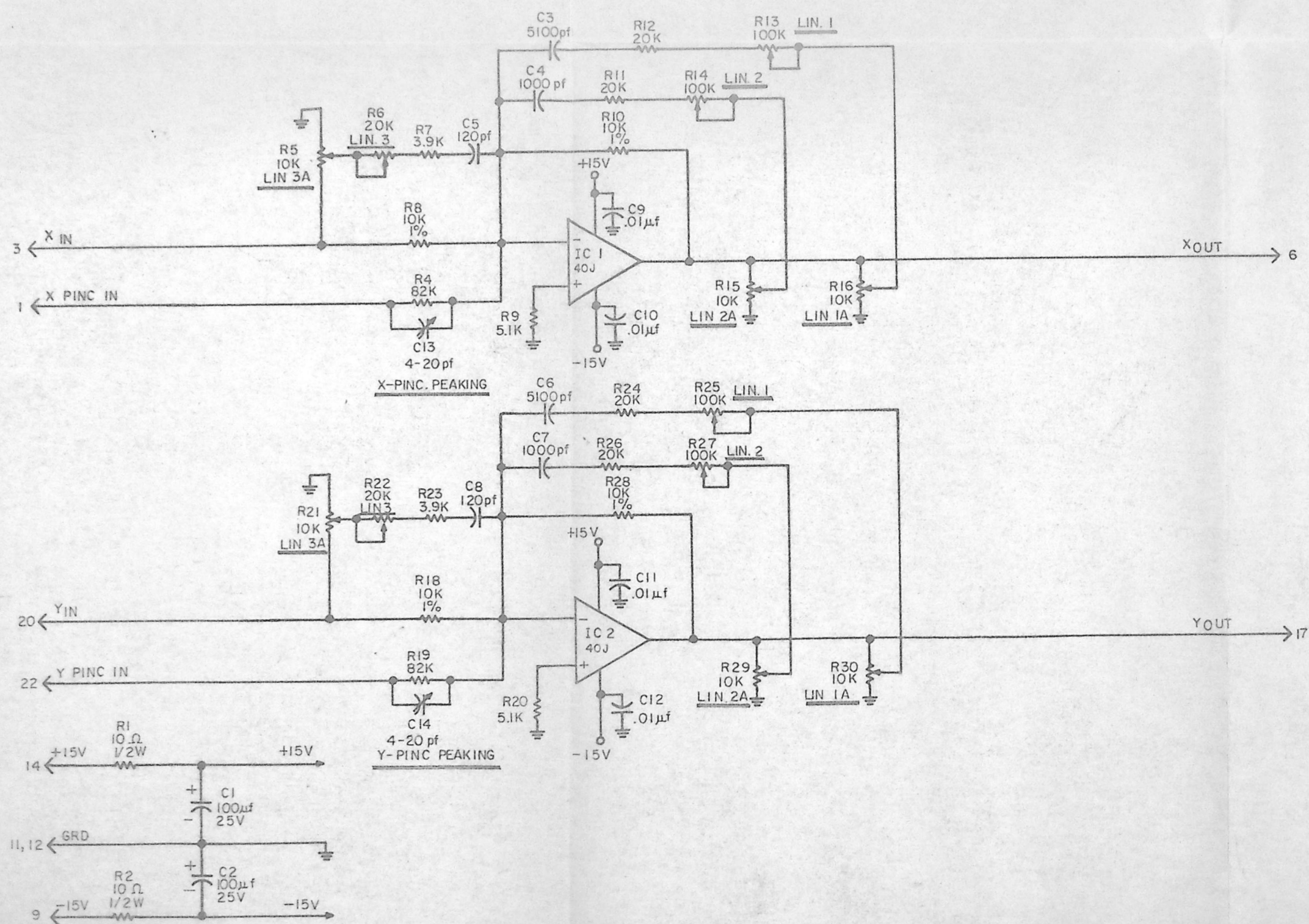
REV: A;

COMPUTER IMAGE CORPORATION 2475 W. 2nd AVE DENVER, CO. 80223			
SCALE NONE	REVISIONS	BY	DATE
DATE 6-15-82			
DRN E.R.	CKD		
APVD			
TITLE LEVEL DETECTORS VIDEO PROCESSOR		NO CVS-125-2 SH 1 OF 1	

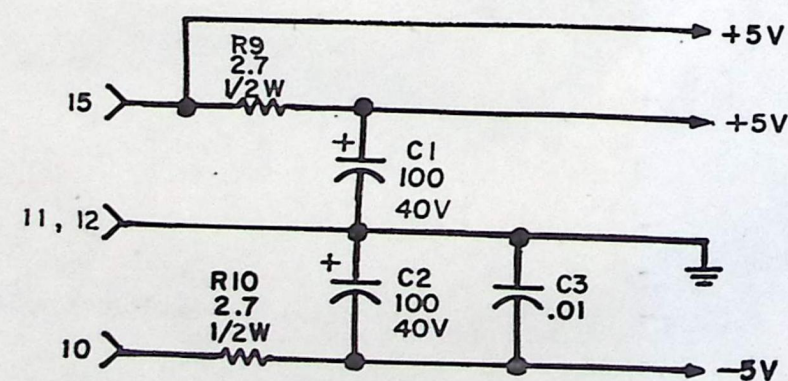
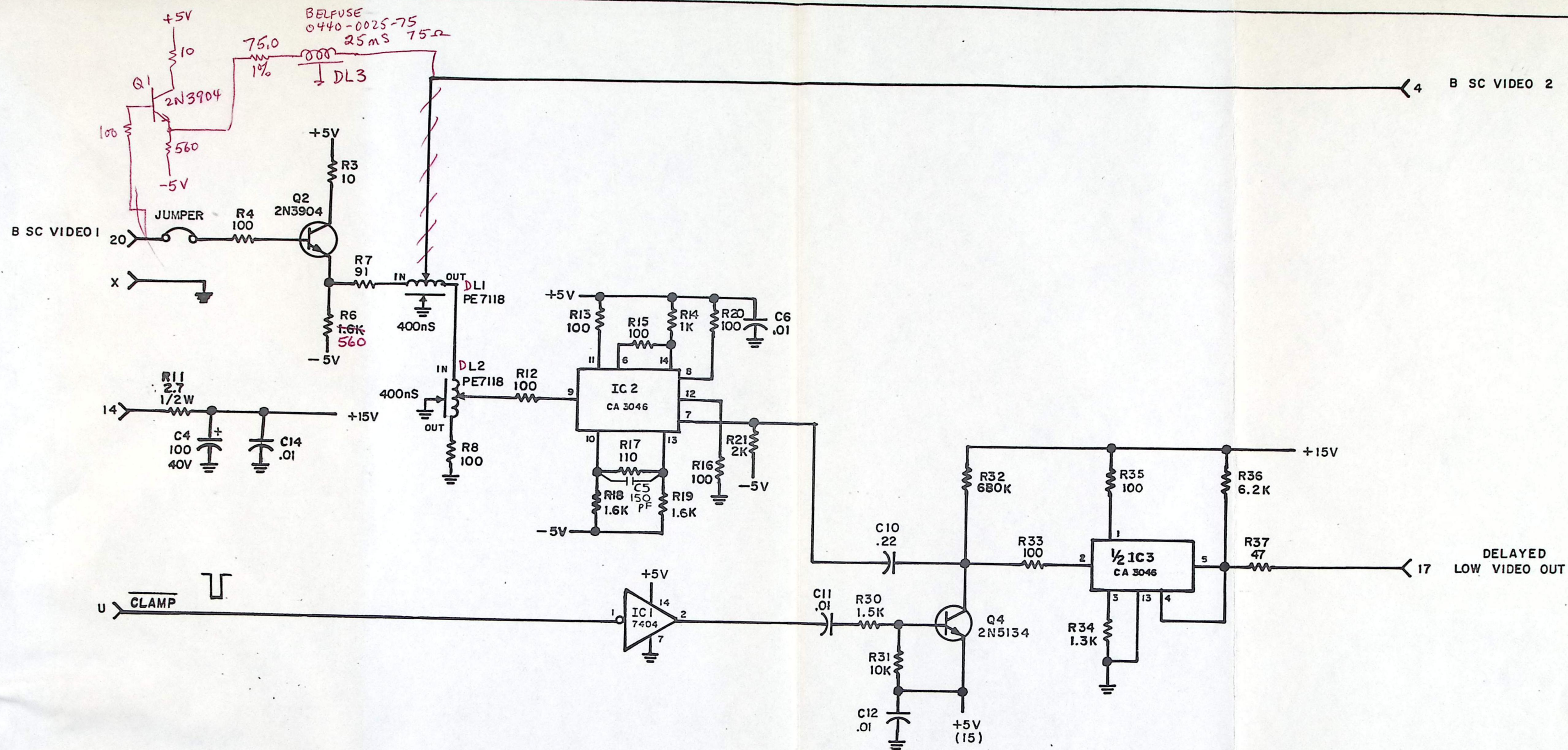


COMPUTER IMAGE CORPORATION
2475 W. 2nd AVE
DENVER, CO. 80223

SCALE NONE		REVISIONS		BY	DATE
DATE 6-19-82					
DRW E.R.	CR'D				
APVD					
TITLE		SYSTEM IV MON. PINCUSHION CORRECTION		NO CVS-127-2 SH 1 OF 1	



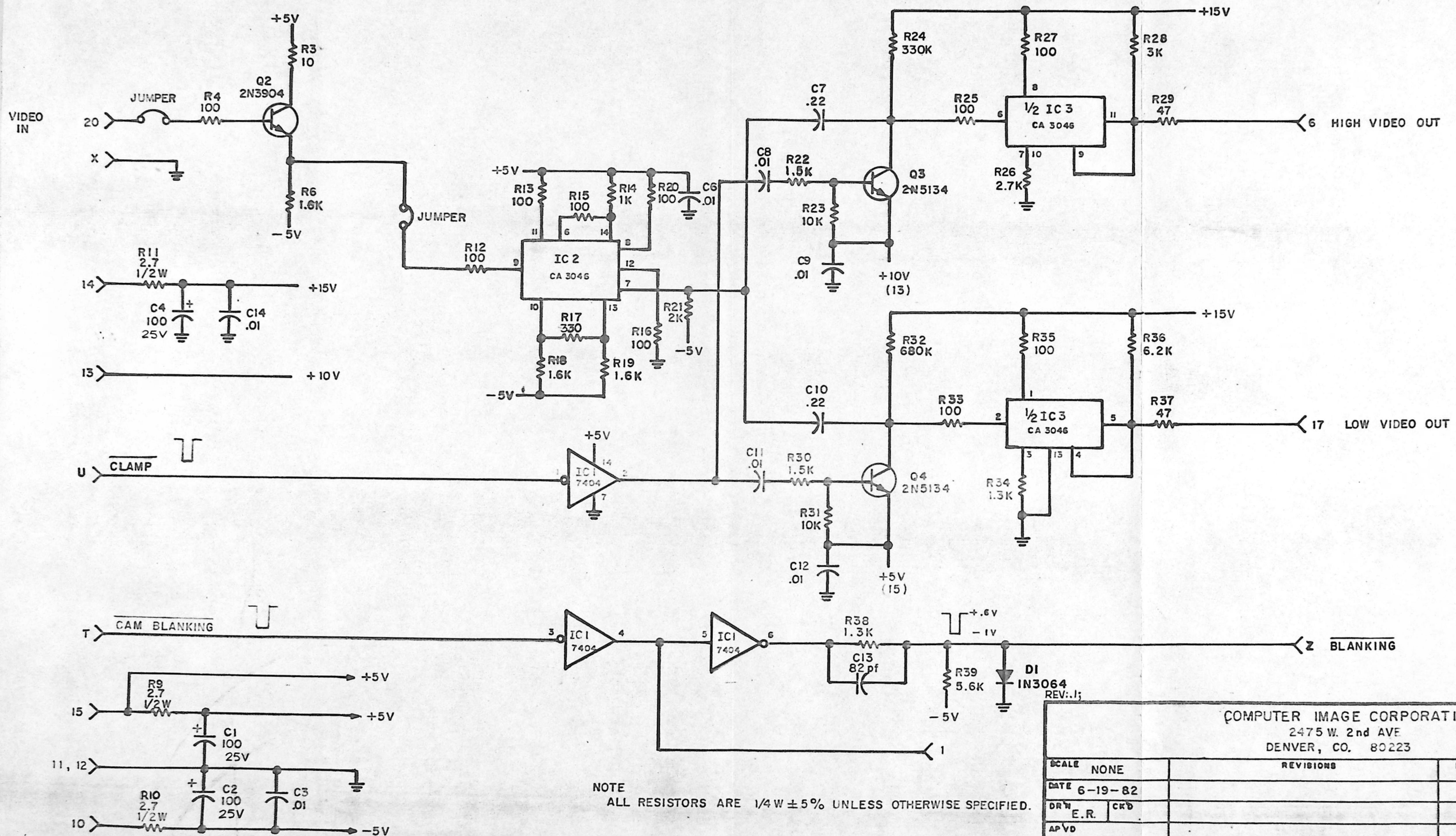
REV:		COMPUTER IMAGE CORPORATION		2475 W. 2nd AVE. DENVER, COLORADO 80223.	
SCALE	NONE	REVISION		BY	DATE
DATE	10-19-72				
DRN	E. R.	CRD.			
AP-VD.					
TITLE MON YOKE COMP & PINCUSHION ADDER					NO. CVS-128 SH 1 OF 1



NOTE:
ALL RESISTORS ARE 1/4W ± 5% UNLESS OTHERWISE SPECIFIED.
ALL CAPS IN μ F UNLESS OTHERWISE SPECIFIED

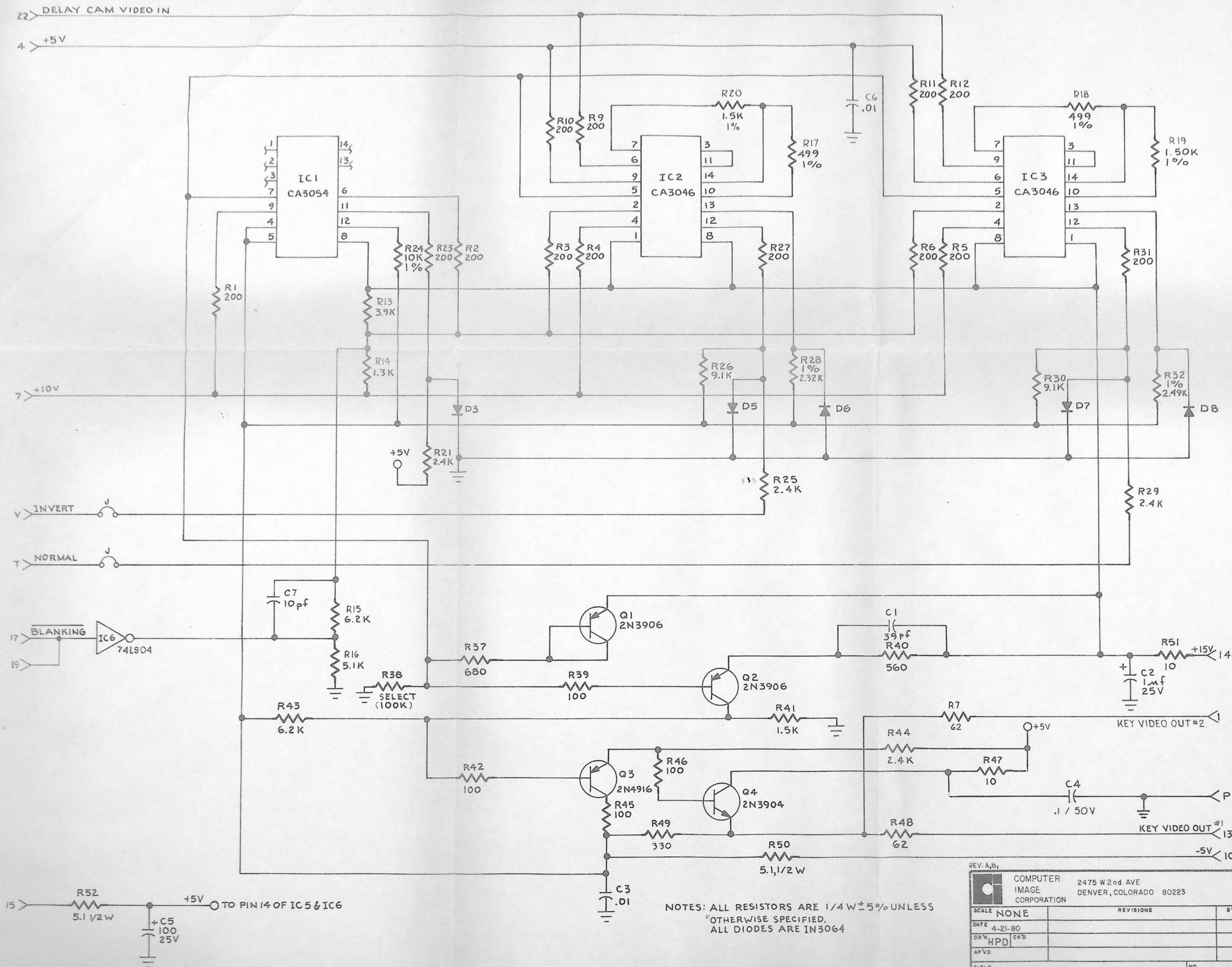
REV:

COMPUTER IMAGE CORPORATION 2475 W. 2nd AVE DENVER, CO. 80223			
SCALE NONE	REVISIONS	BY	DATE
DATE 6-19-82			
DRW E.R. CRB			
APVD			
TITLE	DELAY AMP		NO
	CVS-134-3		SH 1 OF 1

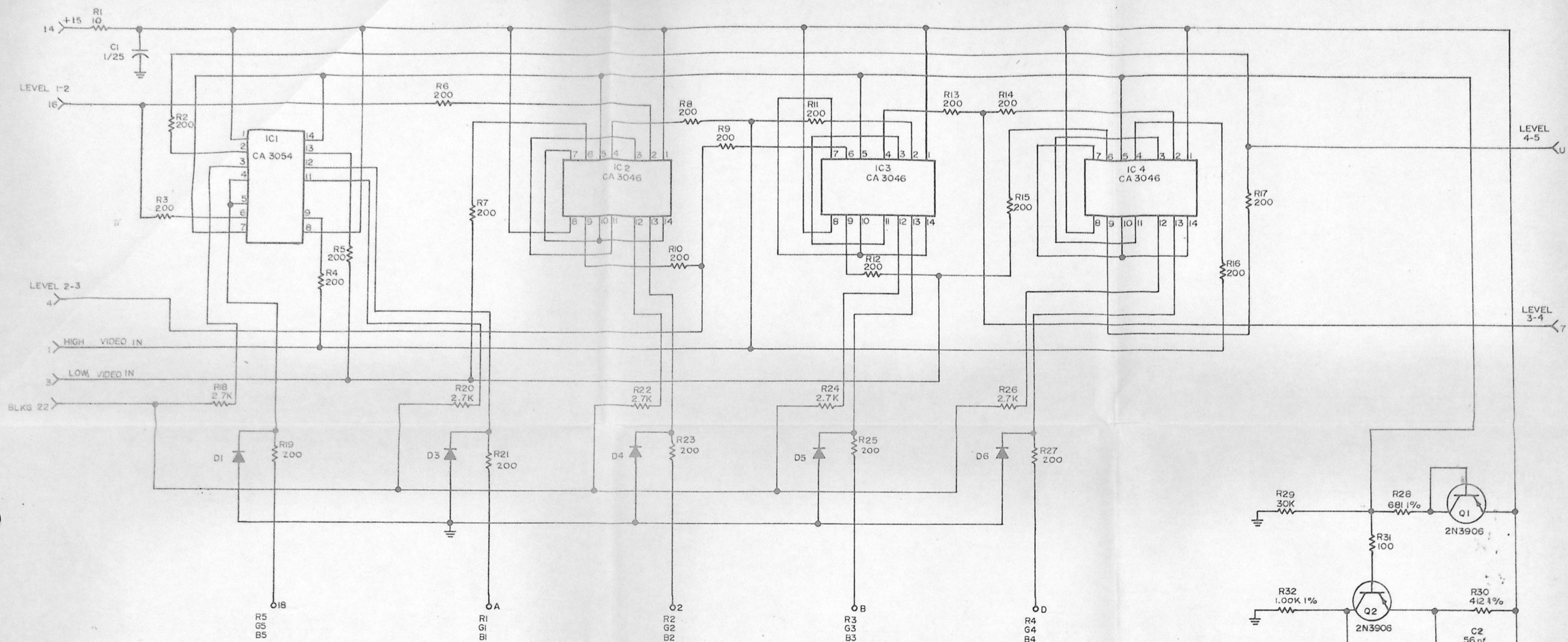


NOTE
ALL RESISTORS ARE 1/4 W $\pm$ 5% UNLESS OTHERWISE SPECIFIED.

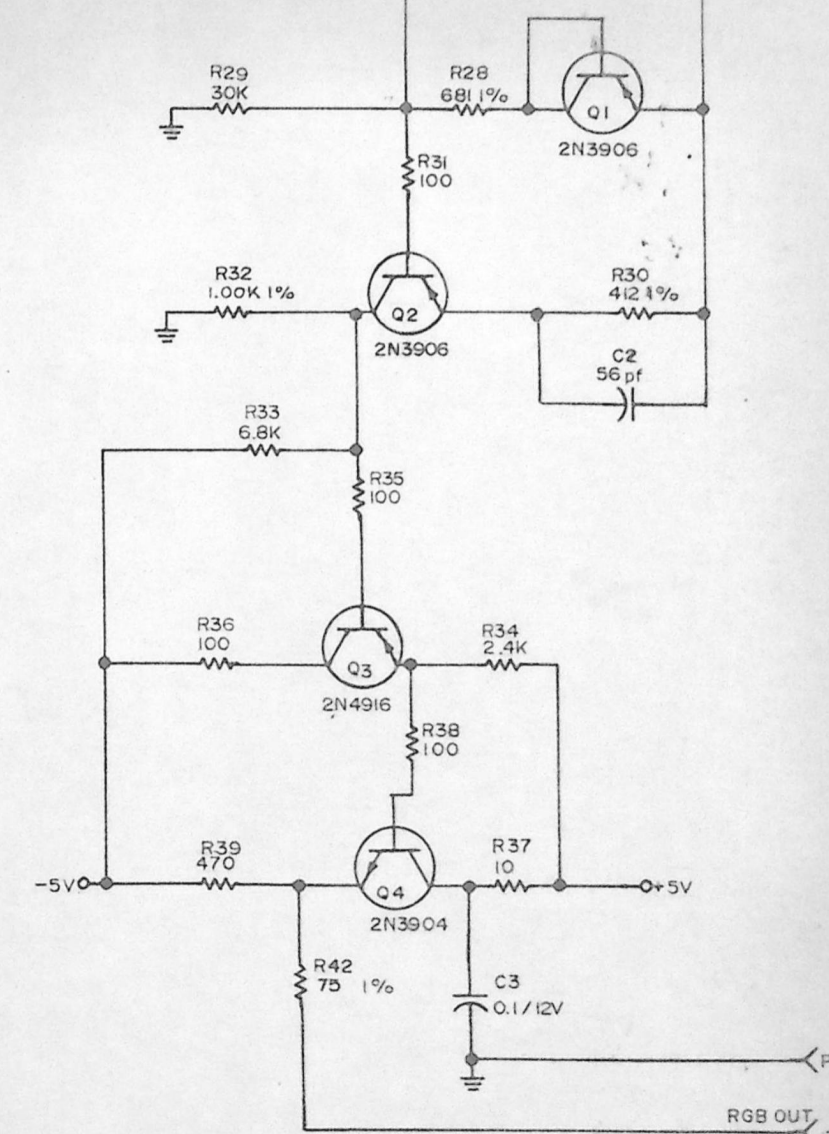
COMPUTER IMAGE CORPORATION 2475 W. 2nd AVE DENVER, CO. 80223			
SCALE NONE	REVISIONS	BY	DATE
DATE 6-19-82			
DRW E.R.	CRD		
APVD			
TITLE		NO	
INPUT AMP		CVS-134-4	
		SH 1 OF 1	



REV. A, B, C		COMPUTER IMAGE CORPORATION		2475 W. 2nd AVE DENVER, COLORADO 80223	
SCALE	NONE	REVISIONS		BY	DATE
DATE	4-21-80				
DRN	HPD	CRD			
APVD					
TITLE BACKGROUND COMPARATORS				NO CVS-135-1	
				SH 1 OF 1	

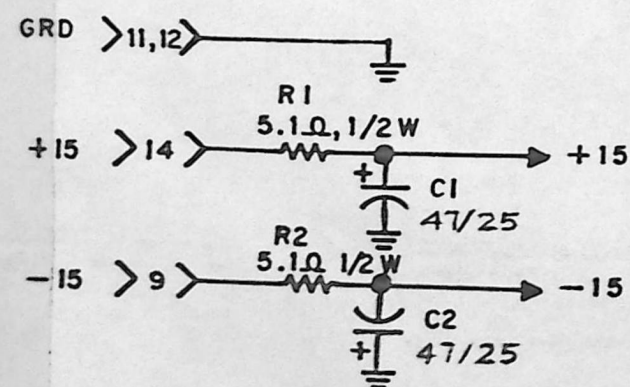
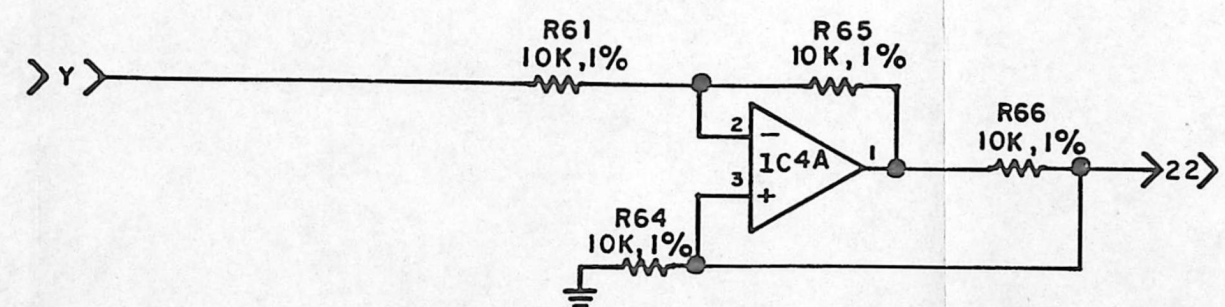
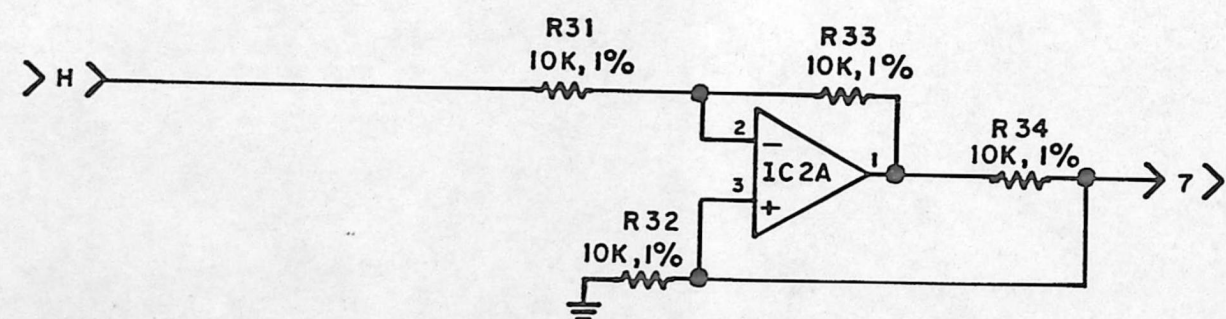
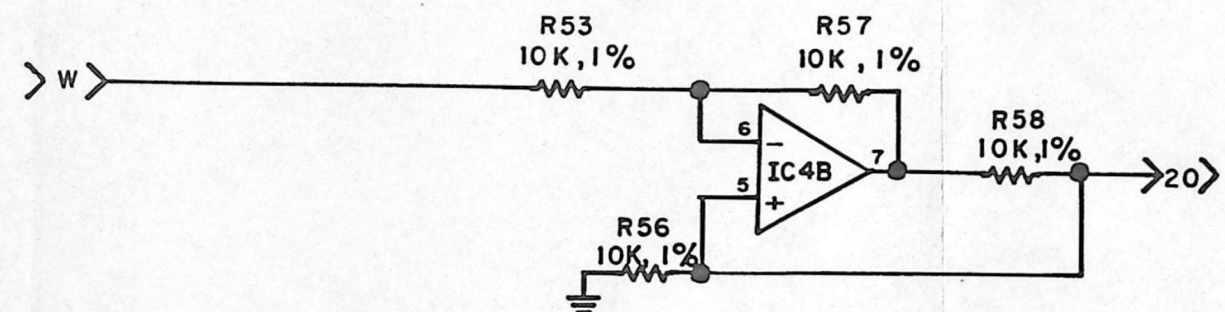
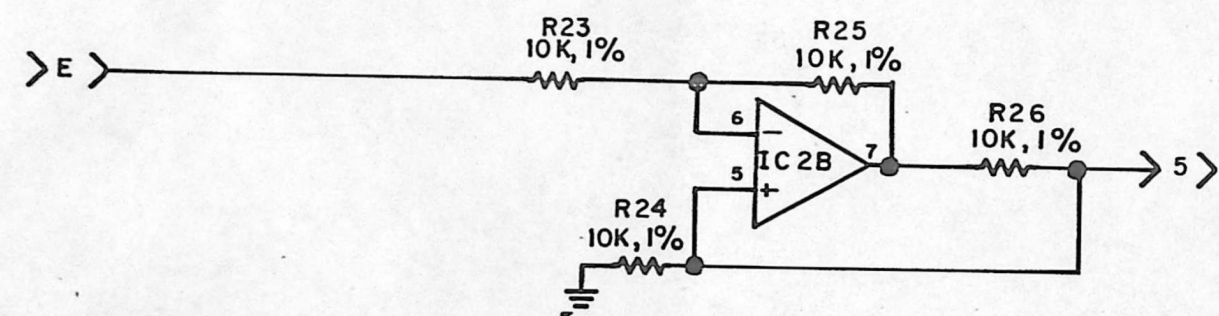
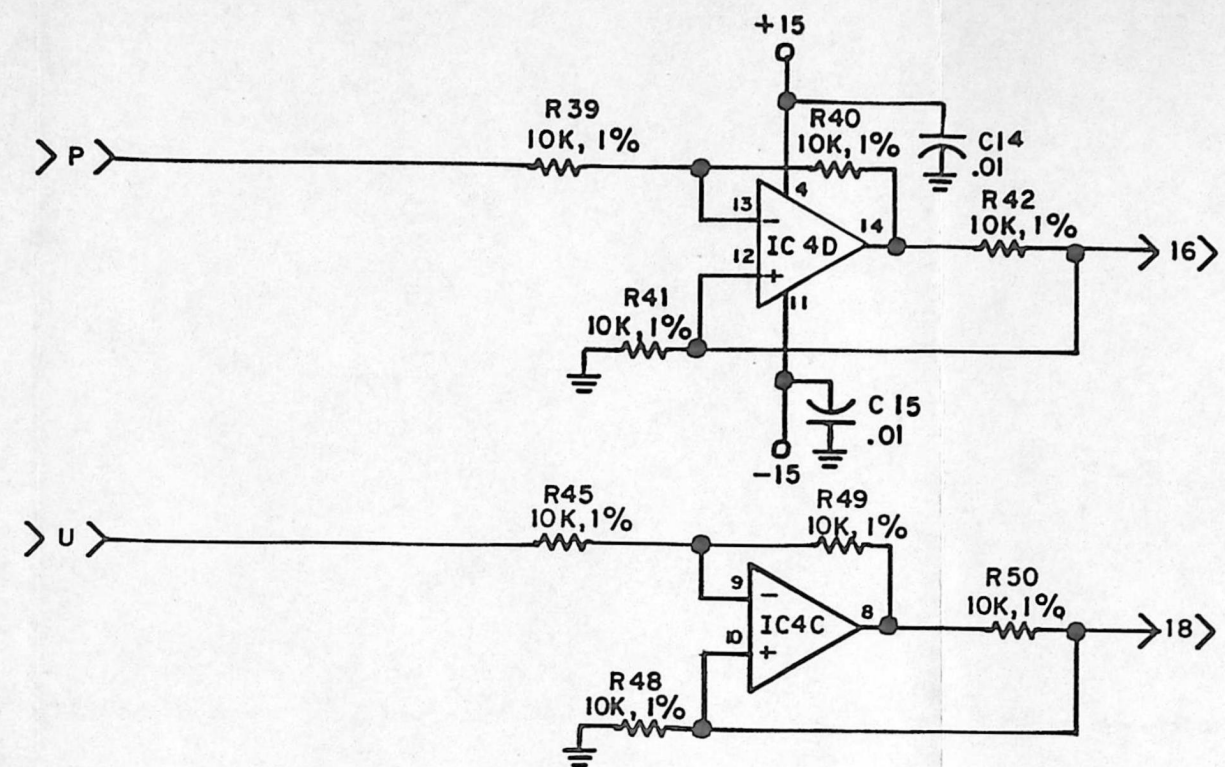
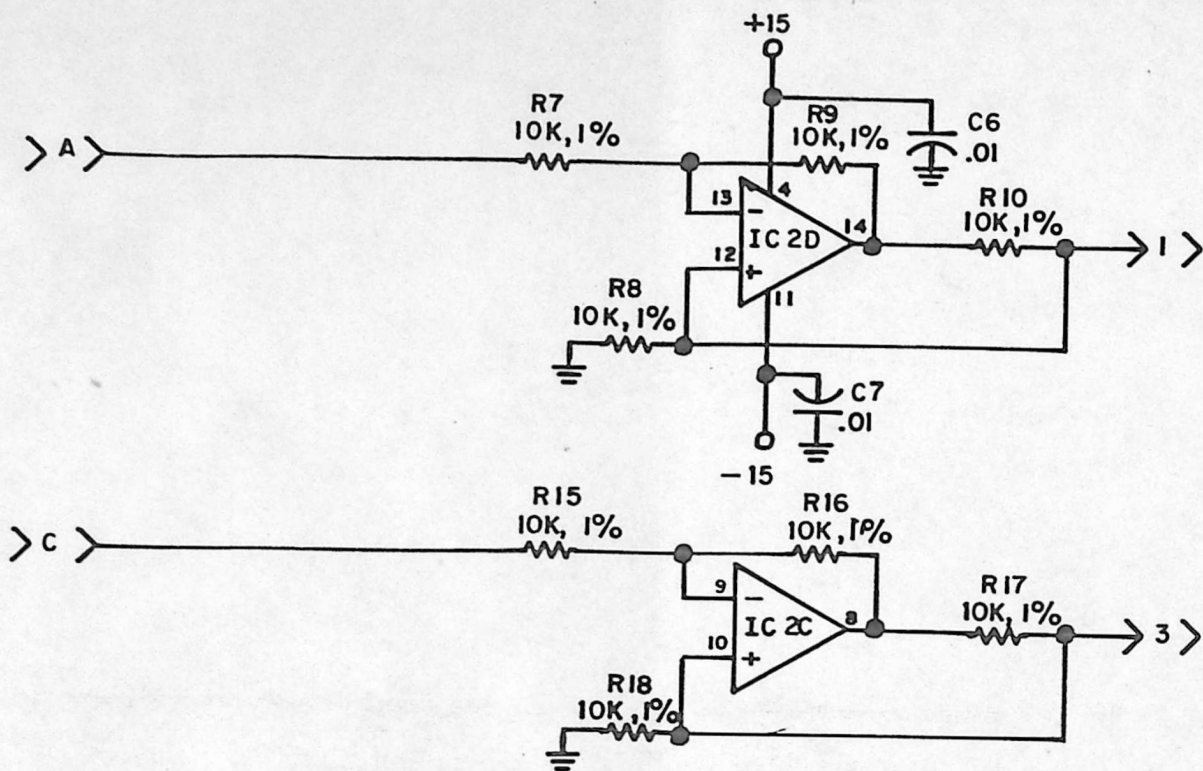


"NOTES"
ALL RESISTORS ARE 1/4W ±5% UNLESS OTHERWISE SPECIFIED
ALL DIODES ARE 1N3064



REV:

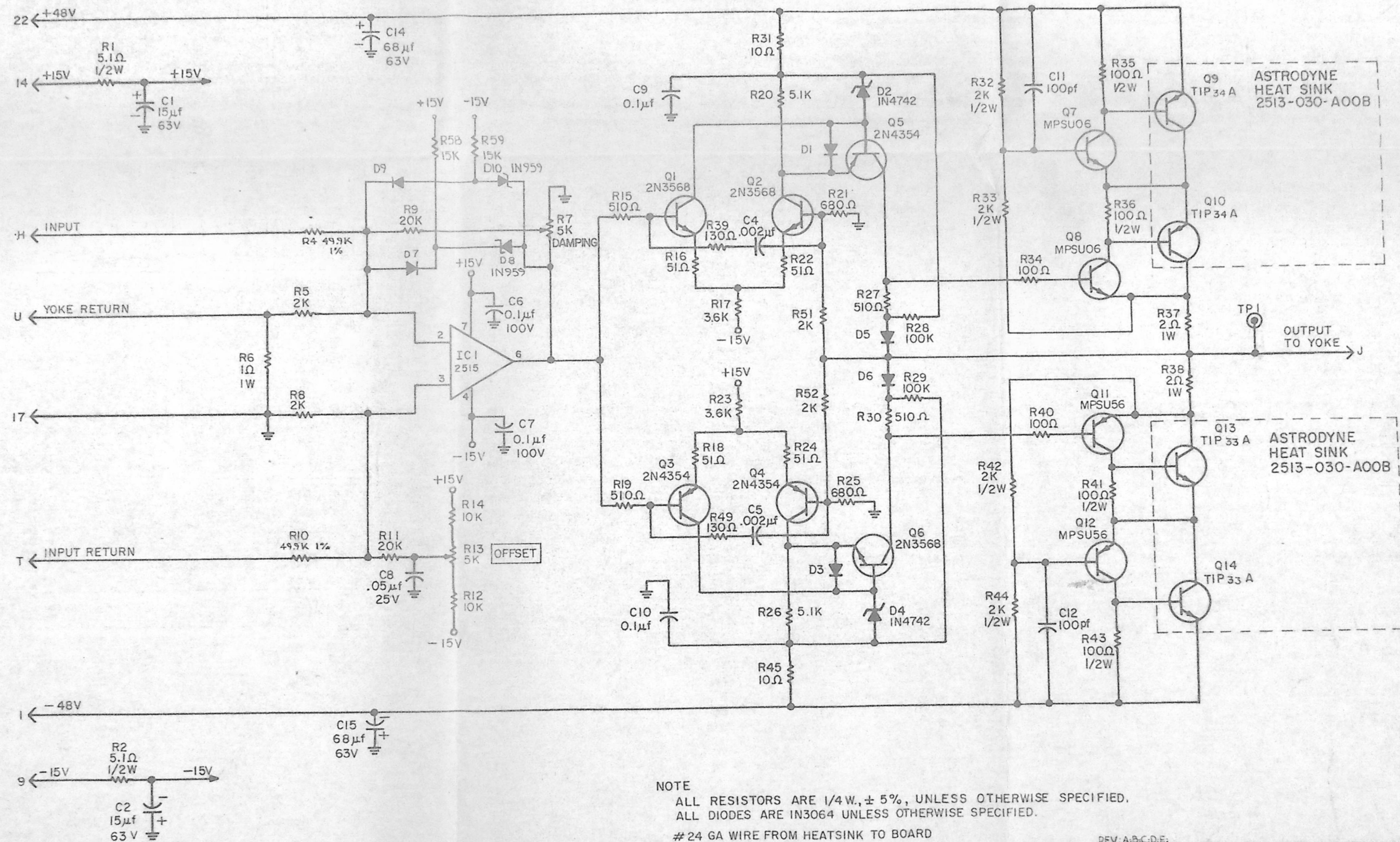
COMPUTER IMAGE			
SCALE	NONE	REVISION	
DATE	11/29/73	BY	
DESIGN	R.K.P.	CAD	
APPROVED			
TITLE	COLOR COMPARATOR		
NO.	CVS-136-2		
	SH 1 OF 1		



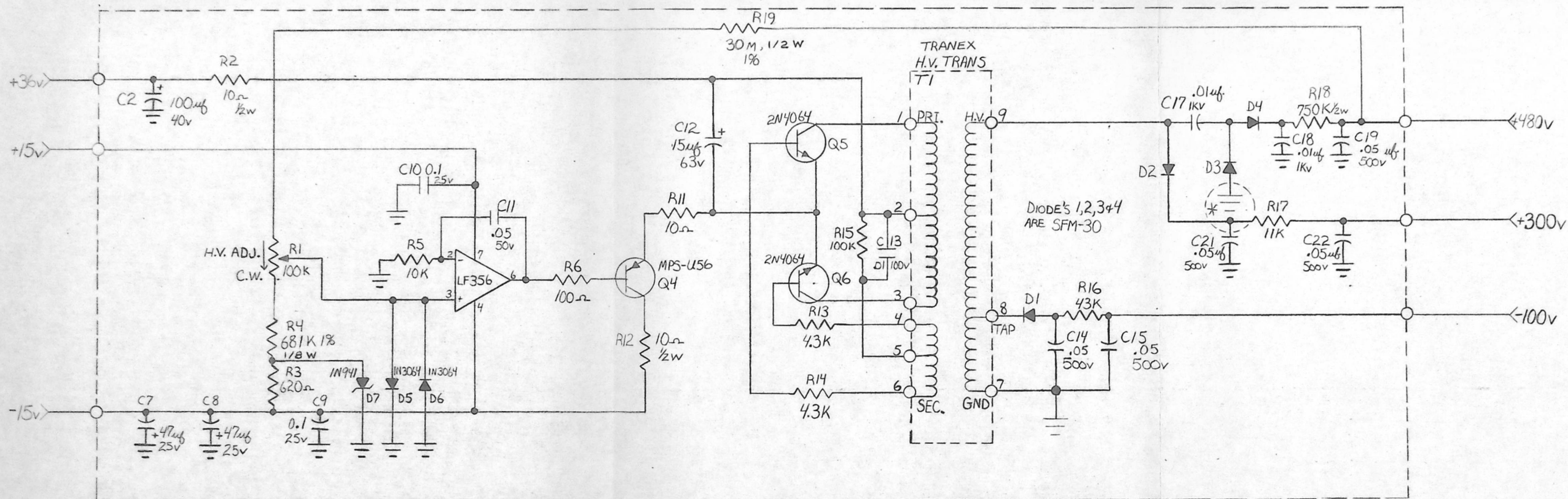
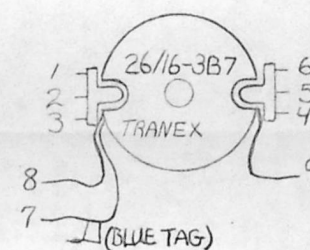
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/4 WATT, $\pm 5\%$
ALL CAPACITORS ARE IN μf
ALL OP AMPS ARE TL084CN

REV:

COMPUTER IMAGE CORPORATION			
2475 W. 2nd AVE.			
DENVER, CO. 80223			
SCALE	NONE	REVISIONS	BY DATE
DATE	6-29-81		
DRN	E.R.	CRD	
APVD			
TITLE	COLOR MIXER SYSTEM IV		NO
			CVS-138-2
			SH 1 OF 1



COMPUTER IMAGE CORPORATION		2475 W. 2nd AVE. DENVER, COLORADO 80223	
SCALE	NONE	REVISION	D
DATE	3-31-70	REVISION	E
DR'N	E. R.	BY	B.A.
AP'VD		DATE	1-6-72
TITLE		CAMERA YOE DRIVER	
NO.		SM-117	
SH 1 OF 1			

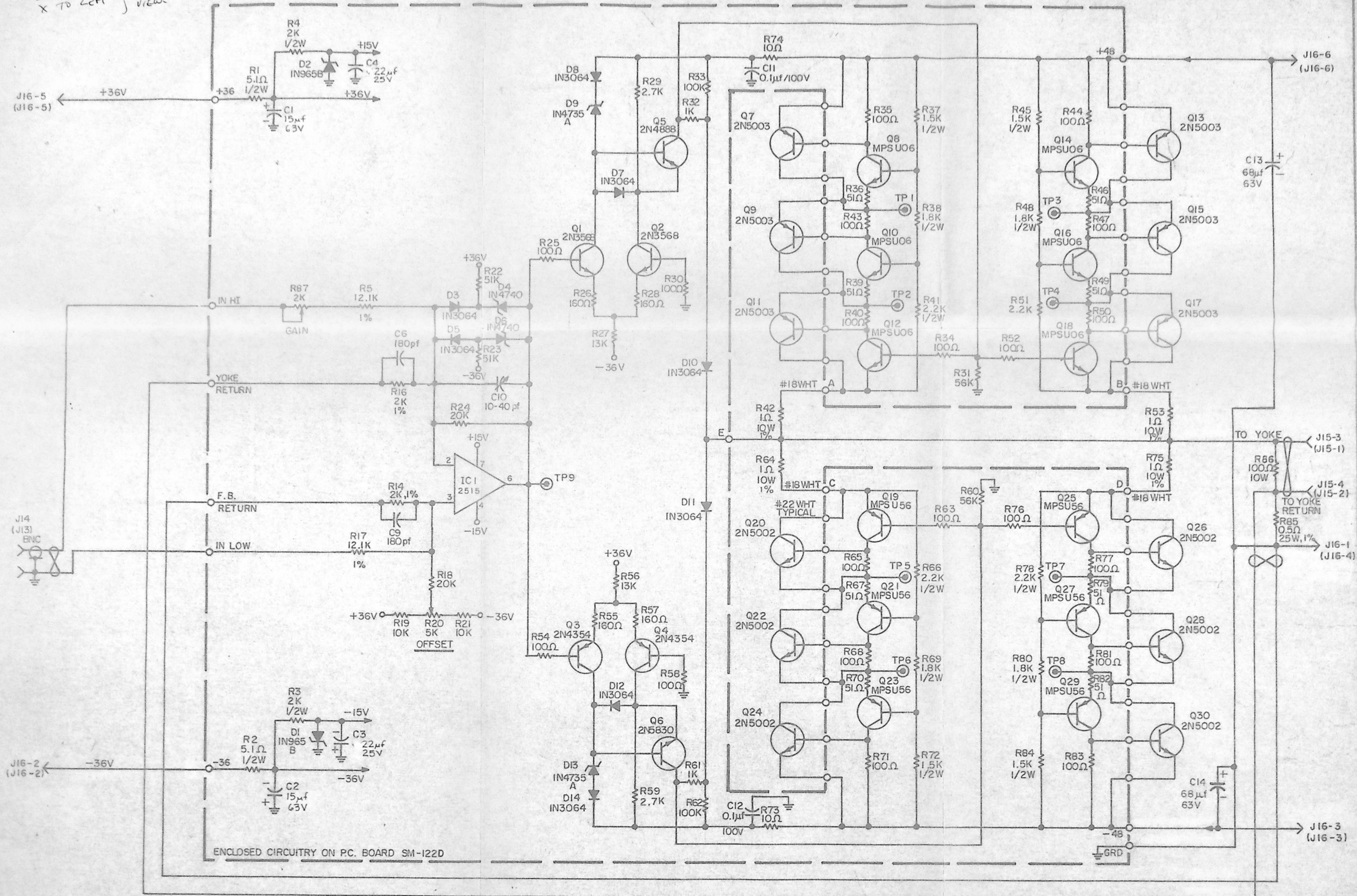


* INDICATES ETCH MODIFICATION ON SM121B BOARD

REV: A, B, C;

		2475 W. 2nd AVE. DENVER, COLORADO 80223	
SCALE	NONE	REVISIONS	BY DATE
DATE	DEC 8 80		
DR'N	SD	CK'D	
TOLERANCE			
FRACT.	± 1/32		
.XX	± .015		
.XXX	± .005		
TITLE		NO	
CAMERA HIGH VOLTAGE POWER SUPPLY		SM-121 SH 1 OF 1	

CONV
COAX
X TO LEFT } FRONT
VIEW



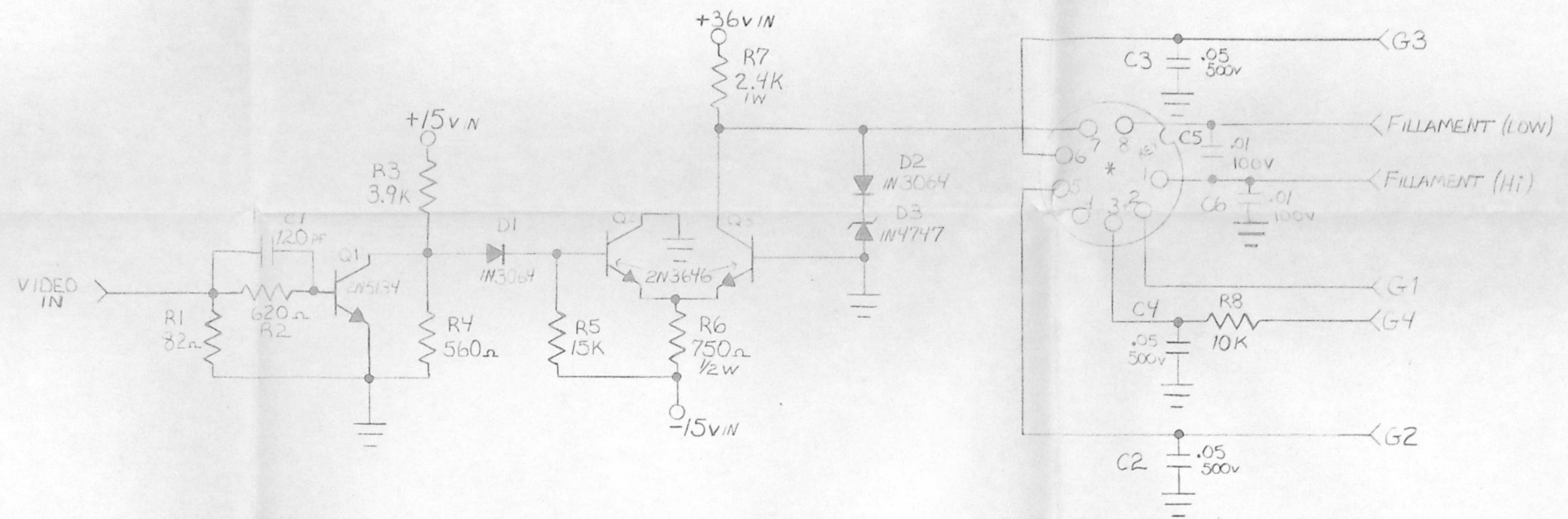
HEAT SINK
ASTRODYNE -2404-4

NOTE:
RESISTORS ARE 1/4W., UNLESS OTHERWISE SPECIFIED.

TWO COMPLETE CIRCUITS REQUIRED FOR ONE X AND Y DEFLECTION UNIT
PIN NUMBERS IN PARENTHESIS ARE FOR MON Y CHANNEL.
OTHER PIN NUMBERS ARE FOR MON X CHANNEL

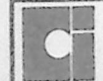
REV: A; B; C; D;

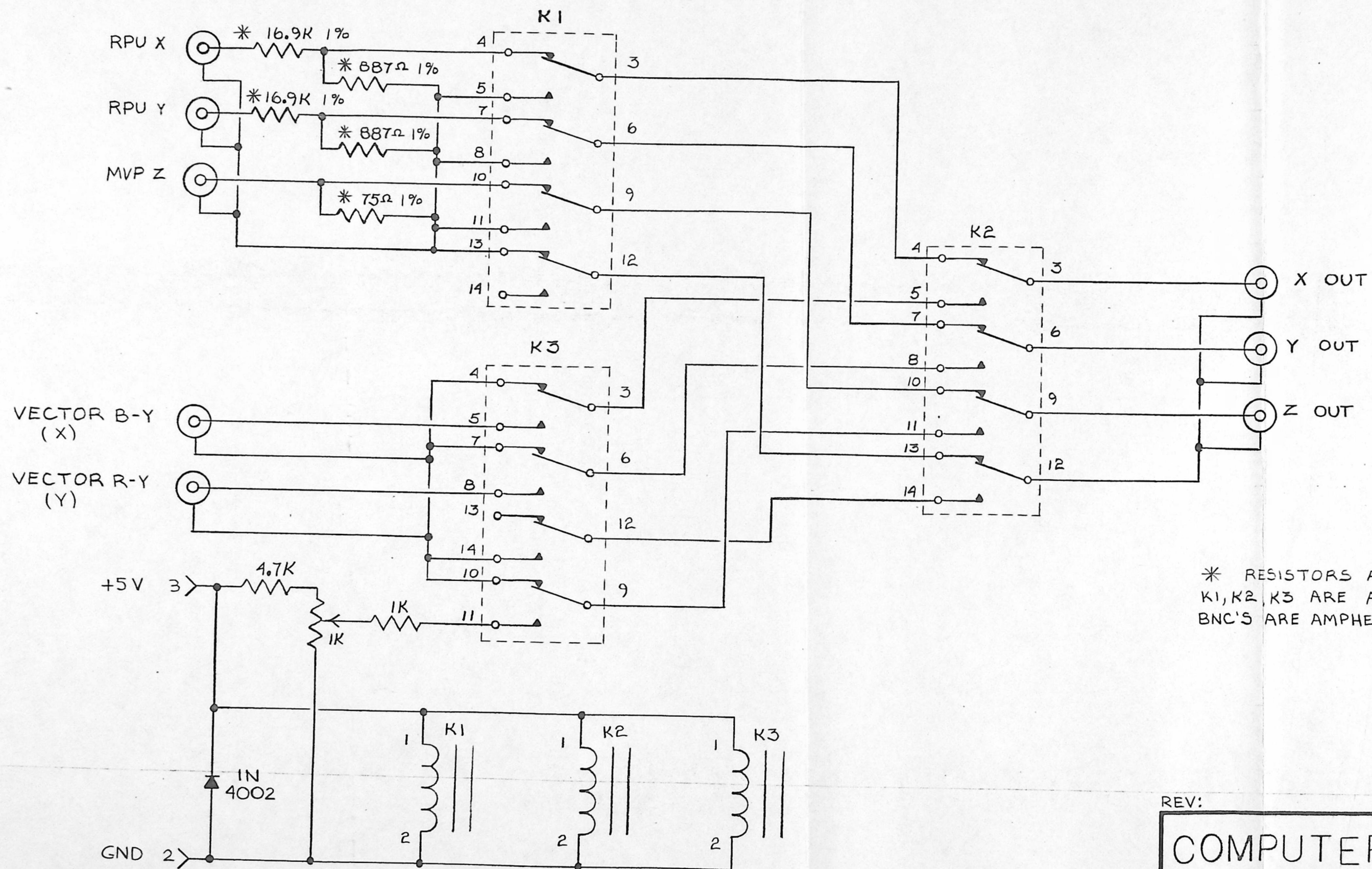
COMPUTER IMAGE CORPORATION		2475 W. 2ND. AVE. DENVER, COLORADO 80223	
SCALE NONE	REVISION	BY	DATE
DATE 9-2-71			12-16-73
DR. E. R.	CKD.	PER WCA MARKED PRINT	E. R. 4-28-82
FILE MONITOR X OR Y DEFLECTION AMPLIFIER SCHEMATIC		NO.	31 OF 1
		SM-122	



*TUBE SOCKET: CINCH 8VT

REV

 COMPUTER IMAGE CORPORATION		2475 W. 2nd AVE DENVER, COLORADO 80223	
SCALE	10X	REVISIONS	BY
DATE	12-16-80		
DR'N	SD	CK'D	
AP'VD			
TOLERANCE		TITLE	
FRACT	± 1/32	OVERLAP WHITE VIDEO AMP.	
XX	± .015	NO 5M-151	
XXX	± .005		



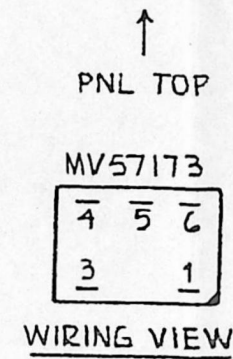
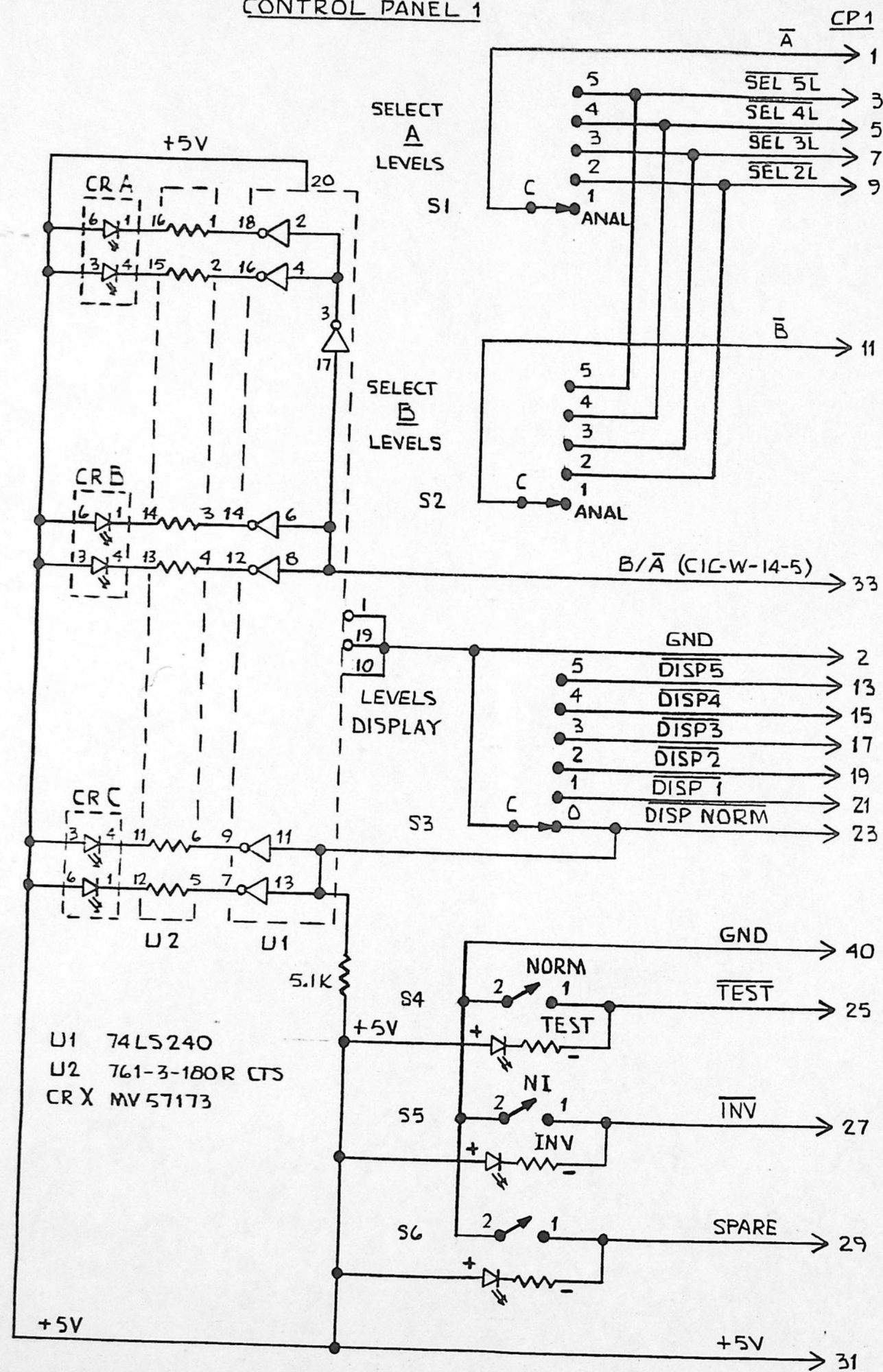
* RESISTORS ARE $\frac{1}{8}W$
 K1, K2, K3 ARE AROMAT[®] NF4-5V
 BNC'S ARE AMPHENOL 31-10

REV:

COMPUTER IMAGE

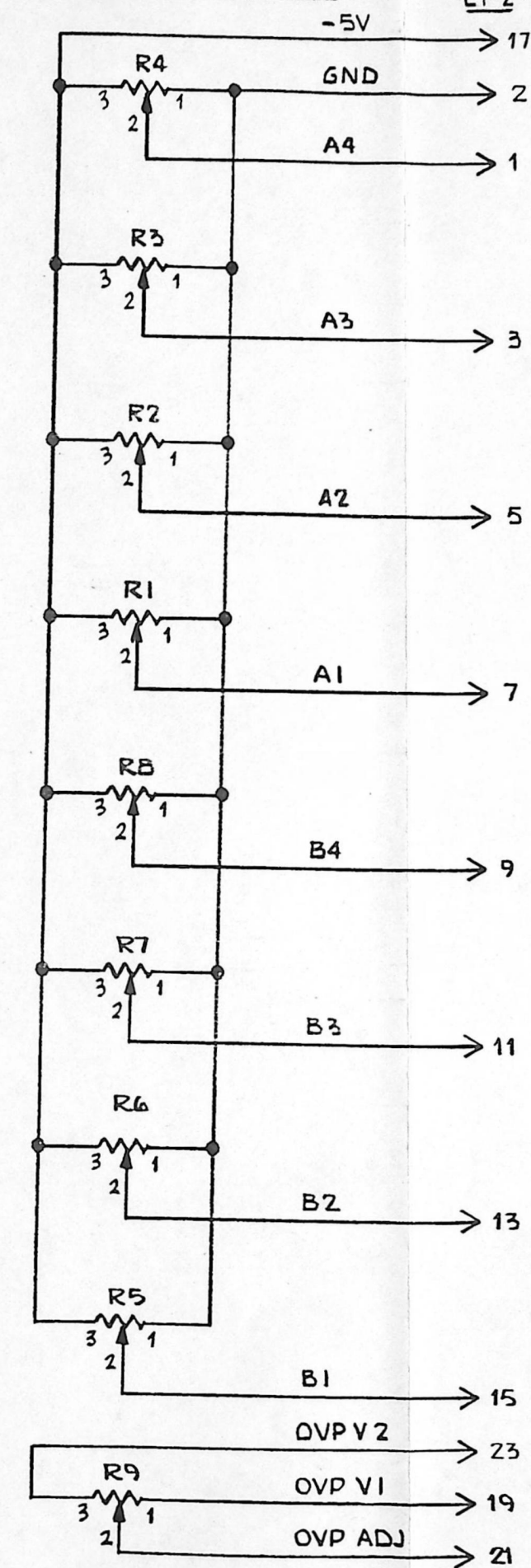
SCALE	REVISIONS	BY	DATE
DATE 1-8-82			
DRN GSK CKD			
APVD			
TITLE X-Y SCOPE SWITCHING UNIT	NO WCIC-00		

CONTROL PANEL 1



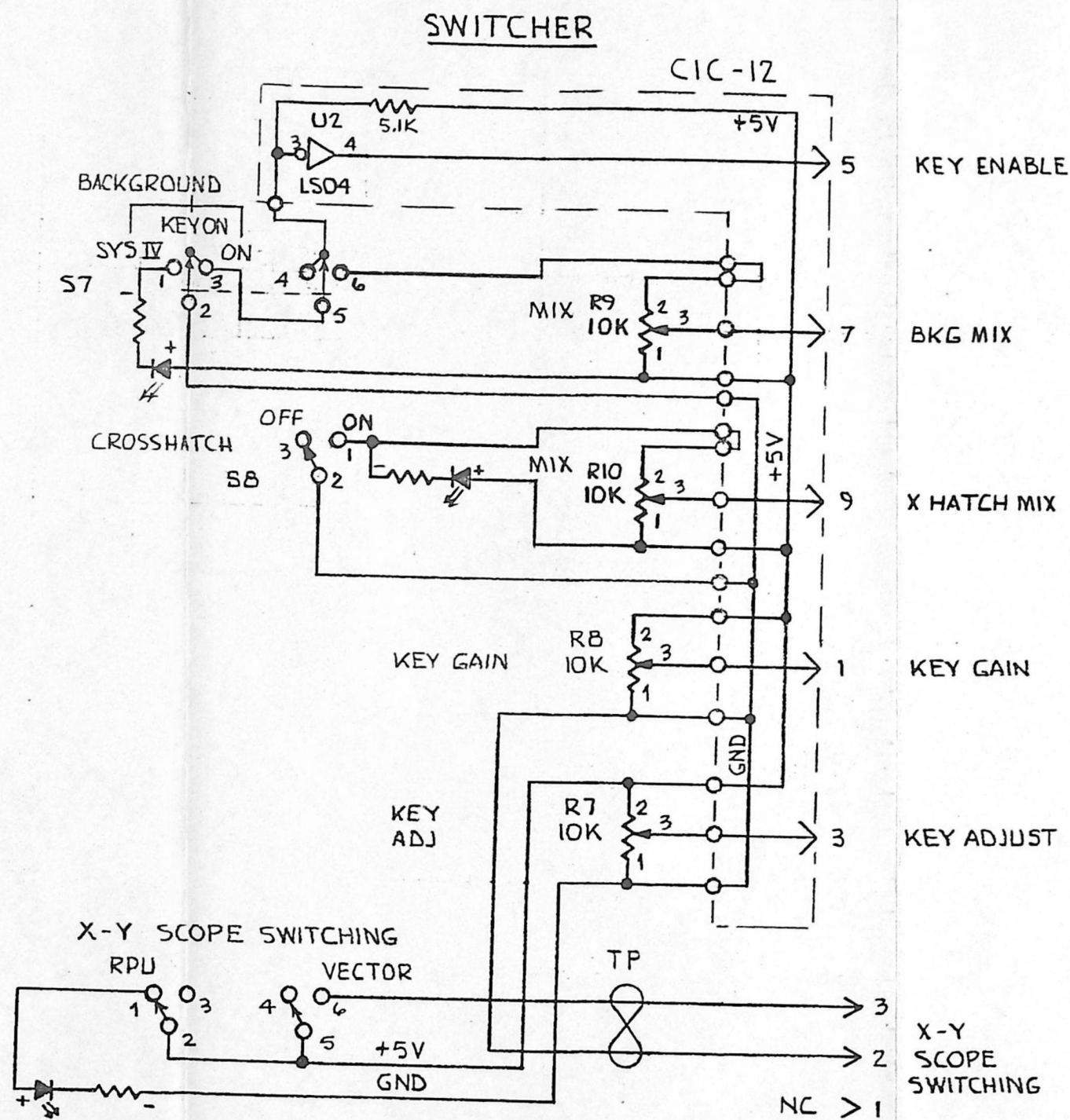
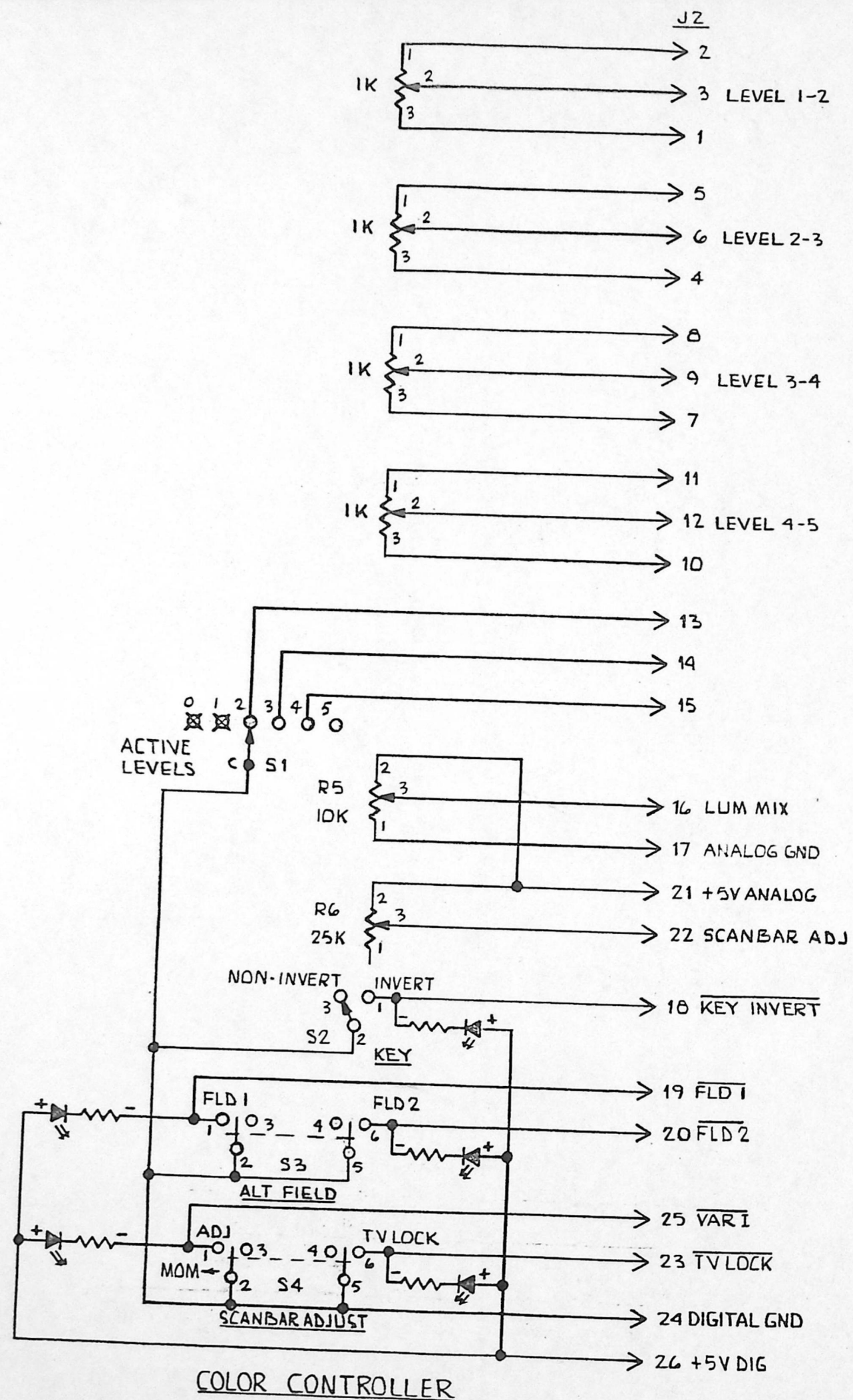
R1-R9 421-SL-10K
DUNCAN

CONTROL PANEL 2



REV: A,

COMPUTER IMAGE CORP
CONTROL PANEL 1 & 2
MONITOR VIDEO PROCESSOR
WCIC-103



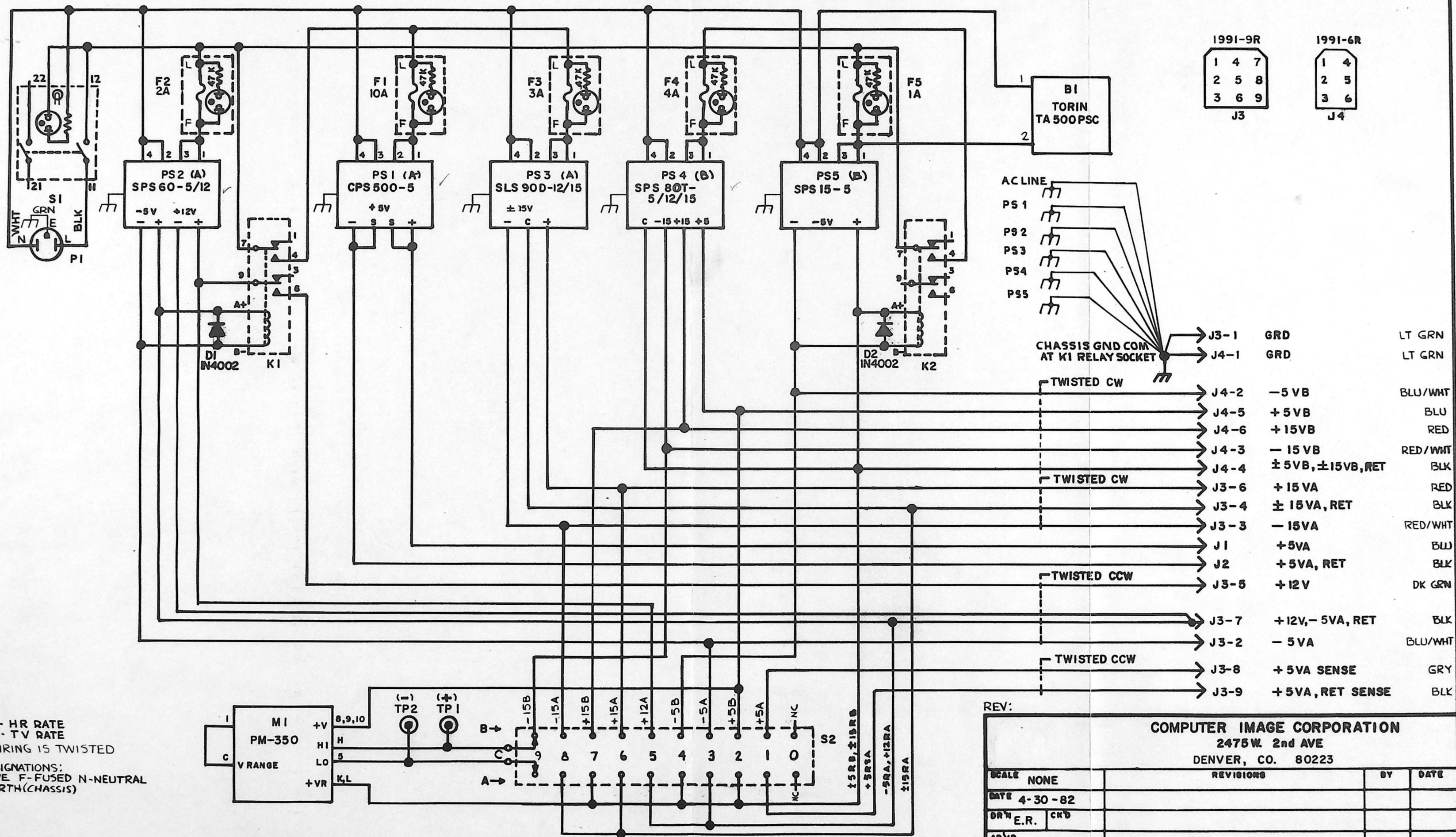
REV:A;

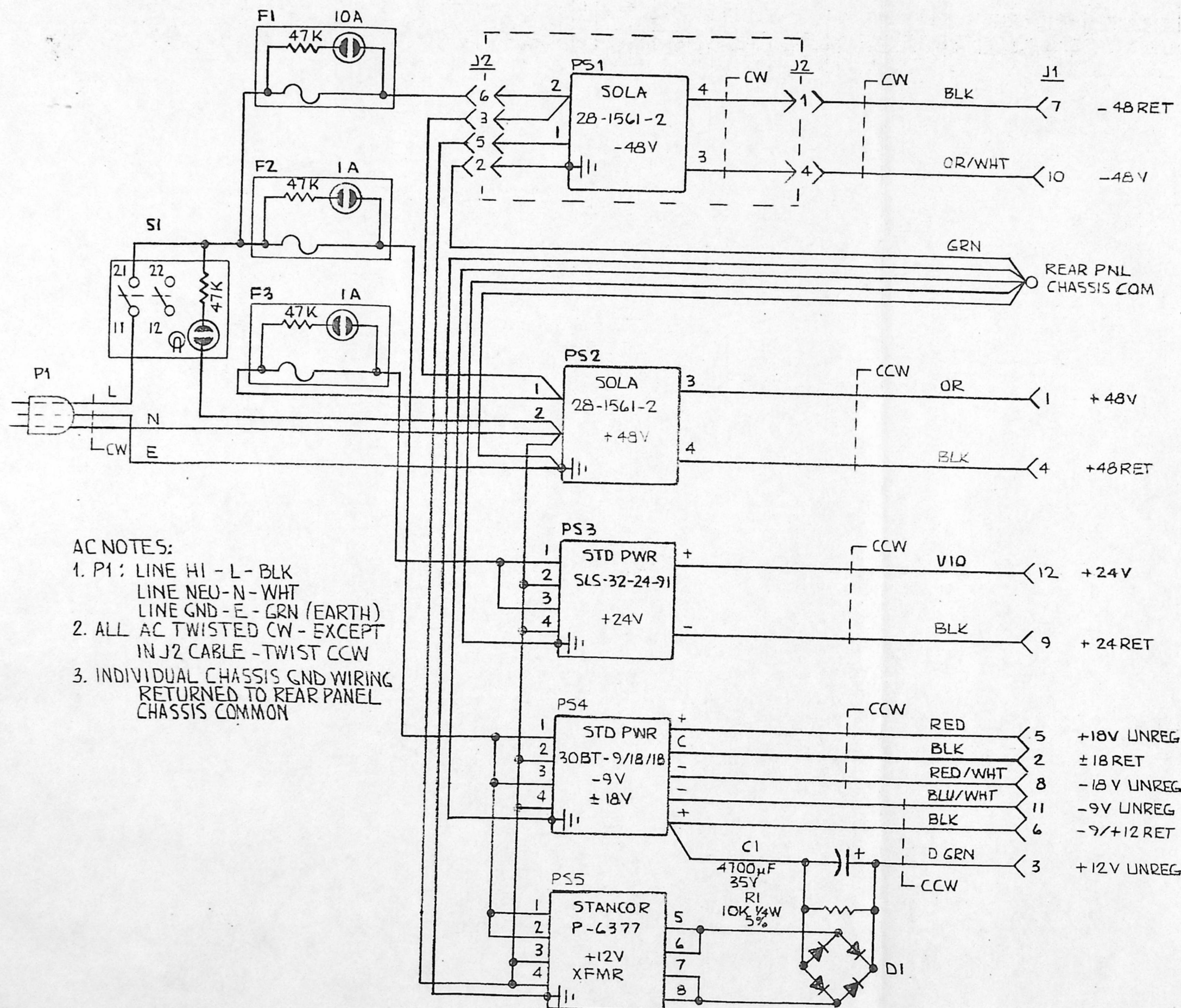
COMPUTER IMAGE CORP

VIDEO SWITCHER/COLORIZER

CONTROL PANEL

WCIC-104



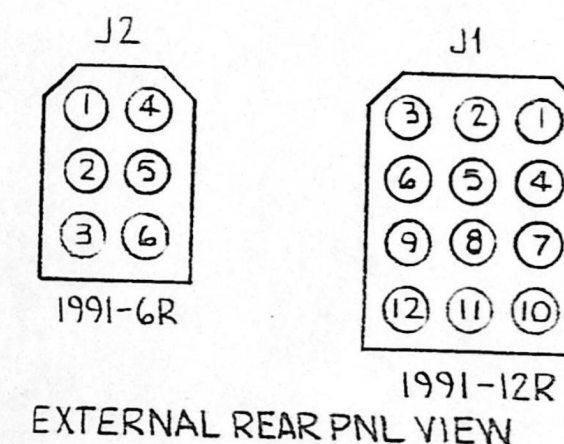


AC NOTES:

1. P1: LINE HI - L - BLK
LINE NEU - N - WHT
LINE GND - E - GRN (EARTH)
2. ALL AC TWISTED CW - EXCEPT
IN J2 CABLE - TWIST CCW
3. INDIVIDUAL CHASSIS GND WIRING
RETURNED TO REAR PANEL
CHASSIS COMMON

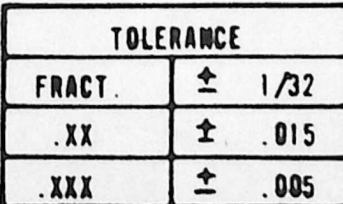
DC NOTES:

1. -48VPS WIRING TWISTED CW FOR MAGNETIC
FIELD CANCELLATION
2. ALL OTHER DC WIRING TWISTED CCW



EXTERNAL REAR PNL VIEW

REV SCHEDULE:	COMPUTER IMAGE CORP
ORIG 6/1/83 EVL	SCAN CONVERTER PWR SUPPLY
	110V/60 HZ
	SYSTEM IV
	NCIC-106-1



 COMPUTER IMAGE CORPORATION	2475 W. 2nd AVE. DENVER, COLORADO 80223			
	SCALE	REVISIONS	BY	DATE
	DATE 3/30/84			
	DR'N EVL	CK'D		
	AP'VD			
TITLE SCAN CONVERTER POWER WIRING		NO WCIC-119		

LINEAR INTEGRATED CIRCUITS

TYPES TL080 THRU TL085, TL080A THRU TL084A, TL081B, TL082B, TL084B JFET-INPUT OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 12484, FEBRUARY 1977—REVISED OCTOBER 1979

24 DEVICES COVER COMMERCIAL, INDUSTRIAL, AND MILITARY TEMPERATURE RANGES

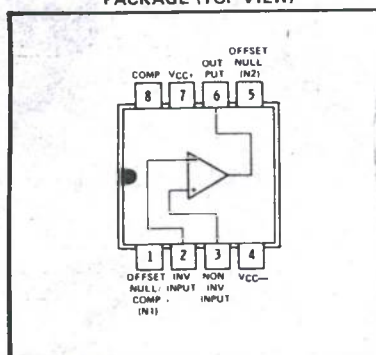
- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation (Except TL080, TL080A)
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/ μ s Typ

description

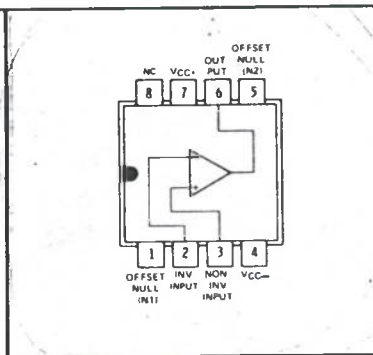
The TL081 JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL081 Family.

Device types with an "M" suffix are characterized for operation over the full military temperature range of -55°C to 125°C , those with an "I" suffix are characterized for operation from -25°C to 85°C , and those with a "C" suffix are characterized for operation from 0°C to 70°C .

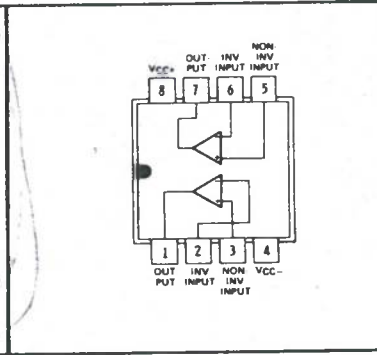
TL080, TL080A
JG OR P DUAL-IN-LINE
PACKAGE (TOP VIEW)



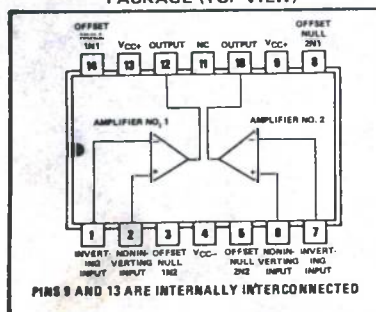
TL081, TL081A, TL081B
JG OR P DUAL-IN-LINE
PACKAGE (TOP VIEW)



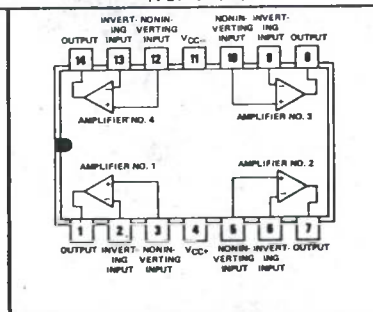
TL082, TL082A, TL082B
JG OR P DUAL-IN-LINE
PACKAGE (TOP VIEW)



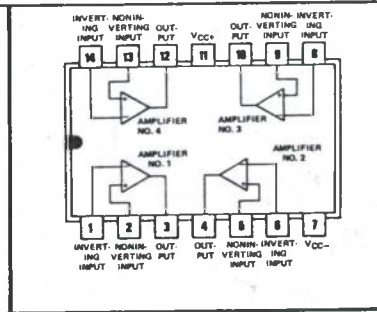
TL083, TL083A
J OR N DUAL-IN-LINE
PACKAGE (TOP VIEW)



TL084, TL084A, TL084B
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE
(TOP VIEW)



TL085
N DUAL-IN-LINE
PACKAGE (TOP VIEW)



NC—No internal connection

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TYPES TL080 THRU TL085, TL080A THRU TL084A, TL081B, TL082B, TL084B JFET-INPUT OPERATIONAL AMPLIFIERS

electrical characteristics, $V_{CC\pm} = \pm 15$ V

PARAMETER	TEST CONDITIONS†	TL08_M			TL08_I			TL08_C TL08_AC TL08_BC			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$R_S = 50 \Omega$, $T_A = 25^\circ\text{C}$	'80,'81,'82,'83,'85‡			3	6		3	6	5 15	mV
		TL084			3	9		3	6	5 15	
		TL08_A								3 6	
	$R_S = 50 \Omega$, $T_A = \text{full range}$	'81B,'82B,'84B								2 3	
		'80,'81,'82,'83,'85‡				9			9	20	
		TL084				15			9	20	
α_{VIO} Temperature coefficient of input offset voltage	$R_S = 50 \Omega$, $T_A = \text{full range}$	TL08_A								7.5	$\mu\text{V}/^\circ\text{C}$
		'81B,'82B,'84B								5	
					10		10		10		
	$T_A = 25^\circ\text{C}$	TL08_‡			5	100		5	100	5 200	
		TL08_A								5 100	
		'81B,'82B,'84B								5 100	
I_{IO} Input offset current §	$T_A = \text{full range}$	TL08_‡				20			10	5	nA
		TL08_A								3	
		'81B,'82B,'84B								3	
	$T_A = 25^\circ\text{C}$	TL08_‡			30	200		30	200	30 400	
		TL08_A								30 200	
		'81B,'82B,'84B								30 200	
I_{IB} Input bias current §	$T_A = \text{full range}$	TL08_‡				50			20	10	nA
		TL08_A								7	
		'81B,'82B,'84B								7	
	$T_A = 25^\circ\text{C}$	TL08_‡			± 11	± 12		± 11	± 12	± 10 ± 11	
		TL08_A								± 11 ± 12	
		'81B,'82B,'84B								± 11 ± 12	
V_{ICR} Common-mode input voltage range	$T_A = 25^\circ\text{C}$	$R_L = 10 \text{ k}\Omega$			24	27		24	27	24 27	V
		$R_L > 10 \text{ k}\Omega$			24			24		24	
	$T_A = \text{full range}$	$R_L > 2 \text{ k}\Omega$			20	24		20	24	20 24	
A_{VD} Large-signal differential voltage amplification	$R_L > 2 \text{ k}\Omega$, $V_O = \pm 10 \text{ V}$, $T_A = 25^\circ\text{C}$	TL08_‡			25	200		50	200	25 200	V/mV
		TL08_A								50 200	
		'81B,'82B,'84B								50 200	
	$R_L > 2 \text{ k}\Omega$, $V_O = \pm 10 \text{ V}$, $T_A = \text{full range}$	TL08_‡			15			25		15	
		TL08_A								25	
		'81B,'82B,'84B								25	
B_1 Unity-gain bandwidth	$T_A = 25^\circ\text{C}$				3		3		3		MHz
r_i Input resistance	$T_A = 25^\circ\text{C}$				10^{12}		10^{12}		10^{12}		Ω
CMRR Common-mode rejection ratio	$R_S > 10 \text{ k}\Omega$, $T_A = 25^\circ\text{C}$	TL08_‡			80	86		80	86	70 76	dB
		TL08_A								80 86	
		'81B,'82B,'84B								80 86	
k_{SVR} Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$R_S > 10 \text{ k}\Omega$, $T_A = 25^\circ\text{C}$	TL08_‡			80	86		80	86	70 76	dB
		TL08_A								80 86	
		'81B,'82B,'84B								80 86	
I_{CC} Supply current (per amplifier)	No load, No signal, $T_A = 25^\circ\text{C}$				1.4	2.8		1.4	2.8	1.4 2.8	mA
V_{01}/V_{02} Channel separation	$A_{VD} = 100$, $T_A = 25^\circ\text{C}$				120		120		120		dB

† All characteristics are specified under open-loop conditions unless otherwise noted. Full range for T_A is -55°C to 125°C for TL08_M; -25°C to 85°C for TL08_I; and 0°C to 70°C for TL08_C, TL08_AC, and TL08_BC.

‡ Types TL0851 and TL085M are not defined by this data sheet.

§ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 18. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

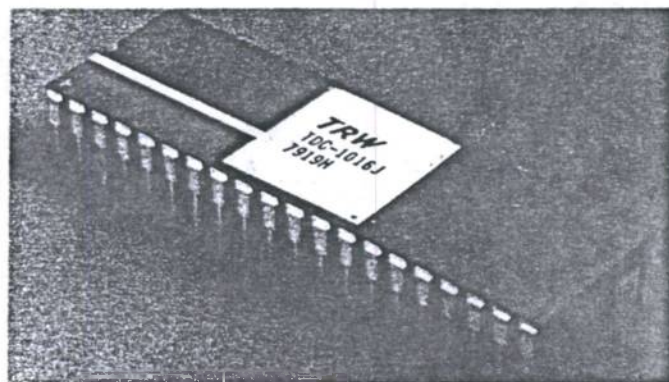
Models: **TDC1016J-8**
TDC1016J-9
TDC1016J-10

PRELIMINARY INFORMATION

The TRW TDC1016J-8/9/10 bit D/A converters are capable of converting a digital signal into an analog voltage at the rate of 20 megasamples per second (MSPS). No external input register, deglitching, or resampling is needed. No operational amplifier or buffer is required at the analog output.

All parts have 10 bits of active digital input. Three accuracy grades are offered: 8, 9, 10 bits. Simply grounding the VCC terminal causes the inputs to become ECL compatible.

The TDC1016J is patented (U.S. Patent No. 3283170) with other patents pending.

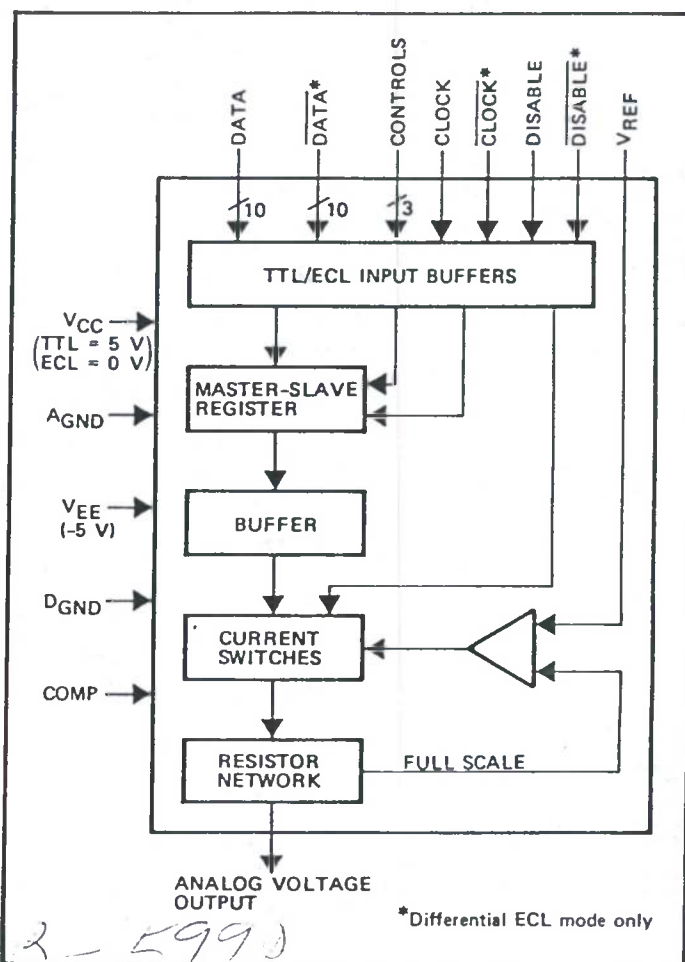


FEATURES

- 8, 9, and 10 bit accuracy
- 20 MSPS
- Voltage output
- ECL or TTL inputs (only -5.0V supply required for ECL mode)
- Single ended or differential ECL inputs
- All data registered on chip
- No deglitching circuit required
- Output disable capability
- Differential phase: 0.5°
- Differential gain: 1.0%
- Binary or two's complement input
- Zero and full scale control for easy calibration
- Data inversion control
- Monolithic, bipolar
- 40 pin ceramic DIP
- 0.6 W power dissipation

APPLICATIONS

- Video data conversion
 - 3X or 4X NTSC color
 - 3X or 4X PAL color
- Color/B&W graphics
- CRT displays
- Waveform/test signal generation



LSI D/A CONVERTERS

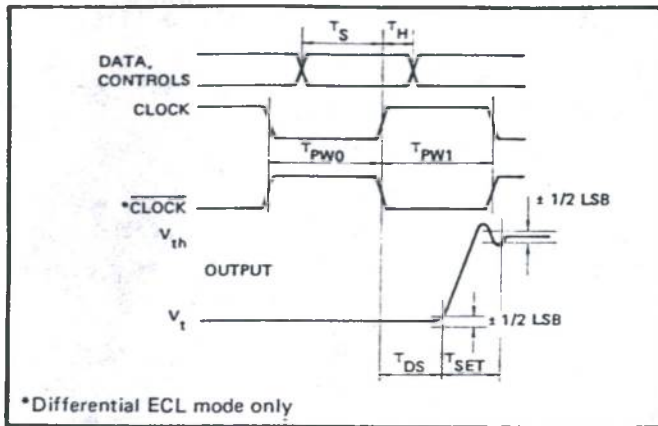


Figure 1. Timing Diagram

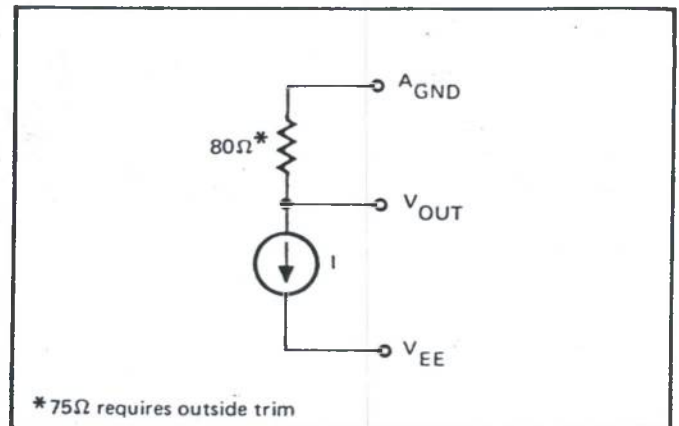


Figure 2. Analog Output Equivalent Circuit, TTL & ECL Mode

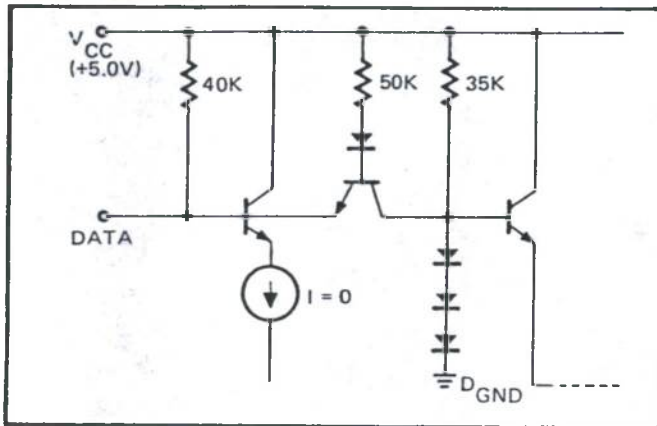


Figure 3. Digital Input Equivalent Circuit, TTL Mode

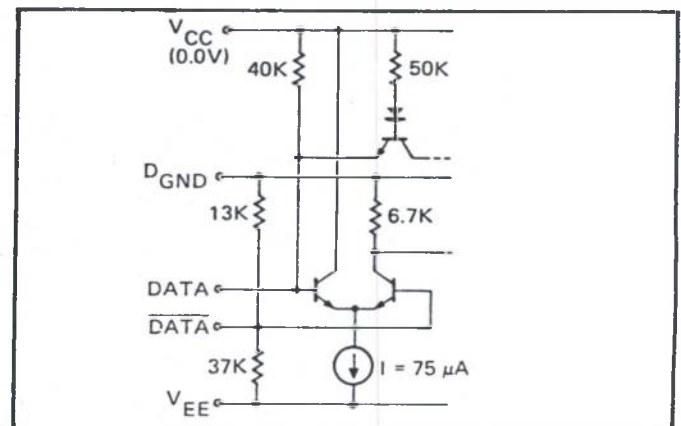


Figure 4. Digital Input Equivalent Circuit, ECL Mode

Performance characteristics, over recommended operating temperature range

PARAMETER	TEST CONDITIONS	TDC1016J-8			TDC1016J-9			TDC1016J-10			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Resolution			8			9			10		Bits
			0.39			0.19			0.10		%
Linearity error	0 to 20 MSPS conversion rate			0.20			0.10			0.05	%
Dynamic range	$Z_L > 10K\Omega$	0.8	1.0	1.2	0.8	1.0	1.2	0.8	1.0	1.2	V
	$Z_L = 75\Omega$	0.4	0.5	0.6	0.4	0.5	0.6	0.4	0.5	0.6	V
Output impedance	Resistance	75	80*	85	75	80*	85	75	80*	85	Ω
	Capacitance		5			5			5		pF
Differential phase			0.5			0.5			0.5		Deg
Differential gain			1.0			1.0			1.0		%

*75Ω requires outside trim

SPECIFICATIONS

Absolute maximum ratings (beyond which the useful life may be impaired)

Supply voltage, V_{CC}	-0.5 to +7.0 V
V_{EE}	+0.5 to -7.0 V
Input voltage, digital	-7.0 to +7.0 V
analog ground	-1.0 to +1.0 V
reference	-7.0 to +7.0 V
Output voltage	-2.0 to +2.0 V
Temperature, operating, ambient	-55 to +150°C
junction	+175°C
lead, soldering (10 seconds)	+300°C
storage	-65 to +150°C

Recommended operating conditions

PARAMETER	TTL			ECL			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} , Supply voltage	+4.75	+5.0	+5.25	-0.25	0	+0.25	V
V_{EE} , Supply voltage	-4.75	-5.0	-5.25	-4.75	-5.0	-5.25	V
V_{REF} , Reference voltage	-0.8	-1.0	-1.2	-0.8	-1.0	-1.2	V
τ_{PW1} , τ_{PW0} , pulsewidth (see Figure 1)	15			15			nsec
τ_S , Input register setup time	20			20			nsec
τ_H , Input register hold time	0			0			nsec
T_A , Operating ambient temperature range	0		+70	0		+70	°C
Compensation capacitor (between COMP and V_{EE})	1.0			1.0			μF

Electrical characteristics over recommended operating temperature range

PARAMETER	TEST CONDITIONS	TTL			ECL			UNIT
		MIN	TYP*	MAX	MIN	TYP*	MAX	
Power Supply								
I_{CC} Supply current	$V_{CC} = \text{MAX}, V_{EE} = \text{MAX}$		10	15				mA
I_{EE} Supply current	$V_{CC} = \text{MAX}, V_{EE} = \text{MAX}$		100	120		100	120	mA
Analog								
I_{REF} Reference input current	$V_{EE} = \text{MAX}, V_{REF} = -1.0 \text{ V}$		0.1			0.1		μA
V_{OFS} Full scale analog output voltage	$V_{EE} = \text{NOM}, V_{REF} = -1.0 \text{ V}, R_L > 10K\Omega$	-0.970	-1.0	-1.030	-0.970	-1.0	-1.030	V
V_{OZS} Zero scale analog output voltage	$V_{EE} = \text{NOM}, V_{REF} = -1.0 \text{ V}, R_L > 10K\Omega$			10			10	mV
Digital								
V_{IH} High level input voltage		+2.0			-1.105			V
V_{IL} Low level input voltage				+0.8			-1.475	V
I_{IH} High level input current	$V_{CC} = \text{MAX}, V_{EE} = \text{MAX}, V_I = 2.4 \text{ V}$ $V_{CC} = 0 \text{ V}, V_{EE} = \text{MAX}, V_I = -0.81 \text{ V}$			75			100	μA
I_{IL} Low level input current	$V_{CC} = \text{MAX}, V_{EE} = \text{MAX}, V_I = 0.4 \text{ V}$ $V_{CC} = 0 \text{ V}, V_{EE} = \text{MAX}, V_I = -1.85 \text{ V}$			-0.75			-0.75	mA

* $V_{CC}, V_{EE}, T_A = \text{TYP}$

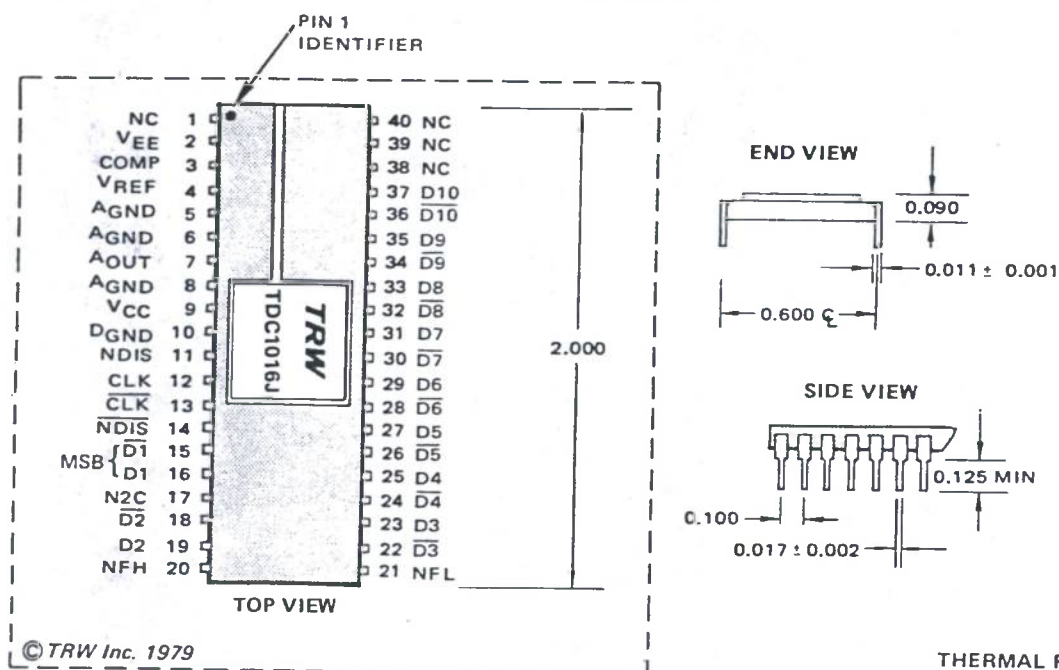
Switching characteristics over recommended operating temperature and supply ranges

PARAMETER	TEST CONDITIONS	TTL/ECL			UNIT
		MIN	TYP	MAX	
F_C Maximum conversion rate		20			MSPS
τ_{DOFF} Ladder turnoff delay	$R_L = 75\Omega$			30	nsec
τ_{DON} Ladder turnon delay	$R_L = 75\Omega$			30	nsec
τ_{DS} Data turnon delay, Figure 1	$R_L = 75\Omega$		15		nsec
τ_{SET8} Transient settling time, Figure 1, 0.20%	$R_L = 75\Omega$		20		nsec
τ_{SET9} 0.10%			25		nsec
τ_{SET10} 0.05%			30		nsec
Output transient (glitch), energy amplitude	$R_L = 75\Omega$, midscale		100		pV-sec
			20		mV

LSI D/A CONVERTERS

PACKAGE INFORMATION

TDC1016J-8/9/10



NOTES: DIMENSIONS IN INCHES.
UNUSED PINS CAN BE LEFT OPEN.

THERMAL RESISTANCE DATA

Junction to case $\theta_{JC} \approx 25^\circ \text{ C/W}$
Case to ambient θ_{CA} (Still air) $\approx 25^\circ \text{ C/W}$
Case to ambient θ_{CA} (5 ft/sec airflow) $\approx 15^\circ \text{ C/W}$

INPUT CODING

DISABLE NDIS	TWO'S COMPLEMENT N2C	FORCE HIGH NFH	FORCE LOW NFL	INPUT		OUTPUT	FUNCTIONAL DESCRIPTION
				MSB	LSB		
1	1	1	1	1111111111	0000000000	0.0V -1.0V	Default controls
0	x	x	x	xxxxxxxxxx		0.0V	Output disable
1	x x	0 1	1 0	xxxxxxxxxx xxxxxxxxxx		0.0V -1.0V	Force high Force low
1	1	0	0	1111111111	0000000000	-1.0V 0.0V	Inverted
1	0	1	1	0111111111	1000000000	0.0V -1.0V	Two's complement
1	0	0	0	0111111111	1000000000	-1.0V 0.0V	Two's complement inverted

x - Don't care

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TRW LSI PRODUCTS

2525 E. EL SEGUNDO BLVD., EL SEGUNDO, CA 90245
(213) 535-1831

LM125/LM325/LM325A, LM126/LM326 Voltage Regulators

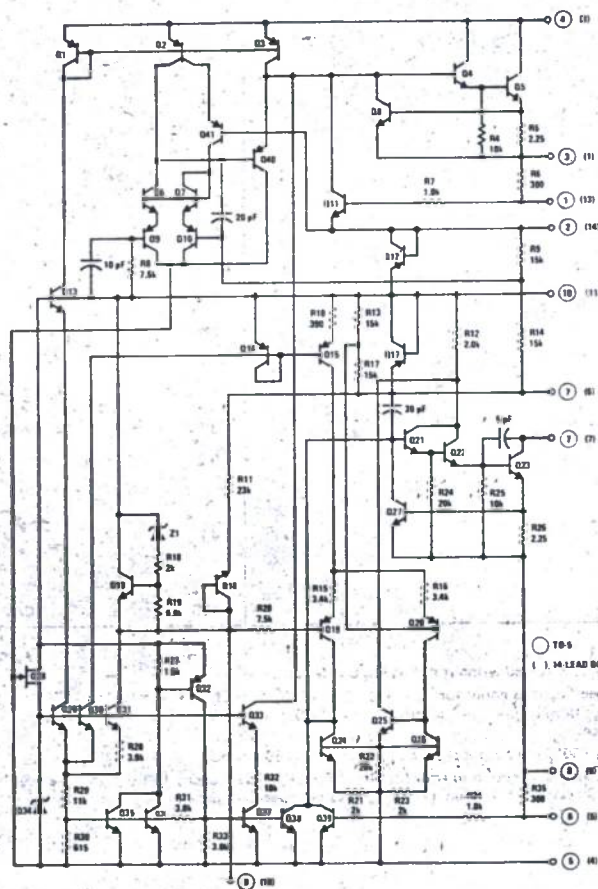
General Description

These are dual polarity tracking regulators designed to provide balanced positive and negative output voltages at current up to 100 mA, the devices are set for ± 15 V, ± 12 V and ± 5 , -12 V outputs respectively. Input voltages up to ± 30 V can be used and there is provision for adjustable current limiting. These devices are available in three package types to accommodate various power requirements and temperature ranges.

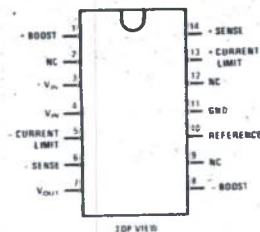
Features

- ± 15 V and ± 12 V tracking outputs
- Output currents to 100 mA
- Output voltages balanced to within 1% (LM125, LM126, LM325A)
- Line and load regulation of 0.06%
- Internal thermal overload protection
- Standby current drain of 3 mA
- Externally adjustable current limit
- Internal current limit

Schematic and Connection Diagrams

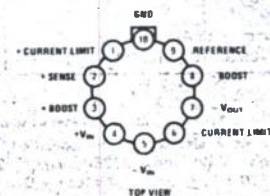


Dual-In-Line Package



Order Number LM325AN, LM325N,
or LM326N
See NS Package N14A

Metal Can Package



Order Number LM125H,
LM325H, LM126H or
LM326H
See NS Package H10C

Absolute Maximum Ratings

Input Voltage	±30V
Forced V_O^+ (min) (Note 1)	-0.5V
Forced V_O^- (max) (Note 1)	+0.5V
Power Dissipation (Note 2)	P_{MAX}
Output Short-Circuit Duration (Note 3)	Indefinite

Operating Conditions

Operating Temperature Range	
LM125	-55°C to +125°C
LM325, LM325A	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics LM125/LM325/LM325A (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_J = 25^\circ\text{C}$				
LM125, LM325A		14.8	15	15.2	V
LM325		14.5	15	15.5	V
Input-Output Differential		2.0			V
Line Regulation	$V_{IN} = 18\text{V to } 30\text{V}$, $I_L = 20\text{ mA}$, $T_J = 25^\circ\text{C}$		2.0	10	mV
Line Regulation Over Temperature Range	$V_{IN} = 18\text{V to } 30\text{V}$, $I_L = 20\text{ mA}$		2.0	20	mV
Load Regulation	$I_L = 0\text{ to } 50\text{ mA}$, $V_{IN} = \pm 30\text{V}$, $T_J = 25^\circ\text{C}$		3.0	10	mV
V_O^+			5.0	10	mV
V_O^-					
Load Regulation Over Temperature Range	$I_L = 0\text{ to } 50\text{ mA}$, $V_{IN} = \pm 30\text{V}$				
V_O^+			4.0	20	mV
V_O^-			7.0	20	mV
Output Voltage Balance	$T_J = 25^\circ\text{C}$				
LM125/LM325A				±150	mV
LM325				±300	mV
Output Voltage Over Temperature Range	$P \leq P_{MAX}$, $0 \leq I_O \leq 50\text{ mA}$, $18\text{V} \leq V_{IN} \leq 30$	14.65		15.35	V
LM125/LM325A		14.27		15.73	V
LM325					
Temperature Stability of V_O			±0.3		%
Short Circuit Current Limit	$T_J = 25^\circ\text{C}$		260		mA
Output Noise Voltage	$T_J = 25^\circ\text{C}$, BW = 100 - 10 kHz		150		μVrms
Positive Standby Current	$T_J = 25^\circ\text{C}$		1.75	3.0	mA
Negative Standby Current	$T_J = 25^\circ\text{C}$		3.1	5.0	mA
Long Term Stability			0.2		%/kHr
Thermal Resistance Junction to Case (Note 4)					
LM125H, LM325H			45		°C/W
Junction to Ambient					
LM325AN, LM325N			150		°C/W

Note 1: That voltage to which the output may be forced without damage to the device.

Note 2: Unless otherwise specified, these specifications apply for $T_J = -55^\circ\text{C}$ to $+150^\circ\text{C}$ on LM125, $T_J = 0^\circ\text{C}$ to $+125^\circ\text{C}$ on LM325 and LM325A, $V_{IN} = \pm 20\text{V}$, $I_L = 0\text{ mA}$, $I_{MAX} = 100\text{ mA}$, $P_{MAX} = 2.0\text{W}$ for the TO-5 H package. $I_{MAX} = 100\text{ mA}$, $P_{MAX} = 1.0\text{W}$ for the DIP N package.

Note 3: If the junction temperature exceeds 150°C the output short circuit duration is 60 seconds.

Note 4: Without a heat sink, the thermal resistance junction to ambient of the TO-5 Package is about 150°C/W . With a heat sink, the effective thermal resistance can only approach the junction to case values specified, depending on the efficiency of the sink.



MOTOROLA

Semiconductors

BOX 20812, PHOENIX, ARIZONA 85036

MC1545 MC1445

GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

... designed for use as a general-purpose gated wideband-amplifier, video switch, sense amplifier, multiplexer, modulator, FSK circuit, limiter, AGC circuit, or pulse amplifier. See Application Notes AN475 and AN491 for design details.

- Large Bandwidth; 75 MHz typical
- Channel-Select Time of 20 ns typical
- Differential Inputs and Differential Output

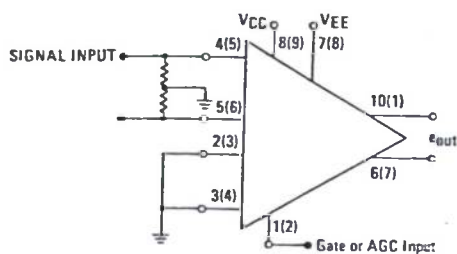
GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

MONOLITHIC SILICON
EPITAXIAL PASSIVATED

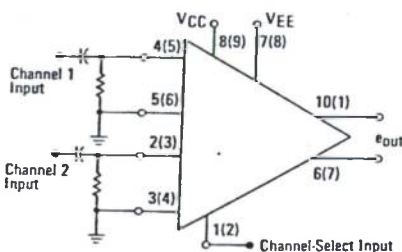
OCTOBER 1971 - DS 9125 R1

TYPICAL APPLICATIONS

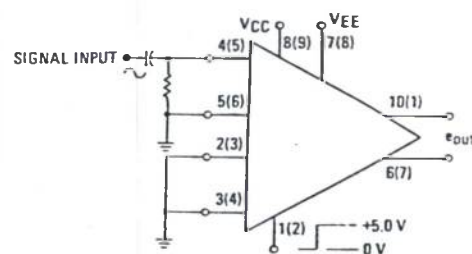
VIDEO SWITCH OR DIFFERENTIAL AMPLIFIER WITH AGC



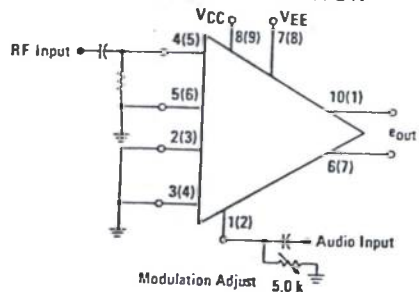
MULTIPLEX OR FSK



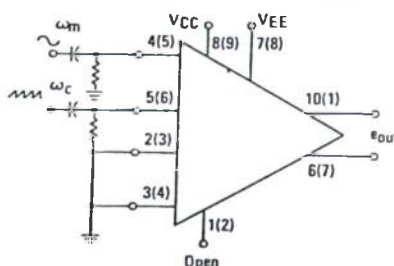
ANALOG SWITCH



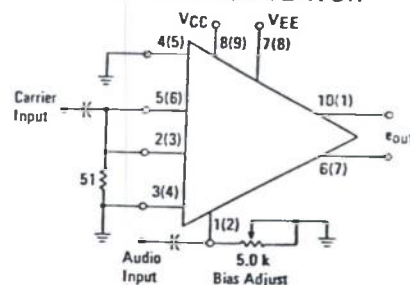
AMPLITUDE MODULATOR



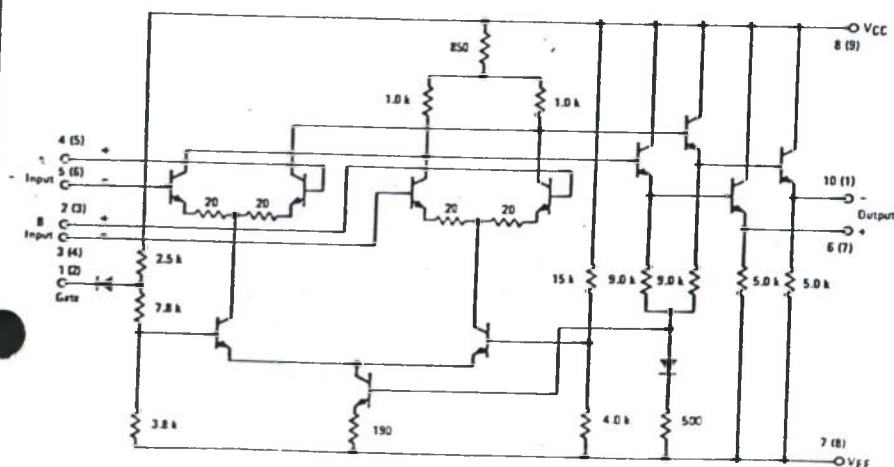
PULSE-WIDTH MODULATOR



BALANCED MODULATOR



CIRCUIT SCHEMATIC



Number in parenthesis denotes pin for F and L packages, number at left in each case denotes corresponding pin for G package.

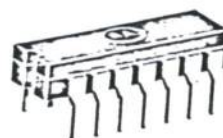


F SUFFIX
CERAMIC PACKAGE
CASE 607
TO-86

G SUFFIX
METAL PACKAGE
CASE 602A



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	+12	V _{dc}
	V _{EE}	-12	V _{dc}
Differential Input Signal	V _{ID}	±5.0	Volts
Load Current	I _L	25	mA
Power Dissipation (Package Limitation)	P _D		
Flat Package Derate above T _A = +25°C		500 3.3	mW mW/°C
Ceramic Dual In-Line Package Derate above T _A = +25°C		625 5.0	mW mW/°C
Metal Can Derate above T _A = +25°C		680 4.6	mW mW/°C
Operating Temperature Range	MC1445 MC1545 T _A	0 to +75 -55 to +125	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V_{dc}, V_{EE} = 5.0 V_{dc}, at T_A = +25°C, specifications apply to both input channels unless otherwise noted)

Characteristic	Fig. No.	Symbol*	Min	Typ	Max	Unit
Single-Ended Voltage Gain	MC1445 MC1545 1, 12	A _{vs}	16 16	19 18	22 20	dB
Bandwidth	MC1445 MC1545 1, 12	BW	— 50	75 75	—	MHz
Input Impedance (f = 50 kHz)	MC1445 MC1545 5, 14	Z _{is}	3.0 4.0	10 10	—	k ohms
Output Impedance (f = 50 kHz)	6, 15	Z _{os}	—	25	—	Ohms
Output Voltage Swing (R _L = 1.0 k ohm, f = 50 kHz)	4, 13	V _{OD}	1.5	2.5	—	V _{p-p}
Input Bias Current (I _{IB} = (I ₁ + I ₂)/2)	MC1445 MC1545 16	I _{IB}	—	15 15	30 25	μA _{dc}
Input Offset Current	16	I _{IO}	—	2.0	—	μA _{dc}
Input Offset Voltage	MC1445 MC1545 17	V _{IO}	—	— 1.0	7.5 5.0	mV _{dc}
Quiescent Output dc Level	17	V _O	—	0.2	—	V _{dc}
Output dc Level Change (Gate Voltage Change: +5.0 V to 0 V)	17	ΔV _O	—	15	—	mV
Common-Mode Rejection Ratio (f = 50 kHz)	9, 18	CMRR	—	85	—	dB
Input Common-Mode Voltage Swing	18	V _{ICR}	—	±2.5	—	V _p
Gate Characteristics						
Gate Voltage Low (See Note 1)	MC1445 MC1545 8	V _{GOL}	0.20 0.45	0.40 0.70	— —	V _{dc}
Gate Voltage High (See Note 2)	MC1445 MC1545	V _{GOH}	— —	1.3 1.5	3.0 2.2	
Gate Current Low (Gate Voltage = 0 V)	MC1445 MC1545 18	I _{GOL}	— —	— —	4.0 2.5	mA
Gate Current High (Gate Voltage = +5.0 V)	MC1445 MC1545 18	I _{GOH}	— —	— —	4.0 2.0	μA
Step Response (e _{in} = 20 mV)	MC1445 MC1545 19	t _{PLH} t _{PHL} t _r t _f	— — — —	6.5 6.5 6.3 6.5 6.5	— 10 — 10 10	ns
Wideband Input Noise (5.0 Hz - 10 MHz, R _S = 50 ohms)	10, 20	V _{N(in)}	—	25	—	μV(rms)
DC Power Dissipation	MC1445 MC1545 11, 20	P _D	— —	70 70	150 110	mW

Note 1 V_{GOL} is the gate voltage which results in channel A gain of unity or less and channel B gain of 16 dB or greater.
 Note 2 V_{GOH} is the gate voltage which results in channel B gain of unity or less and channel A gain of 16 dB or greater.
 * Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

FIGURE 13 – OUTPUT VOLTAGE SWING TEST CIRCUIT

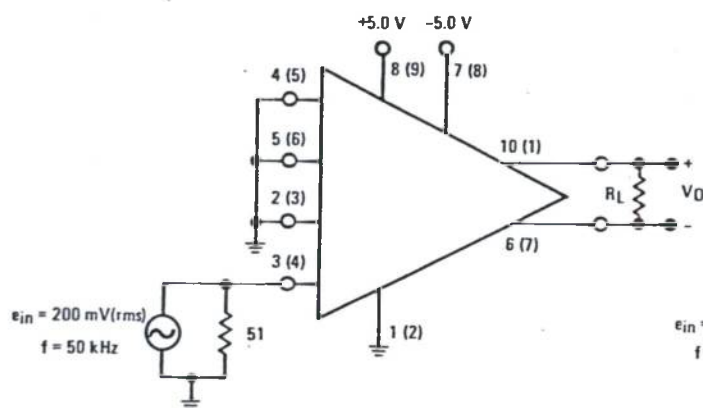


FIGURE 14 – INPUT IMPEDANCE TEST CIRCUIT

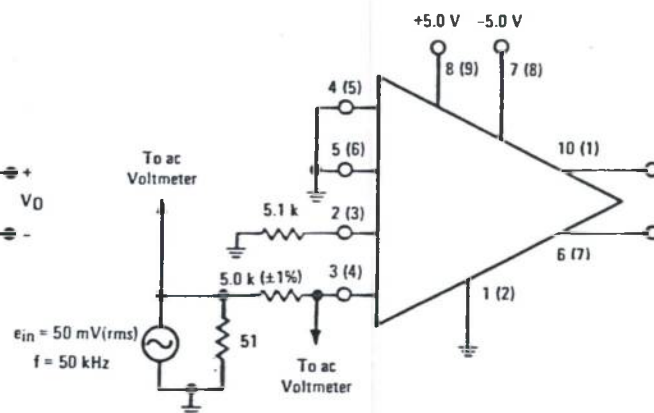


FIGURE 15 – OUTPUT IMPEDANCE TEST CIRCUIT

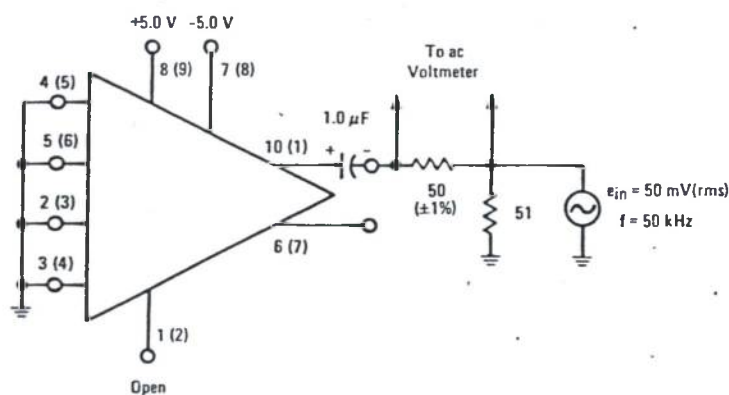


FIGURE 16 – INPUT BIAS CURRENT AND INPUT OFFSET CURRENT TEST CIRCUIT

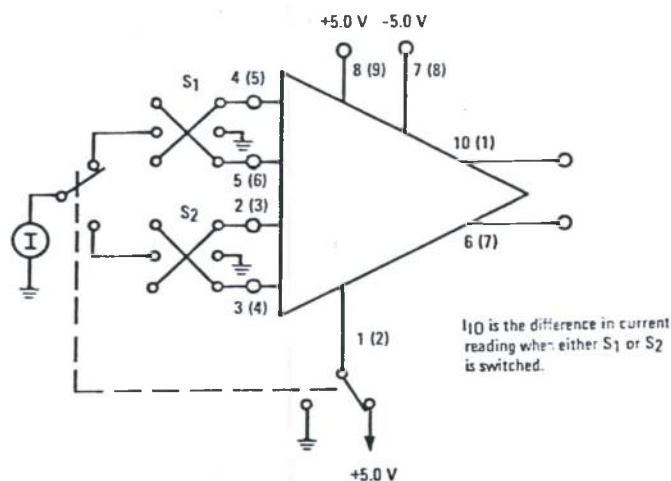


FIGURE 17 – INPUT OFFSET VOLTAGE AND QUIESCENT OUTPUT LEVEL TEST CIRCUIT

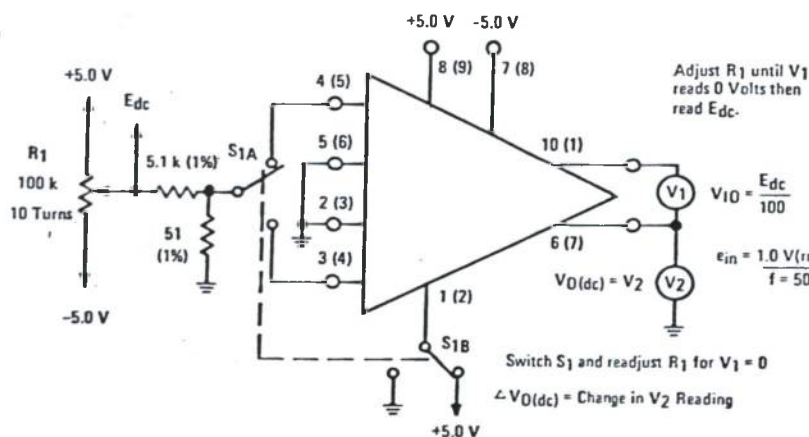
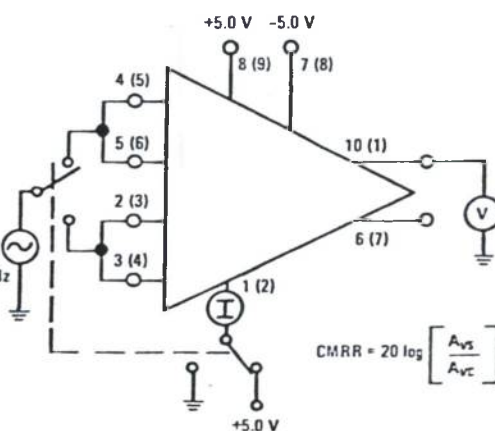


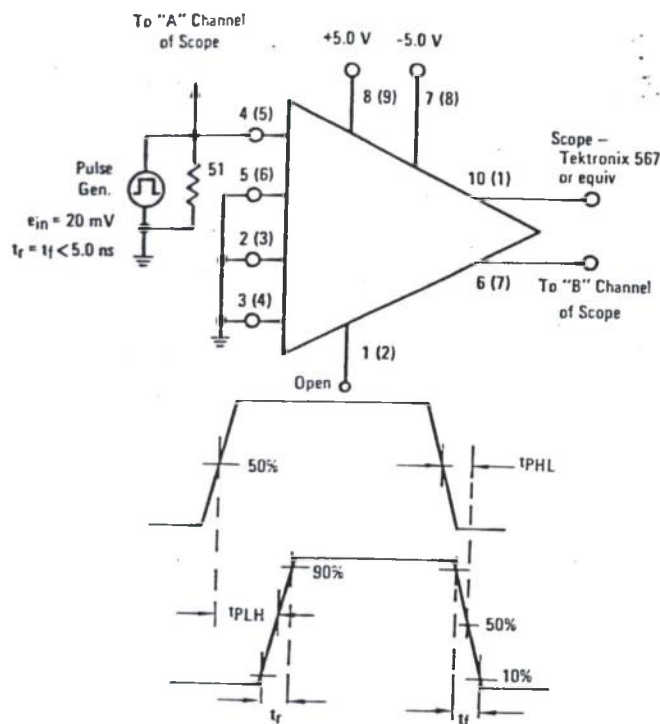
FIGURE 18 – GATE CURRENT (HIGH AND LOW), COMMON-MODE REJECTION AND COMMON-MODE INPUT RANGE TEST CIRCUIT



Number in parenthesis denotes pin for F and L packages, number at left in each case denotes corresponding pin for G package.



FIGURE 19 - PROPAGATION DELAY AND RISE AND FALL TIMES TEST CIRCUIT



Number in parenthesis denotes pin for F and L packages,
number at left in each case denotes corresponding pin for G package.

FIGURE 20 - POWER DISSIPATION AND WIDEBAND INPUT NOISE TEST CIRCUIT

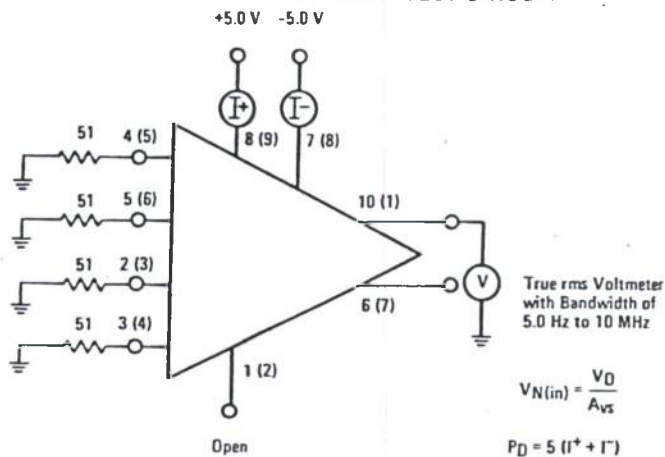
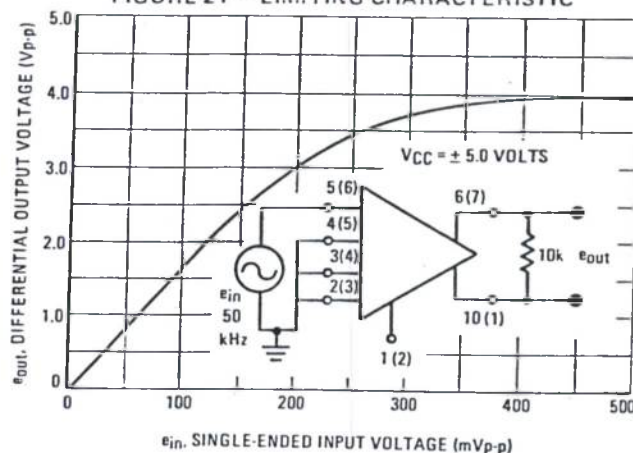
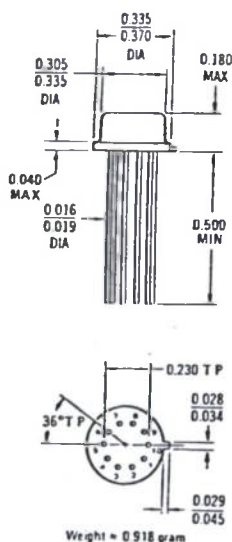


FIGURE 21 - LIMITING CHARACTERISTIC



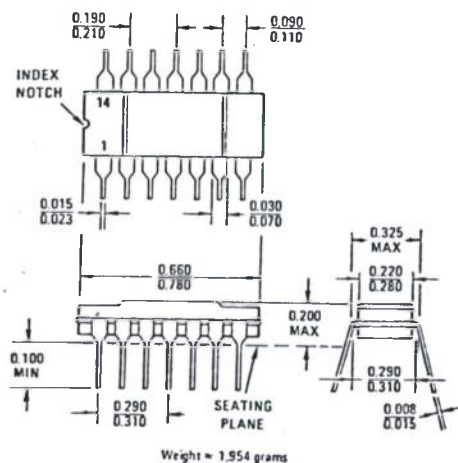
G SUFFIX
METAL PACKAGE
CASE 602A



Pin 7 connected to case

CASE OUTLINES

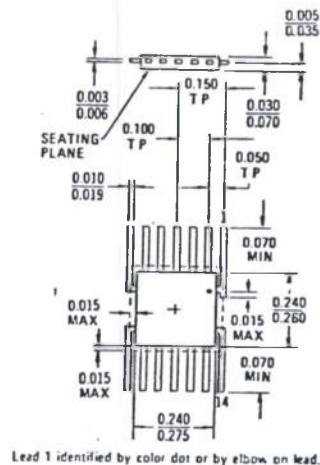
L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



All JEDEC TO-116 dimensions and notes apply.

- ① This dimension is measured from the lead centers at the seating plane.
- ② Orientation will be indicated either by mechanical index point or notch in pin 1 as shown.

F SUFFIX
CERAMIC PACKAGE
CASE 607
TO-86



All JEDEC dimensions and notes apply

Weight ≈ 0.218 Gram

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and

is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.



MOTOROLA Semiconductor Products Inc.

BOX 20912 • PHOENIX, ARIZONA 85036 • A SUBSIDIARY OF MOTOROLA INC.



OP-15

PRECISION JFET INPUT OPERATIONAL AMPLIFIER

LOW SUPPLY CURRENT

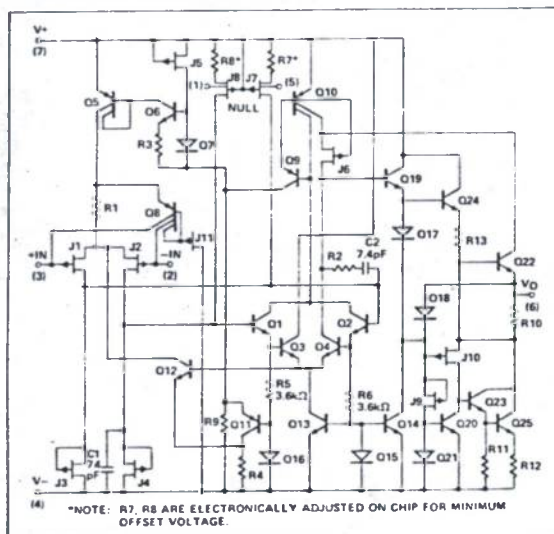
FEATURES

- High Slew Rate $17\text{V}/\mu\text{s}$
- Fast Settling to $\pm 0.1\%$ 900ns
- Low Input Offset Voltage $500\mu\text{V}$ Maximum
- Low Input Offset Voltage Drift $2.0\mu\text{V}/^\circ\text{C}$
- 156 Speed with 155 Dissipation (80MW Typical)
- Wide Bandwidth 6MHz
- Minimum Slew Rate Guaranteed on All Models
- Temperature Compensated Input Bias Currents*
- Guaranteed Input Bias Current
@ 125°C 9nA Maximum
- Bias Current Specified WARMED UP Over Temperature
- Internal Compensation
- Low Input Noise Current $0.01\text{pA}/\sqrt{\text{Hz}}$
- High Common Mode Rejection Ratio 100dB
- Models With MIL-STD-883 Class B Processing Available From Stock

GENERAL DESCRIPTION

The OP-15 provides an excellent combination of high-speed and low input offset voltage. In addition, the OP-15 offers the speed of the 156A op amp with 155A dissipation. To further enhance the excellent input parameters, the OP-15 uses bias current compensation to maintain low input bias current at elevated temperatures.

SIMPLIFIED SCHEMATIC DIAGRAM



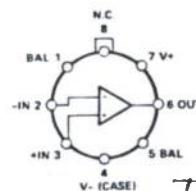
The OP-15 was designed to provide real precision performance along with its high speed. For example, the $500\mu\text{V}$ offset voltage yields less than 1/2 LSB error in a 12-bit, 5V DAC. Although the OP-15 can be nulled, the design objective was to provide low offset voltage and drift WITHOUT NULLING. Systems become MORE COST EFFECTIVE as the number of error correcting "knobs" decrease. PMI achieves this performance by use of an improved BIFET process coupled with on-chip zener-zap offset trimming.

Most high-speed monolithic op amps give settling time specifications to 0.01% error band, and so does PMI. Since 0.01% of 10V is 1mV, it is surprising that these same op amps have offset voltage errors in the 0.02% to 0.3% range. A large number of applications are in the 0.05% to 0.1% range, and PMI also gives specs for these error bands in its settling times. The fact that $500\mu\text{V}$ is only 0.005% of 10V is why PMI specifies settling time to a true 0.01% error band.

The combination of low input offset voltage of $500\mu\text{V}$ Maximum, slew rate of $17\text{V}/\mu\text{s}$, and settling time of 900ns — to 0.1% — makes the OP-15 a true precision, high-speed op amp. The additional features of low supply current coupled with an input bias current of 9nA at 125°C ambient (not junction) temperature makes the OP-15 useful in a wide range of applications.

Applications include high-speed amplifiers for current output DACs, active filters, sample-and-hold buffers, and photocol amplifiers. For additional precision JFET op amps, see the OP-16, OP-17, and OP-215 (dual OP-15) data sheets.

PIN CONNECTIONS & ORDERING INFORMATION



ORDER: OP-15AJ
OP-15BJ
OP-15CJ
OP-15EJ
OP-15FJ
OP-15GJ

TO-99 (J-Suffix)

Military Temperature Range Devices
With MIL-STD-883* Class B Processing

ORDER: OP15AJ/883
OP15BJ/883
OP15CJ/883

*Current revision in effect

OP-15

JFET INPUT AMPLIFIER SUPPLY CURRENT

precision performance
ample, the 500 μ V offset
or in a 12-bit, 5V DAC.
design objective was
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ision JFET op amps,
OP-15) data sheets.

INFORMATION

R: OP-15AJ
OP-15BJ
OP-15CJ
OP-15EJ
OP-15FJ
OP-15GJ

evices
cessing

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
OP-15A, OP-15B, OP-15E, OP-15F ± 22 V
OP-15C, OP-15G ± 18 V
Internal Power Dissipation
All Devices 500mW
(The TO-99 (J) package must be derated based on a
thermal resistance of 150° C/W junction to ambient or
45° C/W junction to case.)
Operating Temperature Range
OP-15A, OP-15B, OP-15C -55°C to +125°C
OP-15E, OP-15F, OP-15G 0°C to +70°C
Maximum Junction Temperature (T_J)
TO-99 (J) +150°C

Differential Input Voltage
OP-15A, OP-15B, OP-15E, OP-15F ± 40 V
OP-15C, OP-15G ± 30 V
Input Voltage
OP-15A, OP-15B, OP-15E, OP-15F ± 20 V
OP-15C, OP-15G ± 16 V
(Unless otherwise specified the absolute maximum
negative input voltage is equal to the negative power
supply voltage.)
Output Short Circuit Duration Indefinite
Storage Temperature Range TO-99 (J) . -65°C to +150°C
Lead Temperature Range (Soldering, 60 sec.) . . . +300°C

ELECTRICAL CHARACTERISTICS at V_S = ± 15 V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-15A			OP-15B			OP-15C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}	R _S = 50 Ω	—	0.2	0.5	—	0.4	1.0	—	0.5	3.0	mV
Input Offset Current	I _{OS}	T _J = 25°C (Note 1) Device Operating	—	3.0 5.0	10 22	—	6.0 10.0	20 40	—	10.0 20	50 100	pA
Input Bias Current	I _B	T _J = 25°C (Note 1) Device Operating	—	15 18	50 110	—	30 40	100 200	—	60 80	200 400	pA
Input Resistance	R _{IN}		—	10 ¹²	—	—	10 ¹²	—	—	10 ¹²	—	Ω
Large Signal Voltage Gain	A _{VO}	R _L $\geq$ 2k Ω V _O = ± 10 V	100	240	—	75	220	—	50	200	—	V/mV
Output Voltage Swing	V _{OM}	R _L = 10k R _L = 2k	± 12 ± 11	± 13 ± 12.7	—	± 12 ± 11	± 13 ± 12.7	—	± 12 ± 11	± 13 ± 12.7	—	V
Supply Current	I _{SY}		—	2.7	4.0	—	2.7	4.0	—	2.8	5.0	mA
Slew Rate	SR	A _{VCL} = +1.0 (Note 3)	10	17	—	7.5	16	—	5.0	15	—	V/ μ s
Gain Bandwidth Product	GBW	(Note 3)	4.0	6.0	—	3.5	5.7	—	3.0	5.4	—	MHz
Closed Loop Bandwidth	CLBW	A _{VCL} = +1.0	—	14	—	—	13	—	—	12	—	MHz
Settling Time	t _s	to 0.01% to 0.05% (Note 2) to 0.10%	—	2.2 1.1 0.9	—	—	2.3 1.1 0.9	—	—	2.4 1.2 1.0	—	μ s
Input Voltage Range	IVR		± 10.5	—	—	± 10.5	—	—	± 10.3	—	—	V
Common Mode Rejection Ratio	CMRR	V _{CM} = ± 10.5 V V _{CM} = ± 10.3 V	86 —	100 —	—	86 —	100 —	—	82 —	96 —	—	dB
Power Supply Rejection Ratio	PSRR	V _S = ± 10 V to ± 18 V V _S = ± 10 V to ± 15 V	86 —	100 —	—	86 —	100 —	—	82 —	100 —	—	dB
Input Noise Voltage Density	e _n	f _o = 100Hz f _o = 1000Hz	— —	20 15	—	— —	20 15	—	— —	20 15	—	nV/ $\sqrt{\text{Hz}}$
Input Noise Current Density	i _n	f _o = 100Hz f _o = 1000Hz	— —	0.01 0.01	—	— —	0.01 0.01	—	— —	0.01 0.01	—	pA/ $\sqrt{\text{Hz}}$
Input Capacitance	C _{IN}		—	3.0	—	—	3.0	—	—	3.0	—	pF

NOTES:

- Due to limited production test times the bias currents correspond to junction temperatures. The bias current vs time (after power-on) curve clarifies this point. Since most amplifiers (in use) are on for more than 1 second, PMI also specifies the bias current for the warmed-up condition. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_J and I_B vs T_A. PMI has a bias current compensation circuit which gives improved bias current over

- the standard JFET input op amps. I_B and I_{OS} are measured at V_{CM} = 0.
- Settling time is defined here for a unity gain inverter connection using 2k Ω resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.

- Parameter is not 100% tested. 90% of all units meet these specifications.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-15A			OP-15B			OP-15C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.4	0.9	—	0.7	2.0	—	0.9	4.5	mV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}		—	2.0	5.0	—	3.0	10	(Note 3)			$\mu V/^\circ C$
With External Trim (Note 3)	TCV_{OSn}	$R_D = 100k\Omega$	—	2.0	—	—	3.0	—	—	4.0	—	
Input Offset Current (Note 1)	I_{OS}	$T_J = 125^\circ C$	—	0.6	4.0	—	0.8	6.0	—	1.0	9.0	nA
		$T_A = 125^\circ C$ Device Operating	—	0.8	7.0	—	1.2	11	—	1.5	17	
Input Bias Current (Note 1)	I_B	$T_J = 125^\circ C$	—	1.2	5.0	—	1.5	7.5	—	1.8	10	nA
		$T_A = 125^\circ C$ Device Operating	—	1.7	9.0	—	2.2	14	—	2.7	19	
Input Voltage Range	IVR		± 10.5	—	—	± 10.5	—	—	± 10.25	—	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10.4V$	85	97	—	85	97	—	—	—	—	dB
		$V_{CM} = \pm 10.25V$	—	—	—	—	—	—	80	93	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	85	97	—	85	97	—	—	—	—	dB
		$V_S = \pm 10V$ to $\pm 15V$	—	—	—	—	—	—	80	93	—	
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10$	35	120	—	30	110	—	25	100	—	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V

OPERATIONAL AMPLIFIERS OP-15

OPERATIONAL AMPLIFIERS OP-15OPERATIONAL AMPLIFIERS OP-15

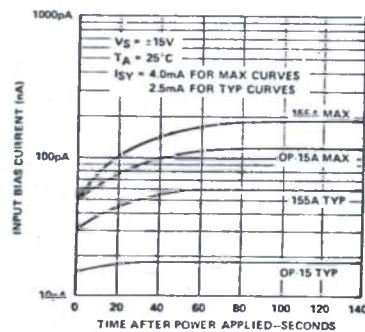
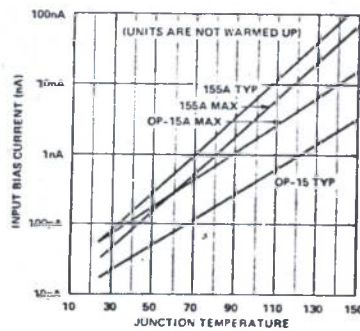
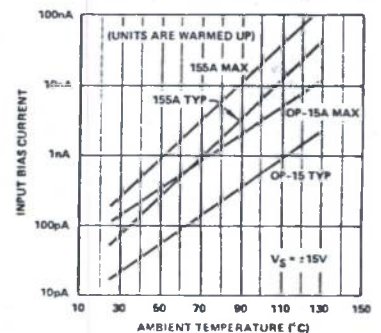
OPERATIONAL AMPLIFIERS OP-15

- OPERATIONAL AMPLIFIERS OP-15

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-15E			OP-15F			OP-15G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.3	0.75	—	0.55	1.5	—	0.7	3.8	mV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}		—	2.0	5.0	—	3.0	10	(Note 3)			$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_p = 100k\Omega$	—	2.0	—	—	3.0	—	—	4.0	—	
Input Offset Current (Note 1)	I_{OS}	$T_J = +70^\circ C$	—	0.04	0.30	—	0.06	0.45	—	0.08	0.65	nA
		$T_A = +70^\circ C$ Device Operating	—	0.06	0.55	—	0.08	0.80	—	0.10	1.2	
Input Bias Current (Note 1)	I_B	$T_J = +70^\circ C$	—	0.10	0.40	—	0.12	0.60	—	0.14	0.80	nA
		$T_A = +70^\circ C$ Device Operating	—	0.13	0.75	—	0.16	1.1	—	0.19	1.5	
Input Voltage Range	IVR	$R_S = 50\Omega$	± 10.4	—	—	± 10.4	—	—	± 10.25	—	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10.4V$	85	98	—	85	98	—	—	—	—	dB
		$V_{CM} = \pm 10.25V$	—	—	—	—	—	—	80	94	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	85	98	—	85	98	—	—	—	—	dB
		$V_S = \pm 10V$ to $\pm 15V$	—	—	—	—	—	—	80	94	—	
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10$	65	200	—	50	180	—	35	130	—	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V

TYPICAL PERFORMANCE CURVES

BIAS CURRENT vs TIME
IN FREE AIRINPUT BIAS CURRENT vs
JUNCTION TEMPERATURE
UNITS ARE NOT WARMED-UPINPUT BIAS CURRENT vs
AMBIENT TEMPERATURE (UNITS
ARE WARMED-UP IN FREE AIR)



MOTOROLA
Semiconductors
BOX 20012, TUCSON, ARIZONA 85720

MC1595L
MC1495L

Specifications and Applications Information

WIDEBAND MONOLITHIC FOUR-QUADRANT MULTIPLIER

... designed for uses where the output is a linear product of two input voltages. Maximum versatility is assured by allowing the user to select the level shift method. Typical applications include: multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

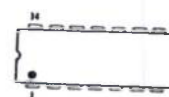
*When used with an operational amplifier.

- c Wide Bandwidth
- c Excellent Linearity — 1% max Error on X-Input, 2% max Error on Y-Input — MC1595L
- c Excellent Linearity — 2% max Error on X-Input, 4% max Error on Y-Input — MC1495L
- c Adjustable Scale Factor, K
- c Excellent Temperature Stability
- c Wide Input Voltage Range — ± 10 Volts
- c ± 15 Volt Operation

LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT

MONOLITHIC SILICON
EPITAXIAL PASSIVATED

DS 9124 R1



(top view)



CERAMIC PACKAGE
CASE 632
TO-116

FIGURE 1 — FOUR-QUADRANT
MULTIPLIER TRANSFER CHARACTERISTIC

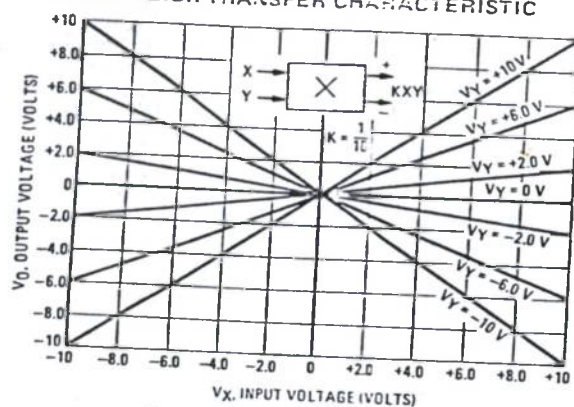


FIGURE 2 — TRANSCONDUCTANCE BANDWIDTH

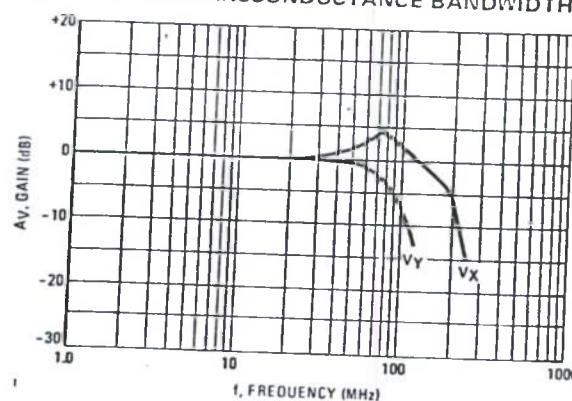
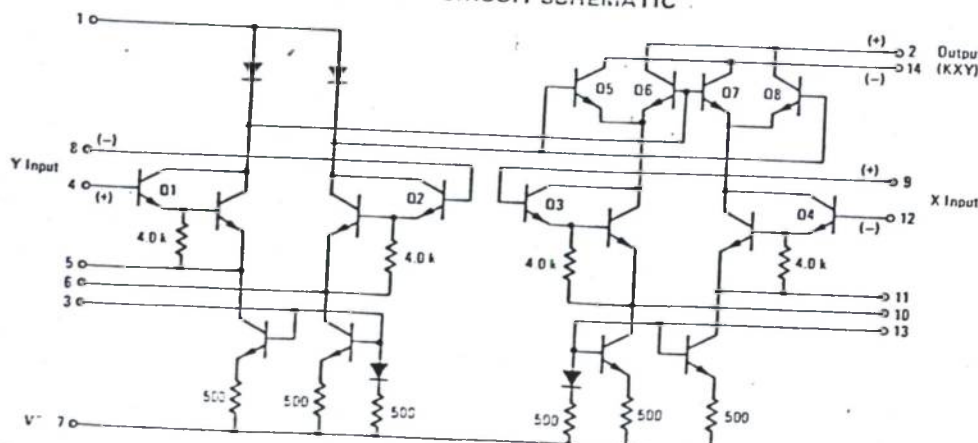


FIGURE 3 — CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS ($V^+ = -30V$, $V^- = -15V$, $T_A = +25^\circ C$, $I_3 = I_{13} = 1mA$, $R_X = R_Y = 15k\Omega$, $R_L = 11k\Omega$ unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Linearity: Output Error in Percent of Full Scale: $T_A = +25^\circ C$ $-10 < V_X < +10$ ($V_Y = \pm 10V$) $-10 < V_Y < +10$ ($V_X = \pm 10V$) $T_A = 0$ to $+70^\circ C$ $-10 < V_X < +10$ ($V_Y = \pm 10V$) $-10 < V_Y < +10$ ($V_X = \pm 10V$) $T_A = -55^\circ C$ to $+125^\circ C$ $-10 < V_X < +10$ ($V_Y = \pm 10V$) $-10 < V_Y < +10$ ($V_X = \pm 10V$)	5	ERX ERY	— — — — — — — —	± 1.0 ± 0.5 ± 2.0 ± 1.0 ± 1.5 ± 3.0 ± 0.75 ± 1.50	± 2.0 ± 1.0 ± 4.0 ± 2.0 — — — —	%
Squaring Mode Error: Accuracy in Percent of Full Scale After Offset and Scale Factor Adjustment $T_A = +25^\circ C$ $T_A = 0$ to $+70^\circ C$ $T_A = -55^\circ C$ to $+125^\circ C$	5	ESQ	— — — —	± 0.75 ± 0.5 ± 1.0 ± 0.75	— — — —	%
Scale Factor (Adjustable) $(K = \frac{2R_L}{I_3 R_X R_Y})$	—	K	—	0.1	—	—
Input Resistance ($f = 20Hz$)	7	R _{INX} R _{INY}	— — — —	20 35 20 35	— — — —	MegOhms
Differential Output Resistance ($f = 20Hz$)	8	R _O	—	300	—	k Ohms
Input Bias Current $I_{bx} = \frac{(I_9 + I_{12})}{2}$, $I_{by} = \frac{(I_4 + I_8)}{2}$	6	I _{bx} I _{by}	— — — —	2.0 2.0 2.0 2.0	12 8.0 12 8.0	μA
Input Offset Current $ I_9 - I_{12} $ $ I_4 - I_8 $	6	I _{iox} I _{ioy}	— — — —	0.4 0.2 0.4 0.2	2.0 1.0 2.0 1.0	μA
Average Temperature Coefficient of Input Offset Current ($T_A = 0$ to $+70^\circ C$) ($T_A = -55^\circ C$ to $+125^\circ C$)	6	TC _{Iio}	— —	2.0 2.0	— —	nA/ $^\circ C$
Output Offset Current $ I_{14} - I_{12} $	6	I _{oos}	— —	20 10	100 50	μA
Average Temperature Coefficient of Output Offset Current ($T_A = 0$ to $+70^\circ C$) ($T_A = -55^\circ C$ to $+125^\circ C$)	6	TC _{Ioo}	— —	20 20	— —	nA/ $^\circ C$
Frequency Response 3.0 dB Bandwidth, $R_L = 11k\Omega$ 3.0 dB Bandwidth, $R_L = 50\Omega$ (Transconductance Bandwidth) 3 $^\circ$ Relative Phase Shift Between V_X and V_Y 1% Absolute Error Due to Input-Output Phase Shift	9,10	BW _{3dB} TBW _{3dB} f_ϕ f_θ	— — — —	3.0 80 750 30	— — — —	MHz MHz kHz kHz
Common Mode Input Swing (Either Input)	11	CMV	± 10.5 ± 11.5	± 12 ± 13	— —	Vdc
Common Mode Gain (Either Input)	11	A _{CM}	-40 -50	-50 -60	— —	dB
Common Mode Quiescent Output Voltage	12	V _{o1} V _{o2}	— —	21 21	— —	Vdc
Differential Output Voltage Swing Capability	9	V _O	—	± 14	—	V _{peak}
Power Supply Sensitivity	12	S ⁺ S ⁻	— —	5.0 10	— —	mV/V
Power Supply Current	12	I ₇	—	6.0	7.0	mA
DC Power Dissipation	12	P _D	—	135	170	mW





**National
Semiconductor**

LM104/LM204/LM304 Negative Regulator

General Description

The LM104 series are precision voltage regulators which can be programmed by a single external resistor to supply any voltage from 40V down to zero while operating from a single unregulated supply. They can also provide 0.01 percent regulation in circuits using a separate, floating bias supply, where the output voltage is limited only by the breakdown of external pass transistors. Although designed primarily as linear, series regulators, the circuits can be used as switching regulators, current regulators or in a number of other control applications. Typical performance characteristics are:

- Subsurface zener reference
- 1 mV regulation no load to full load
- 0.01%/V line regulation
- 0.2 mV/V ripple rejection

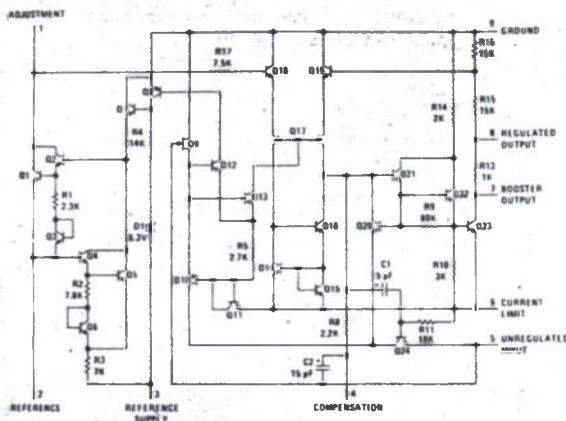
Voltage Regulators

- 0.3% temperature stability over military temperature range

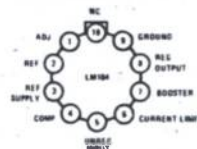
The LM104 series are complements of the LM100 and LM105 positive regulators, intended for systems requiring regulated negative voltages which have a common ground with the unregulated supply. By themselves, they can deliver output currents to 25 mA, but external transistors can be added to get any desired current. The output voltage is set by external resistors, and either constant or foldback current limiting is made available.

The LM104 is specified for operation over the -55°C to $+125^{\circ}\text{C}$ military temperature range. The LM204 is specified for operation over the -25°C to $+85^{\circ}\text{C}$ temperature range. The LM304 is specified for operation from 0°C to $+70^{\circ}\text{C}$.

Schematic and Connection Diagrams



Metal Can Package

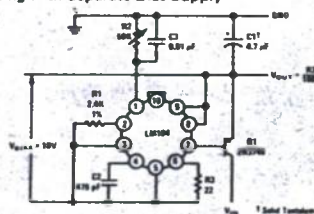


Note: Pin 5 connected to case.
TOP VIEW

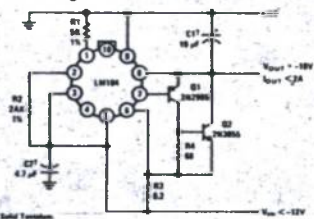
Order Number LM104H, LM204H or LM304H
See NS Package H10C

Typical Applications

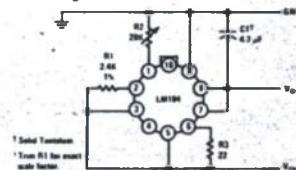
Operating with Separate Bias Supply



High Current Regulator



Basic Regulator Circuit



Absolute Maximum Ratings

	LM104/LM204	LM304
Input Voltage	50V	40V
Input-Output Voltage Differential	50V	40V
Power Dissipation (Note 1)	500 mW	500 mW
Operating Temperature Range		
LM104	-55°C to 125°C	
LM204	-25°C to 85°C	
LM304		0°C to +70°C
Storage Temperature Range	-65°C to 150°C	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C	300°C

Electrical Characteristics

PARAMETER	CONDITIONS	LM104/LM204			LM304			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage Range		-50		-8	-40		-8	V
Output Voltage Range		-40		-0.015	-30		-0.035	V
Output-Input Voltage Differential (Note 3)	$I_O = 20 \text{ mA}$ $I_O = 5 \text{ mA}$	2.0 0.5		50 50	2.0 0.5		40 40	V V
Load Regulation (Note 4)	$0 \leq I_O \leq 20 \text{ mA}$ $R_{SC} = 15\Omega$		1	5		1	5	mV
Line Regulation (Note 5)	$V_{OUT} \leq -5V$ $\Delta V_{IN} = 0.1 V_{IN}$		0.056	0.1		0.056	0.1	%
Ripple Rejection	$C_{19} = 10 \mu F$, $f = 120 \text{ Hz}$ $V_{IN} < -15V$ $-7V \geq V_{IN} \geq -15V$		0.2 0.5	0.5 1.0		0.2 0.5	0.5 1.0	mV/V mV/V
Output Voltage Scale Factor	$R_{23} = 2.4k$	1.8	2.0	2.2	1.8	2.0	2.2	V/k Ω
Temperature Stability	$V_O \leq -1V$		0.3	1.0		0.3	1.0	%
Output Noise Voltage	$10 \text{ Hz} \leq f \leq 10 \text{ kHz}$ $V_O \leq -5V$, $C_{19} = 0$ $C_{19} = 10 \mu F$		0.007 15			0.007 15		% μV
Standby Current Drain	$I_L = 5 \text{ mA}$, $V_O = 0$ $V_O = -30V$ $V_O = -40V$		1.7 3.6	2.5 5.0		1.7 3.6	2.5 5.0	mA mA mA
Long Term Stability	$V_O \leq -1V$		0.01	1.0		0.01	1.0	%

Note 1: The maximum junction temperature of the LM104 is 150°C, while that of the LM204 is 125°C and LM304 is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case.

Note 2: These specifications apply for junction temperatures between -55°C and 150°C (between -25°C and 100°C for the LM204 and 0°C to +85°C for the LM304) and for input and output voltages within the ranges given, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

Note 3: When external booster transistors are used, the minimum output-input voltage differential is increased, in the worst case, by approximately 1V.

Note 4: The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.

Note 5: With zero output, the dc line regulation is determined from the ripple rejection. Hence, with output voltages between 0V and -5V, a dc output variation, determined from the ripple rejection, must be added to find the worst-case line regulation.



Voltage Regulators

LM105/LM205/LM305

LM105/LM205/LM305 voltage regulator general description

The LM105, LM205 and LM305 are positive voltage regulators similar to the LM100, except that an extra gain stage has been added for improved regulation. A redesign of the biasing circuitry removes any minimum load current requirement and at the same time reduces standby current drain, permitting higher voltage operation. They are direct, plug-in replacements for the LM100 in both linear and switching regulator circuits with output voltages greater than 4.5V. Important characteristics of the circuits are:

- Output voltage adjustable from 4.5V to 40V
- Output currents in excess of 10A possible by adding external transistors
- Load regulation better than 0.1%, full load with current limiting

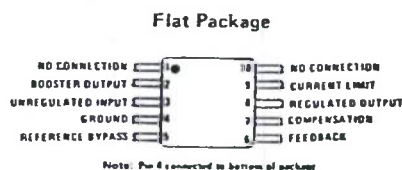
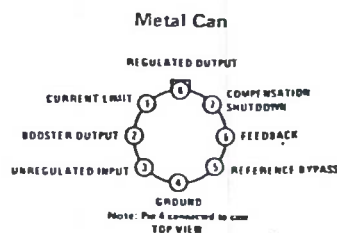
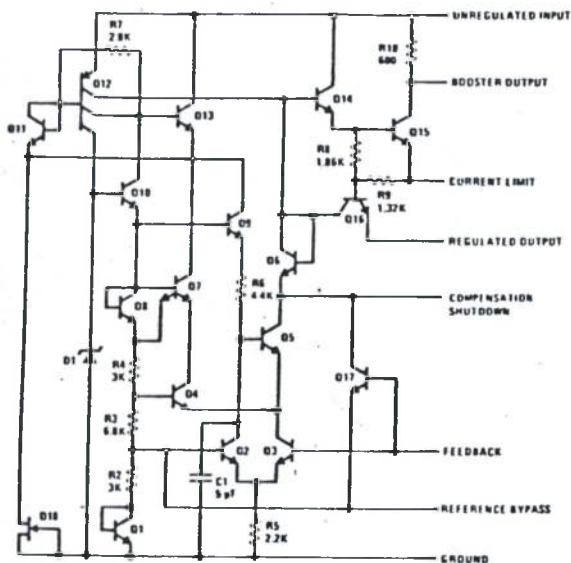
- DC line regulation guaranteed at 0.03%/V
- Ripple rejection of 0.01%/V

Like the LM100, they also feature fast response to both load and line transients, freedom from oscillations with varying resistive and reactive loads and the ability to start reliably on any load within rating. The circuits are built on a single silicon chip and are supplied in either an 8-lead, TO-5 header or a 1/4" x 1/4" metal flat package.

The LM205 is identical to the LM105 except that it is specified for operation from -25°C to 85°C.

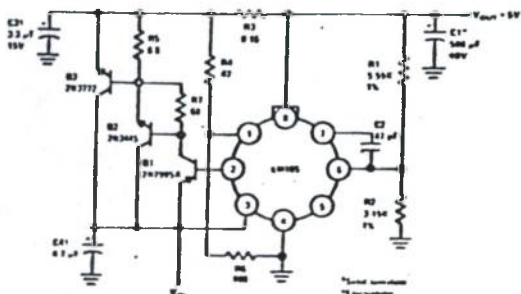
The LM305 is specified for operation from 0°C to 70°C and for output voltages to 30V.

schematic and connection diagrams

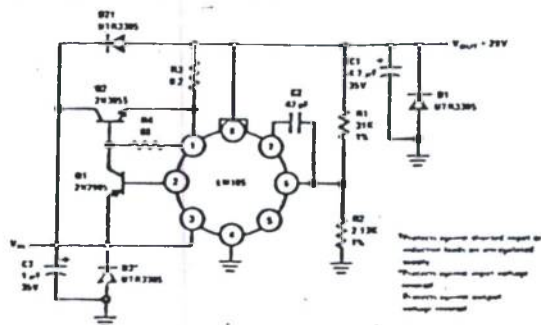


typical applications

10A Regulator with Foldback Current Limiting



1.0A Regulator with Protective Diodes



absolute maximum ratings

Input Voltage	50V
LM105, LM205	40V
LM305	40V
Input-Output Voltage Differential	40V
Power Dissipation (Note 1)	800 mW
LM105, LM205	500 mW
LM305	
Operating Temperature Range	0°C to 70°C
LM105	-55°C to +85°C
LM205	-25°C to +150°C
LM305	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range					
LM105, LM205		8.5		50	V
LM305		8.5		40	V
Output Voltage Range					
LM105, LM205		4.5		40	V
LM305		4.5		30	V
Output Input Voltage Differential		3.0		30	V
Load Regulation (Note 3)					
LM105	$0 \leq I_O \leq 12 \text{ mA}$ $R_{SC} = 18\Omega, T_A = 25^\circ\text{C}$ $R_{SC} = 10\Omega, T_A = 125^\circ\text{C}$ $R_{SC} = 18\Omega, T_A = -55^\circ\text{C}$		0.02 0.03 0.03	0.05 0.1 0.1	% % %
LM205	$0 \leq I_O \leq 12 \mu\text{A}$ $R_{SC} = 18\Omega, T_A = 25^\circ\text{C}$ $R_{SC} = 10\Omega, T_A = 85^\circ\text{C}$ $R_{SC} = 18\Omega, T_A = -25^\circ\text{C}$		0.02 0.03 0.03	0.05 0.1 0.1	% % %
LM305	$0 \leq I_O \leq 12 \text{ mA}$ $R_{SC} = 18\Omega, T_A = 25^\circ\text{C}$ $R_{SC} = 15\Omega, T_A = 70^\circ\text{C}$ $R_{SC} = 18\Omega, T_A = 0^\circ\text{C}$		0.02 0.03 0.03	0.05 0.1 0.0	% % %
Line Regulation	$V_{IN} - V_{OUT} \leq 5\text{V}$ $V_{IN} - V_{OUT} > 5\text{V}$		0.025 0.015	0.06 0.03	%/V %/V
Ripple Rejection	$C_{REF} = 10 \mu\text{F}, f = 120 \text{ Hz}$		0.003	0.01	%/V
Temperature Stability					
LM105	$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		0.3	1.0	%
LM205	$-25^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		0.3	1.0	%
LM305	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$		0.3	1.0	%
Feedback Sense Voltage		1.63	1.7	1.81	V
Output Noise Voltage	$10 \text{ Hz} \leq f \leq 10 \text{ kHz}$ $C_{REF} = 0$ $C_{REF} > 0.1 \mu\text{F}$		0.005 0.002		% %
Standby Current Drain					
LM105, LM205	$V_{IN} = 40\text{V}$		0.8	2.0	mA
LM305	$V_{IN} = 50\text{V}$		0.8	2.0	mA
Long Term Stability			0.1	1.0	%

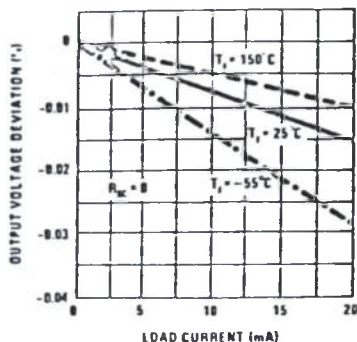
Note 1: The maximum junction temperature of the LM105 is 150°C, while that for the LM205 is 100°C, and that for the LM305 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. Peak dissipations to 1W are allowable providing the dissipation rating is not exceeded with the power averaged over a five second interval for the LM105 and LM205, and averaged over a two second interval for the LM305.

Note 2: These specifications apply for input and output voltages within the ranges given, and for a divider impedance seen by the feedback terminal of 2 k Ω , unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation. With the LM205, however, all temperature specifications are limited to -25°C to 85°C.

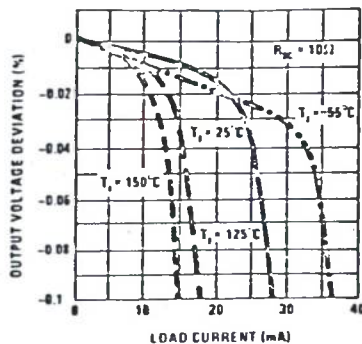
Note 3: The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.

typical performance characteristics

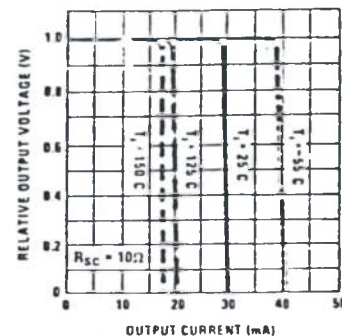
Load Regulation



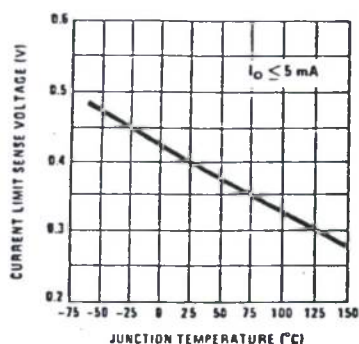
Load Regulation



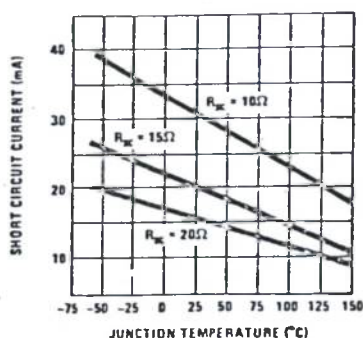
Current Limiting Characteristics



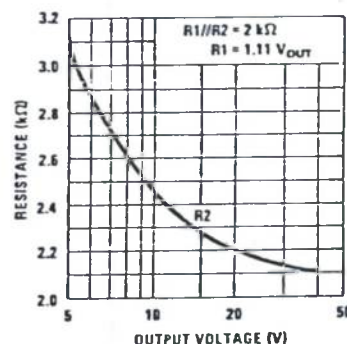
Current Limit Sense Voltage



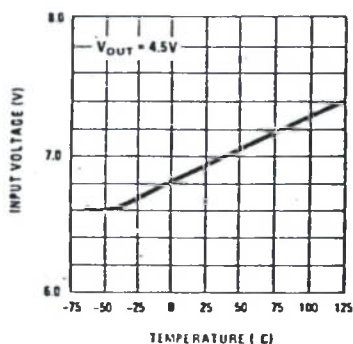
Short Circuit Current



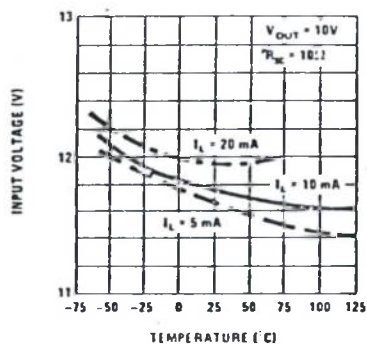
Optimum Divider Resistance Values



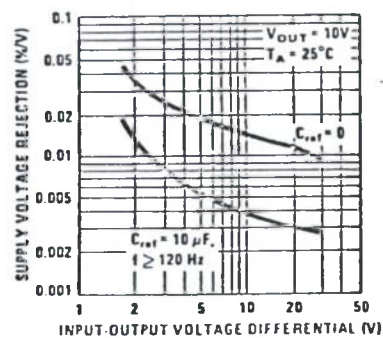
Minimum Input Voltage



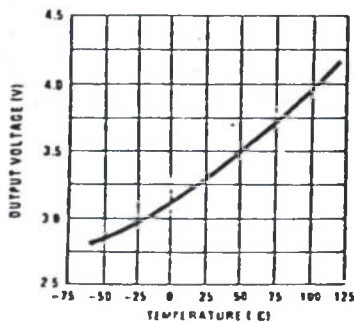
Regulator Dropout Voltage



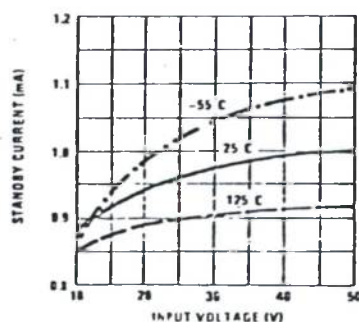
Supply Voltage Rejection



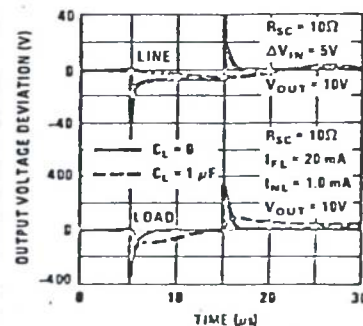
Minimum Output Voltage



Standby Current Drain



Transient Response





General Purpose Resistors

TYPE TR—1/10 Watt

TYPE CB—1/4 Watt

TYPE EB—1/2 Watt

TYPE GB—1 Watt

TYPE HB—2 Watt

Metal Clad Resistors

TYPE GM—3 Watt

TYPE HM—4 Watt

Hermetically Sealed— Ceramic Encased Resistors

TYPE TS—1/4 Watt

TYPE CS—1/2 Watt

TYPE ES—1 Watt

1. Resistance changes due to humidity are temporary, and in the case of Allen-Bradley resistors are reversible.
2. Resistance changes due to increase in moisture content are always positive.
3. Resistance change due to humidity in low-value resistors is less than in high-value resistors.
4. Change of resistance which has occurred due to humidity may be essentially eliminated by conditioning the resistor at 100°C for 48 hours.
5. Resistors operating with as little as 1/10th rated wattage load are essentially not affected by humidity.
6. Hermetically-sealed resistors do not exhibit resistance change because of humidity.
7. Resistance change due to load life is permanent and ultimately negative.
8. Resistance change due to load life can be minimized —1% to 2% in many thousands of hours by 50% derating.
9. This same result can be attained by limiting the maximum operating surface temperature of the resistor under load to 100°C.
10. Resistance change due to soldering is positive and may be permanent if the resistor has moisture present in its body. It can be greatly minimized if resistors are dry at the time of soldering.
11. The temperature characteristic of the Allen-Bradley resistor is positive above and below room temperature —room temperature is considered to be between 10°C and 30°C.
12. The temperature characteristic of the Allen-Bradley resistor is negligible from —10°C to +80°C.
13. The voltage characteristic of the Allen-Bradley resistor is negative and is less at elevated operated temperatures than at room ambient.
14. The voltage characteristic is less in low-value resistors than in high-value units.
15. The voltage characteristic and the temperature characteristic tend to cancel one another in an Allen-Bradley resistor under average operating conditions, where both voltage and temperature are present.
16. The heat sink to which a resistor is connected affects its rating. Resistors operated in parallel should be derated unless an adequate heat sink is provided.
17. The quality and reliability of Allen-Bradley resistors is the same for, and independent of, any resistance tolerances shown on the resistor.



MM2114, MM2114L Family 4096-Bit (1024 x 4) Static RAMs

General Description

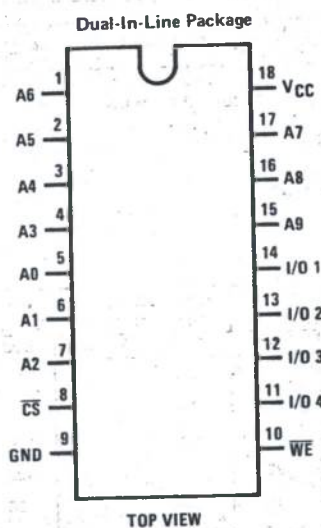
The MM2114 family of 1024-word by 4-bit static random access memories is fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The separate chip select input ($\overline{CS}$) allows easy memory expansion by OR-tying individual devices to a data bus.

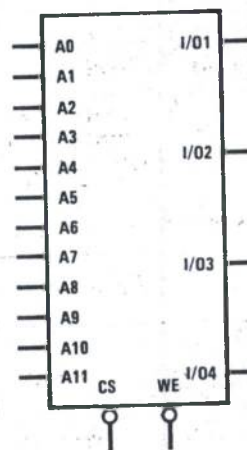
Features

- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Low power—225 mW typical
- High speed—down to 200 ns access time
- TRI-STATE® output for bus interface
- Common Data In and Data Out pins
- Single 5V supply
- Standard 18-pin dual-in-line package

Connection Diagram



Logic Symbol



Order Number MM2114J-25L, MM2114J-25,
MM2114J-2L, MM2114J-2, MM2114J, MM2114J-L,
MM2114J-3L or MM2114J-3
See NS Package J18A

Order Number MM2114N-2L, MM2114N-2,
MM2114N, MM2114N-L, MM2114N-3L
or MM2114N-3
See NS Package N18A

Truth Table

$\overline{CS}$	$\overline{WE}$	I/O	MODE
H	X	Hi-Z	Not Selected
L	L	H	Write 1
L	L	L	Write 0
L	H	DOUT	Read

Two pins (Select (CS) controls Tri-State Enable (WE) and also controls details the and WE co

READ-cycle Time Wave any change fetched an low, howe transfer th

Address a address of assuming arrival. Cl

Functional Description

Two pins control the operation of the MM2114. Chip Select ($\overline{CS}$) enables write and read operations and controls TRI-STATING of the data-output buffer. Write Enable ($\overline{WE}$) chooses between READ and WRITE modes and also controls output TRI-STATING. The truth table details the states produced by combinations of the $\overline{CS}$ and $\overline{WE}$ controls.

READ-cycle timing is shown in the section on Switching Time Waveforms. $\overline{WE}$ is kept high. Independent of $\overline{CS}$, any change in address code causes new data to be fetched and brought to the output buffer. $\overline{CS}$ must be low, however, for the output buffer to be enabled and transfer the data to the output pin.

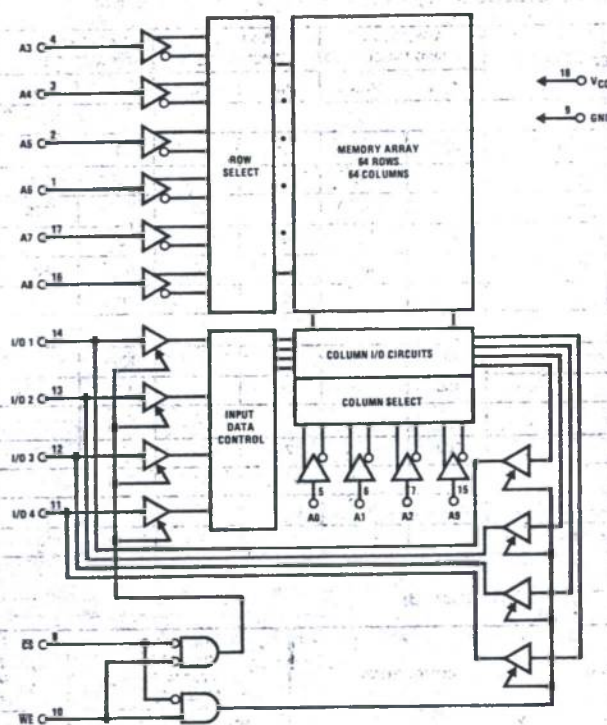
Address access time, t_A , is the time required for an address change to produce new data at the output pin, assuming $\overline{CS}$ has enabled the output buffer prior to data arrival. Chip Select-to-output delay, t_{CO} , is the time

required for $\overline{CS}$ to enable the output buffer and transfer previously fetched data to the output pin. Operation with $\overline{CS}$ continuously held low is permissible.

WRITE-cycle timing is shown in the section on Switching Time Waveforms. Writing occurs only during the time both $\overline{CS}$ and $\overline{WE}$ are low. Minimum write pulse width, t_{WP} , refers to this simultaneous low region. Data set-up and hold times are measured with respect to whichever control first rises. Successive write operations may be performed with $\overline{CS}$ continuously held low. $\overline{WE}$ then is used to terminate WRITE between address changes. Alternatively, $\overline{WE}$ may be held low for successive WRITES and $\overline{CS}$ used for WRITE interruption between address change.

In any event, either $\overline{WE}$ or $\overline{CS}$ (or both) must be high during address transitions to prevent erroneous WRITE.

Block Diagram



Absolute Maximum Ratings

Voltage at Any Pin	-0.5V to +7V
Storage Temperature	-65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C

DC Electrical Characteristics $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MM2114 MM2114-2 MM2114-25 MM2114-3		MM2114-L MM2114-2L MM2114-25L MM2114-3L		UNITS
			MIN	MAX	MIN	MAX	
V_{IH}	Logical "1" Input Voltage		2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Logical "0" Input Voltage		-0.5	0.8	-0.5	0.8	V
V_{OH}	Logical "1" Output Voltage	$I_{OH} = -1.0\text{ mA}$	2.4		2.4		V
V_{OL}	Logical "0" Output Voltage	$I_{OL} = 2.1\text{ mA}$		0.4		0.4	V
I_{LI}	Input Load Current	$V_{IN} = 0$ to $5.25V$	-10	10	-10	10	μA
I_{LO}	Output Leakage Current	$V_O = 4V$ to $0.4V$, $C_S = V_{IH}$	-10	10	-10	10	μA
I_{CC1}	Power Supply Current	All Inputs = $5.25V$, $T_A = 25^\circ\text{C}$		95		65	mA
I_{CC2}	Power Supply Current	All Inputs = $5.25V$, $T_A = 0^\circ\text{C}$		100		70	mA

AC Electrical Characteristics $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$, (Note 2)

SYMBOL	PARAMETER	MM2114-2 MM2114-2L		MM2114-25 MM2114-25L		MM2114-3 MM2114-3L		MM2114 MM2114-L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE										
t _{RC}	Read Cycle Time ($\overline{WE} = V_{IH}$)	200		250		300		450		ns
t _A	Access Time		200		250		300		450	ns
t _{CO}	Chip Select to Output Valid		70		90		100		120	ns
t _{CX}	Chip Select to Output Active	20		20		20		20		ns
t _{COT}	Chip Select to Output TRI-STATE	0	40	0	60	0	80	0	100	ns
t _{OHA}	Output Hold from Address Change	10		10		10		10		ns
WRITE CYCLE										
t _{WC}	Write Cycle Time	200		250		300		450		ns
t _{WP}	Write Pulse Width	100		125		150		200		ns
t _{WR}	Write Recovery Time	0		0		0		0		ns
t _{DS}	Data Set-Up Time	100		125		150		200		ns
t _{DH}	Data Hold Time	0		0		0		0		ns
t _{WOT}	Write Enable to Output TRI-STATE	0	40	0	60	0	80	0	100	ns
t _{WO}	Write Enable to Output Valid		80		90		100		120	ns

Capacitance $T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MM2114 MM2114-2 MM2114-25 MM2114-3		MM2114-L MM2114-2L MM2114-25L MM2114-3L		UNITS
			MIN	MAX	MIN	MAX	
C_{IN}	Input Capacitance	All Inputs $V_{IN} = 0V$		5		5	pF
C_{OUT}	Output Capacitance	$V_O = 0V$		10		10	pF

Note 1: Typical values at $T_A = 25^\circ\text{C}$.

Note 2: All input transitions $\leq 10\text{ ns}$. Timing referenced to $V_{IL}(\text{MAX})$ or $V_{IH}(\text{MIN})$ for inputs, $0.8V$ and $2V$ for output. For test purposes, input levels should swing between $0V$ and $3V$. Output load = 1 TTL gate and $C_L = 100\text{ pF}$.

Note 3: This parameter is guaranteed by periodic testing.

HIGH SPEED 4096 x 1 BIT STATIC RAM

	2147H-1	2147H-2	2147H-3	2147H-4
Max. Access Time (ns)	35	45	55	55
Max. Active Current (mA)	180	180	180	125
Max. Standby Current (mA)	30	30	30	15

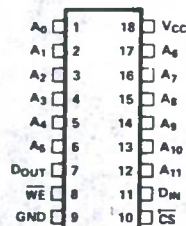
- Pinout, Function, and Power Compatible to Industry Standard 2147
- HMOS II Technology
- Completely Static Memory — No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Single +5V Supply
- 0.8 - 2.0V Output Timing Reference Levels
- Direct Performance Upgrade for 2147
- Automatic Power-Down
- High Density 18-Pin Package
- Directly TTL Compatible — All Inputs and Output
- Separate Data Input and Output
- Three-State Output

The Intel® 2147H is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit using HMOS-11, Intel's next generation high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

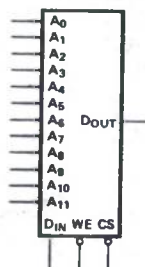
$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high — deselecting the 2147H — the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are deselected.

The 2147H is placed in an 18-pin package configured with the industry standard 2147 pinout. It is directly TTL compatible in all respects: inputs, output, and a single +V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

PIN CONFIGURATION



LOGIC SYMBOL



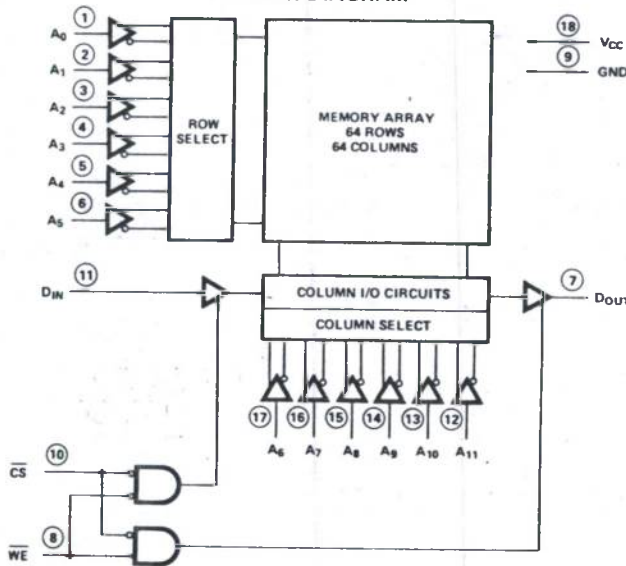
PIN NAMES

A ₀ -A ₁₁	ADDRESS INPUTS	V _{CC}	POWER (+5V)
WE	WRITE ENABLE	GND	GROUND
CS	CHIP SELECT		
D _{IN}	DATA INPUT		
D _{OUT}	DATA OUTPUT		

TRUTH TABLE

CS	WE	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D _{OUT}	ACTIVE

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-10°C to 85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin With Respect to Ground	-3.5V to +7V
Power Dissipation	1.2W
D.C. Output Current	20mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS ^[1]

T_A = 0°C to 70°C, V_{CC} = +5V ± 10%, unless otherwise noted.

Symbol	Parameter	2147H-1, 2, 3			2147H-4			Unit	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
I _{LI}	Input Load Current (All Input Pins)		.01	10		.01	10	μA	V _{CC} =MAX, V _{IN} =GND to V _{CC}
I _{LO}	Output Leakage Current		0.1	50		0.1	50	μA	$\overline{CS}$ =V _{IH} , V _{CC} =Max., V _{OUT} =GND to 4.5V
I _{CC}	Operating Current		120	170 180			115 125	mA	TA=25°C V _{CC} =Max., $\overline{CS}$ =V _{IL} TA=0°C Outputs Open
I _{SB}	Standby Current		18	30		6	15	mA	V _{CC} =Min. to Max. $\overline{CS}$ =V _{IH}
I _{PO} ^[3]	Peak Power-On Current		35	70		25	50	mA	V _{CC} =GND to V _{CC} Min., $\overline{CS}$ =Lower of V _{CC} or V _{IH} Min.
V _{IL}	Input Low Voltage	-3.0		0.8	-3.0		0.8	V	
V _{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V	
V _{OL}	Output Low Voltage			0.4			0.4	V	I _{OL} =8mA
V _{OH}	Output High Voltage	2.4			2.4			V	I _{OH} =-4.0mA
I _{OS}	Output Short Circuit Current	-150		+150	-150		+150	mA	V _{OUT} =GND to V _{CC}

Notes:

- The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
- Typical limits are at V_{CC}=5V, T_A=+25°C, and specified loading.
- A pull-up resistor to V_{CC} on the CS input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.

A.C. TEST CONDITIONS

Input Pulse Levels	GND to 3.0Volts
Input Rise and Fall Times	5nsec
Input Timing Reference Levels	1.5Volts
Output Timing Reference Level (2147H-1)	1.5Volts
Output Timing Reference Levels (2147H-2, 3, 4)	0.8-2.0V
Output Load	See Figure 1

CAPACITANCE ^[4]

T_A=25°C, f=1.0MHz

Symbol	Parameter	Max.	Unit	Conditions
C _{IN}	Input Capacitance	5	pF	V _{IN} =0V
C _{OUT}	Output Capacitance	6	pF	V _{OUT} =0V

Note 4. This parameter is sampled and not 100% tested.

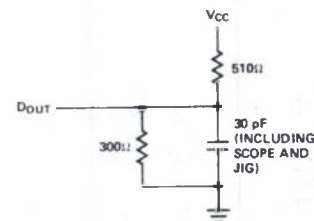


Figure 1. Output Load

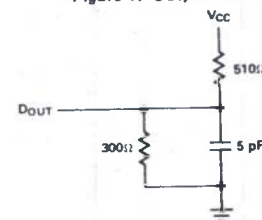


Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

A.C. CH
T_A = 0°C to 7

Symbol	Para
t _{RC} ^[1]	Reac
t _{AA}	Add
t _{ACS} ¹	Chip
t _{ACS} ²	Chip
t _{OH}	Outp
t _{LZ} ^[2] ^[7]	Chip
t _{HZ} ^[2] ^[7]	Chip
t _{PU}	Chip
t _{PD}	Chip

WAVEFORM

READ CYCLE

ADDRESS

DATA OUT

READ CYCLE

CS

DATA OUT

V_{CC} SUPPLY
CURRENT I_{CC} I_{SB}

Notes:

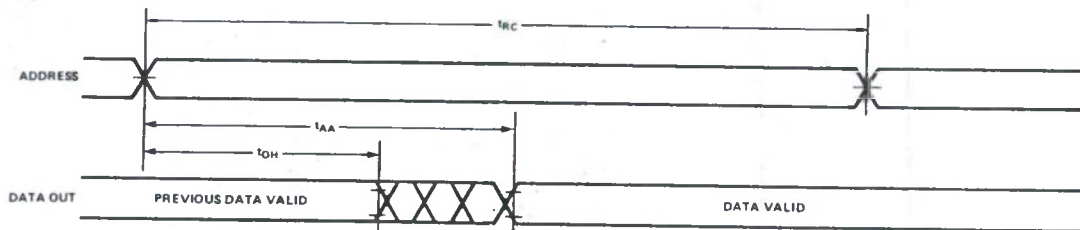
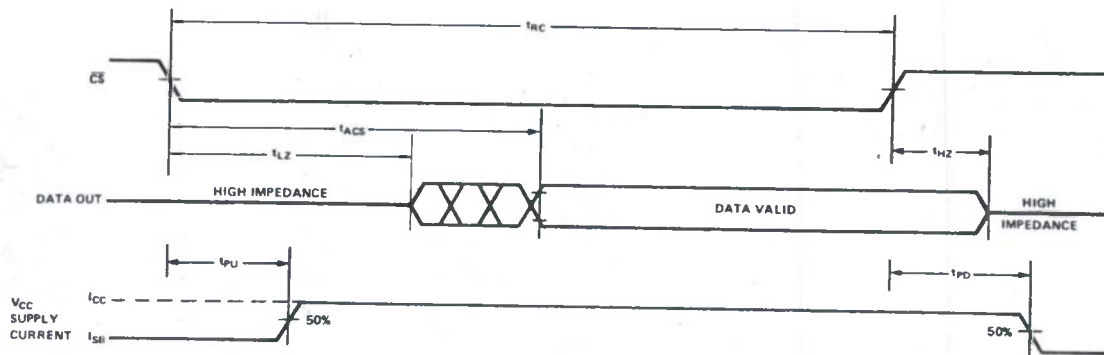
- All Read Cycle t
- At any given tem
- Transition is me
- WE is high for R
- Device is continu
- Addresses valid
- This parameter is
- Chip deselected
- Chip deselected
- occurs according

A.C. CHARACTERISTICS

TA = 0°C to 70°C, VCC = +5V±10%, unless otherwise noted.

Symbol	Parameter	2147H-1		2147H-2		2147H-3, 4		Unit	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{RC} ^[1]	Read Cycle Time	35		45		55		ns	
t _{AA}	Address Access Time		35		45		55	ns	
t _{ACS} ¹	Chip Select Access Time		35		45		55	ns	Note 8
t _{ACS} ²	Chip Select Access Time		35		45		65	ns	Note 9
t _{OH}	Output Hold from Address Change	5		5		5		ns	
t _{LZ} ^{[2] [7]}	Chip Selection to Output in Low Z	5		5		10		ns	Note 3
t _{HZ} ^{[2] [7]}	Chip Deselection to Output in High Z	0	30	0	30	0	30	ns	Note 3
t _{PU}	Chip Selection to Power Up Time	0		0		0		ns	
t _{PD}	Chip Deselection to Power Down Time		20		20		20	ns	

WAVEFORMS

READ CYCLE NO. 1^[4,5]READ CYCLE NO. 2^[4,6]

Notes:

1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500 mV from steady state voltage with specified loading in Figure 2.
4. $\overline{WE}$ is high for Read Cycles.
5. Device is continuously selected, $\overline{CS} = V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.
8. Chip deselected for greater than 55 ns prior to selection.
9. Chip deselected for a finite time that is less than 55 ns prior to selection. (If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle No. 1. Applies to 2147H-3 specification.

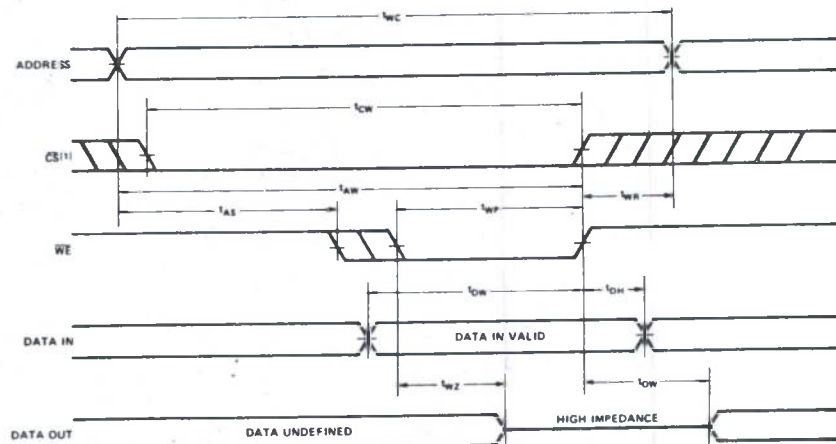
A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

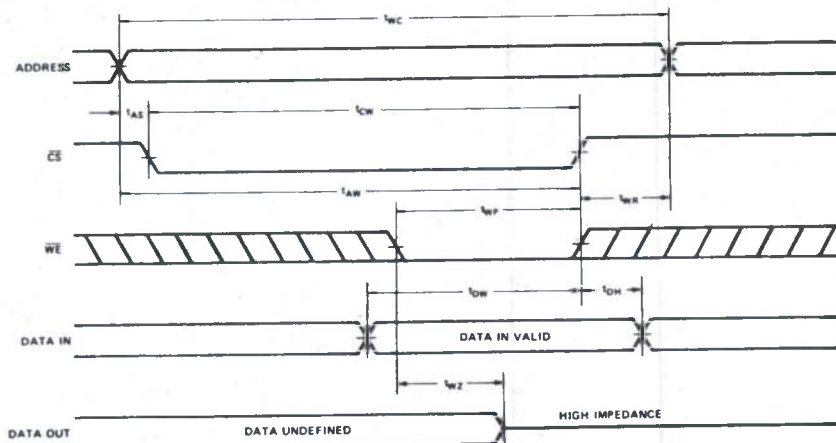
Symbol	Parameter	2147H-1		2147H-2		2147H-3, 4		Unit	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{WC}^{(2)}$	Write Cycle Time	35		45		55		ns	
t_{CW}	Chip Selection to End of Write	35		45		45		ns	
t_{AW}	Address Valid to End of Write	35		45		45		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{WP}	Write Pulse Width	20		25		25		ns	
t_{WR}	Write Recovery Time	0		0		10		ns	
t_{DW}	Data Valid to End of Write	20		25		25		ns	
t_{DH}	Data Hold Time	10		10		10		ns	
t_{WZ}	Write Enabled to Output in High Z	0	20	0	25	0	25	ns	Note 3
t_{OW}	Output Active from End of Write	0		0		0		ns	Note 3

WAVEFORMS

WRITE CYCLE #1

(WE CONTROLLED)^[4]

WRITE CYCLE #2

(CS CONTROLLED)^[4]

Note:

1. If CS goes high simultaneously with WE high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ± 500 mV from steady state voltage with specified loading in Figure 2.
4. CS or WE must be high during address transitions.

Am25LS2521

Eight-Bit Equal-To Comparator

DISTINCTIVE CHARACTERISTICS

- 8-bit byte oriented equal comparator
- Cascadable using $\bar{E}_{IN}$
- High-speed, Low-Power Schottky technology
- $t_{pd} A \bullet B$ to $\bar{E}_{OUT}$ in 9ns
- Standard 20-pin package
- 100% product assurance screening to MIL-STD-883 requirements

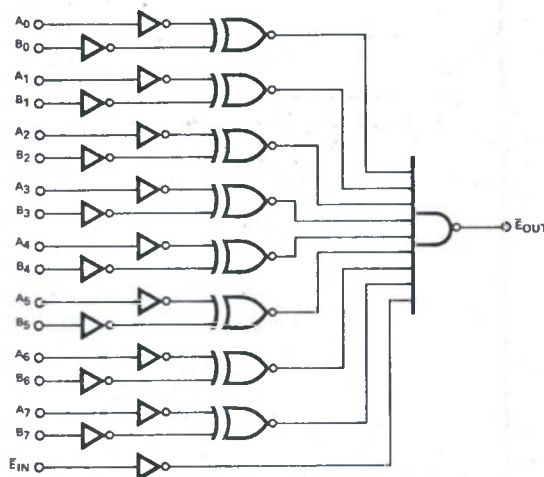
FUNCTIONAL DESCRIPTION

The Am25LS2521 is an 8-bit "equal to" comparator capable of comparing two 8-bit words for "equal to" with provision for expansion or external enabling. The matching of the two 8-bit inputs plus a logic LOW on the $\bar{E}_{IN}$ produces an active LOW on the output $\bar{E}_{OUT}$.

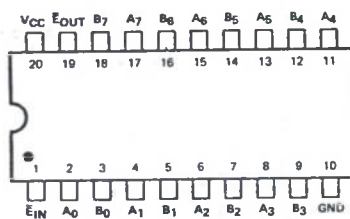
The logic expression for the device can be expressed as:

$$\bar{E}_{OUT} = (A_0 \odot B_0) (A_1 \odot B_1) (A_2 \odot B_2) (A_3 \odot B_3) (A_4 \odot B_4) (A_5 \odot B_5) (A_6 \odot B_6) (A_7 \odot B_7) \bar{E}_{IN}$$
 It is obvious that the expression is valid where $A_0 - A_7$ and $B_0 - B_7$ are expressed as either assertions or negations. This is also true for pair of terms i.e. A_0 can be compared with B_0 at the same time $\bar{A}_1$ is compared with $\bar{B}_1$. It is only essential that the polarity of the paired terms be maintained.

LOGIC DIAGRAM

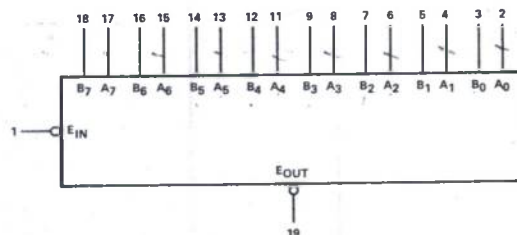


CONNECTION DIAGRAM



Note: Pin 1 is marked for orientation

LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 5\%$ MIN. = 4.75V MAX. = 5.25V
 MIL $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$ MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

DC CHARACTERISTICS OVER OPERATING RANGE								
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units	
V _{OH}	Output HIGH Voltage	V _{CC} = MIN. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -440μA	MIL COM'L	2.5 2.7		Volts	
V _{OL}	Output LOW Voltage	V _{CC} = MIN. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 4.0mA			0.4	Volts	
			I _{OL} = 8.0mA			0.45		
			I _{OL} = 12mA			0.5		
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0		Volts	
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL COM'L		0.7 0.8	Volts	
V _I	Input Clamp Voltage	V _{CC} = MIN., I _{IN} = -18mA				-1.5	Volts	
I _{IL}	Input LOW Current	V _{CC} = MAX., V _{IN} = 0.4 V		A _i , B _i E		-0.36 -0.72	mA	
I _{IH}	Input HIGH Current	V _{CC} = MAX., V _{IN} = 2.7 V		A _i , B _i E		20 40	μA	
I _I	Input HIGH Current	V _{CC} = MAX., V _{IN} = 7.0 V		A _i , B _i E		0.1 0.2	mA	
I _{SC}	Output Short Circuit Current (Note 3)	V _{CC} = MAX.			-15		-85	mA
I _{CC}	Power Supply Current (Note 4)	V _{CC} = MAX.				27	40	mA

- Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
 2. Typical limits are at $V_{CC} = 5.0\text{V}$, 25°C ambient and maximum loading.
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
 4. $\bar{E} = \text{GND}$, all other inputs and outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	$-65^\circ\text{C to } +150^\circ\text{C}$
Temperature (Ambient) Under Bias	$-55^\circ\text{C to } +125^\circ\text{C}$
Supply Voltage to Ground Potential Continuous	$-0.5\text{V to } +7.0\text{V}$
DC Voltage Applied to Outputs for High Output State	$-0.5\text{V to } +V_{CC \text{ max.}}$
DC Input Voltage	$-0.5\text{V to } +7.0\text{V}$
DC Output Current, Into Outputs	30mA
DC Input Current	$-30\text{mA to } +5.0\text{mA}$

SWITCHING CHARACTERISTICS

($T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
tPLH	A _i or B _i to Equal		9	15	ns	C _L = 15pF R _L = 2.0kΩ
tPHL			9	15		
tPLH	E to Equal		5	7	ns	
tPHL			6	8		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE *

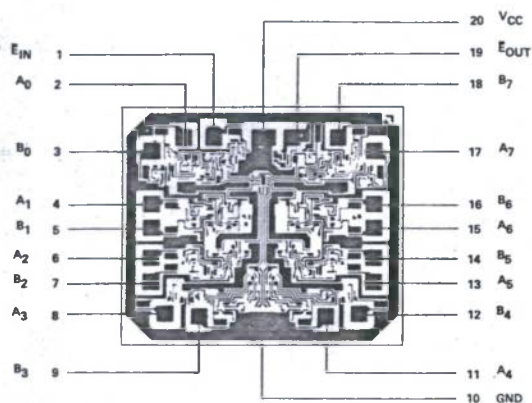
Parameters	Description	Min.	Max.	Min.	Max.	Units	Test Conditions
t_{PLH}	A_i or B_i to Equal Output		20		22	ns	$C_L = 50\text{pF}$ $R_L = 2.0\text{k}\Omega$
t_{PHL}			19		21		
t_{PLH}	E to Equal Output		10.5		12	ns	
t_{PHL}			12.5		15		

* AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

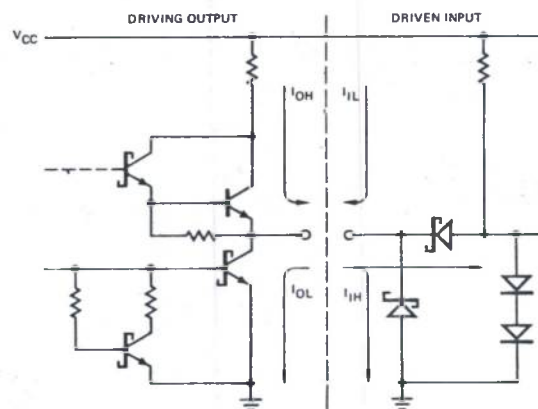
A_0-A_7	A input to comparator
B_0-B_7	B input to comparator
$\overline{E}_{IN}$	Enable active LOW
$\overline{E}_{OUT}$	EQUAL output active LOW

Metallization and Pad Layout



DIE SIZE 0.063" x 0.074"

Am25LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

DESCRIPTION

Model 40J was designed to fill the need for a low-cost general-purpose differential FET-input operational amplifier with a minimum of performance compromises. As will be seen in the table below, it turns out to be a "Best Buy" when its salient specifications are compared with those of two competitive discrete FET-input op amps, a "super-beta" I.C., and the 118A, a general-purpose bipolar-input modular operational amplifier.

Because of its low cost, Model 40J is a natural first choice for applications requiring FET-input amplifiers, or where marginal bias current specifications of available low-cost bipolars have in the past led to performance compromises for the sake of cost. This new low cost even makes it feasible to think in terms of stocking Model 40J, and buying bipolar-input types only for those exceptional cases where their characteristics are entirely adequate.

Where higher performance is required, Model 40K provides 20 pA of bias current and $20\mu\text{V}/^\circ\text{C}$ drift at only \$19.00 (1-9). For even more demanding applications, Analog Devices offers a broad line of FET op amps offering tighter specifications on key parameters. Examples are: Low voltage drift $2\mu\text{V}/^\circ\text{C}$ (Model 146), high common-mode rejection 40,000 (Model 143), ultra-fast response 0.8 and $1.5\mu\text{s}$ to 0.01% (Models 45 & 149), and miniature hybrid TO-8 construction (Model M501).

WHERE TO USE MODEL 40

FET op amps are usually the best choice when the amplifier's signal input comes from a high-impedance source (such as a photomultiplier), where extremely high input impedance is desired to minimize loading of a signal source (for example, measuring voltage across an unknown impedance), or for the measurement of very small currents. The benefits of FET op amps in these applications are manifest in two ways:

1. Input impedances are high. High input impedance is especially useful in such non-inverting applications as buffer amplifiers and moderate speed sample-holds, and in inverting applications requiring large values of feedback resistance, including integrators and differentiators for slowly-varying signals.

2. Bias currents are low. (Bias currents are the small leakage currents which flow through the input terminals). This allows accurate measurement of small currents, and also reduces that component of output voltage drift due to the voltage drop of bias current in feedback circuit resistors. It also allows the design of integrator circuits having low drifts and sample-hold circuits with excellent ability to retain charge. For example, in an integrator application at room temperature, employing Model 40J, the rate of leakage across a $1.0\mu\text{F}$ capacitor in HOLD will be less than $50 \times 10^{-12} / (1.0 \times 10^{-6}) = 50\mu\text{V}$ per second. That capacitor, if charged to +10V, would lose less than 0.1% of its charge (i.e., 10mV) in 200 seconds (assuming that the capacitor's own time constant were greater than 0.2 million seconds, circuit leakage resistance were better than $200\text{ k}\Omega$, etc.).

SALIENT SPECIFICATIONS OF TYPICAL ALTERNATIVES

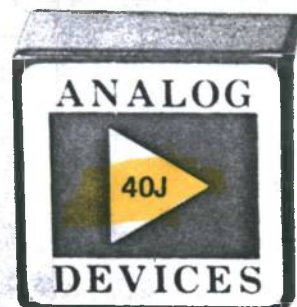
		40J	3308/12C*	QFT-5*	LM208*	118A
A_o , min, 10k load	V/V	200k typ.	200k no load	75k	50k	250k rated load
f_p , min.	kHz	100	100	50	2	100 (INV)
Output, rated	V@mA	$\pm 10 @ \pm 5$	$\pm 10 @ \pm 5$	$\pm 10 @ \pm 5$	$\pm 10 @ \pm 2$	$\pm 10 @ \pm 5$
$\Delta E_{os}/\Delta T$, max.	$\mu\text{V}/^\circ\text{C}$	± 50	± 50	± 300	± 15	± 20
I_b , max, 25°C .	pA	-50	-100	-100	3nA	+35nA
R_{in} , differential	ohms	10^{11}	10^{11}	10^{10}	7×10^7	10^6
Price (1-9) U.S. Dol.		\$12.00	\$11.90	\$12.00	\$40.00	\$11.00

*Published specifications available November, 1969

MODEL 40J/K GENERAL PURPOSE LOW COST FET OP-AMP

FEATURES

Voltage Drift	$\pm 50\mu\text{V}/^\circ\text{C}$ max
Bias Current	50pA max
Bandwidth	4MHz
Slew Rate	$6\text{V}/\mu\text{sec}$
Low Noise	$3\mu\text{V}$ rms
Low Cost (1-9)	\$12.00 (40J)



APPLICATIONS

High Impedance Buffer Amplifiers
Precision Integrators
Sample-and-Hold Circuits
Picoamp Current Measurements



221 FIFTH ST., CAMBRIDGE, MASS. 02142
TEL: 617/492-6000 TWX: 710/320-0326

Am26LS32 • Am26LS33

Quad Differential Line Receivers

DISTINCTIVE CHARACTERISTICS

- Input voltage range of 15V (differential or common mode) on Am26LS33; 7V (differential or common mode) on Am26LS32
- $\pm 0.2V$ sensitivity over the input voltage range on Am26LS32; $\pm 0.5V$ sensitivity on Am26LS33
- The Am26LS32 meets all the requirements of RS-422 and RS-423
- 6k minimum input impedance
- 30mV input hysteresis
- Operation from single +5V supply
- 16-pin hermetic and molded DIP package
- Fail safe input-output relationship. Output always high when inputs are open.
- Three-state drive, with choice of complementary output enables, for receiving directly onto a data bus.
- Propagation delay 17ns typical
- Available in military and commercial temperature range
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am26LS32 is a quad line receiver designed to meet the requirements of RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

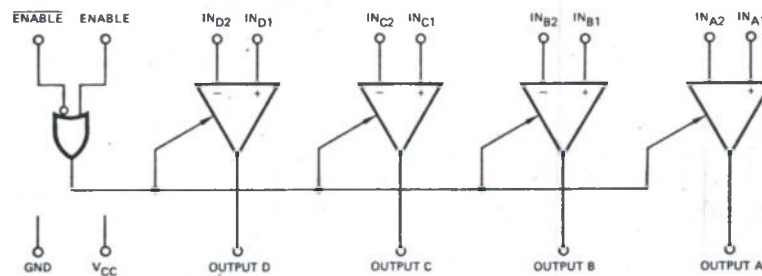
The Am26LS32 features an input sensitivity of 200mV over the input voltage range of $\pm 7V$.

The Am26LS33 features an input sensitivity of 500mV over the input voltage range of $\pm 15V$.

The Am26LS32 and Am26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-state outputs with 8mA sink capability and incorporate a fail safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32 and Am26LS33 are constructed using Advanced Low-Power Schottky processing.

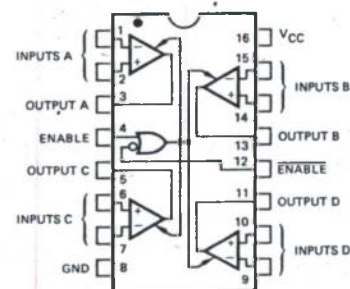
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Am26LS32	Am26LS33
		Order Number	Order Number
Hermetic DIP	-55°C to +125°C	AM26LS32DM	AM26LS33DM
Flat Pak	-55°C to +125°C	AM26LS32FM	AM26LS33FM
Dice	-55°C to +125°C	AM26LS32XM	AM26LS33XM
Hermetic DIP	0°C to +70°C	AM26LS32DC	AM26LS33DC
Molded DIP	0°C to +70°C	AM26LS32PC	AM26LS33PC
Dice	0°C to +70°C	AM26LS32XC	AM26LS33XC

CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orientation.

ABSOLUTE
Supply Volt
Common M
Differential
Enable Volt
Output Sink
Storage Tem

ELECTRI
The followi
Am26LS32X
Am26LS32X

Parameters

VTH
RIN
IIN
IIN
VOH
VOL
VIL
VIH
VI
IO
IIL
IIL
ISC
ICC
II
VHYST
PLH
PHL
ILZ
IHZ
IZL
IZH

Note: 1. All ty

L
FOR

FROM OUTPUT
UNDER TEST
C_L INCLUDES
PROBE AND JIG
CAPACITANCE

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

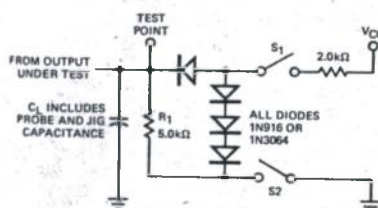
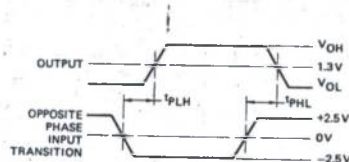
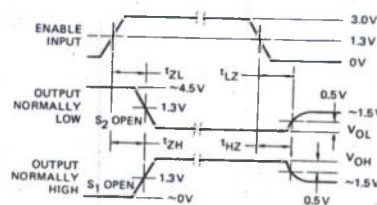
Supply Voltage	7.0V
Common Mode Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7.0V
Output Sink Current	50mA
Storage Temperature Range	-65°C to +165°C

ELECTRICAL CHARACTERISTICS Over the operating temperature range

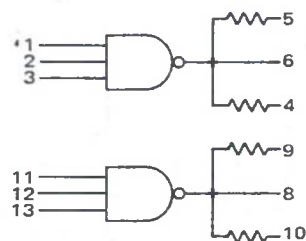
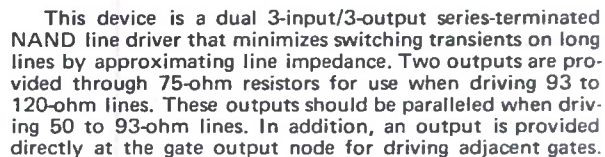
The following conditions apply unless otherwise specified:

Am26LS32XM, Am26LS33XM (MIL) $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$
 Am26LS32XC, Am26LS33XC (COM'L) $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 5\%$

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OL}$ or V_{OH} Am26LS32, $-7\text{V} < V_{CM} < +7\text{V}$ Am26LS33, $-15\text{V} < V_{CM} < +15\text{V}$	0.2 0.5	0.06 0.12	0.2 0.5	Volts
R_{IN}	Input Resistance	$-15\text{V} < V_{CM} < +15\text{V}$ (One input AC ground)	6.0k	8.5k		Ω
I_{IN}	Input Current (Under Test)	$V_{IN} = +15\text{V}$, Other Input $-15\text{V} < V_{IN} < +15\text{V}$			2.3	mA
I_{IN}	Input Current (Under Test)	$V_{IN} = -15\text{V}$, Other Input $-15\text{V} < V_{IN} < +15\text{V}$			-2.8	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$, $\Delta V_{IN} = +1.0\text{V}$ $V_{ENABLE} = 0.8\text{V}$, $I_{OH} = -440\mu\text{A}$ COM'L MIL	2.7 2.5	3.4 3.4		Volts
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$, $\Delta V_{IN} = -1.0\text{V}$ $V_{ENABLE} = 0.8\text{V}$ $I_{OL} = 4.0\text{mA}$ $I_{OL} = 8.0\text{mA}$			0.4 0.45	Volts
V_{IL}	Enable LOW Voltage				0.8	Volts
V_{IH}	Enable HIGH Voltage		2.0			Volts
V_I	Enable Clamp Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{mA}$			-1.5	Volts
I_O	Off-State (High Impedance) Output Current	$V_{CC} = \text{Max.}$ $V_O = 2.4\text{V}$ $V_O = 0.4\text{V}$			20 -20	mA
I_{IL}	Enable LOW Current	$V_{IN} = 0.4\text{V}$			-0.36	mA
I_{IH}	Enable HIGH Current	$V_{IN} = 2.7\text{V}$			20	μA
I_{SC}	Output Short Circuit Current	$V_O = 0\text{V}$, $V_{CC} = \text{Max.}$, $\Delta V_{IN} = +1.0\text{V}$	-15		-85	mA
I_{CC}	Power Supply Current	$V_{CC} = \text{Max.}$, All $V_{IN} = \text{GND}$, Outputs Disabled		52	70	mA
I_I	Input High Current	$V_{IN} = 5.5\text{V}$			100	μA
V_{HYST}	Input Hysteresis	$T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$, $V_{CM} = 0\text{V}$		30		mV
ϕ_{LH}	Input to Output	$T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$, $C_L = 15\text{pF}$, see test cond. below		17	25	ns
ϕ_{HL}	Input to Output	$T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$, $C_L = 15\text{pF}$, see test cond. below		17	25	ns
t_{LZ}	Enable to Output	$T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$, $C_L = 5\text{pF}$, see test cond. below		20	30	ns
t_{HZ}	Enable to Output	$T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$, $C_L = 5\text{pF}$, see test cond. below		15	22	ns
t_{ZL}	Enable to Output	$T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$, $C_L = 15\text{pF}$, see test cond. below		15	22	ns
t_{ZH}	Enable to Output	$T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$, $C_L = 15\text{pF}$, see test cond. below		15	22	ns

Note: 1. All typical values are $V_{CC} = 5.0\text{V}$, $T_A = 25^\circ\text{C}$.**LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS****PROPAGATION DELAY** (Notes 1 and 3)**ENABLE AND DISABLE TIMES** (Notes 2 and 3)**Notes:**

- Diagram shown for Enable LOW.
- S_1 and S_2 of Load Circuit are closed except where shown.
- Pulse Generator for All Pulses: Rate $< 1.0\text{MHz}$; $Z_0 = 50\Omega$; $t_r < 15\text{ns}$; $t_f < 6.0\text{ns}$.

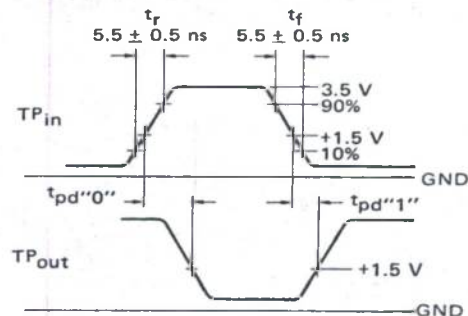


Negative Logic: $4, 5, 6 = \overline{1 + 2 + 3}$

Output Loading Factor, Direct Output (Pins 6 and 8) =
10 Minus The Number of Resistor-Terminated Outputs
Being Used.

Total Power Dissipation = 44 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

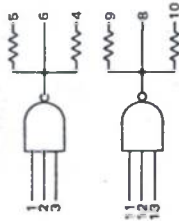
VOLTAGE WAVEFORMS AND DEFINITIONS



$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one line driver. The other line driver is tested in the same manner. Further, test procedures are shown for only one input of the line driver under test. To complete testing sequence through remaining inputs.



Characteristic		Symbol	Pin Under Test	MC3029 Test Limits						TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																							
				0°C			+25°C			+75°C			TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																				
				Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	I _{OL1A}	I _{OL1B}	I _{OL1C}	I _{OL2A}	I _{OL2B}	I _{OL2C}	I _{OLHA}	I _{OLHB}	I _{OLHC}	I _{OL}	I _{OL}	V _{IH}	V _R	V _{BH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}	V _{IHK}																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																		
Input	Forward Current	I _{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.



MOTOROLA Semiconductor Products Inc.

BOX 20912 • PHOENIX, ARIZONA 85036 • A SUBSIDIARY OF MOTOROLA INC.

General-Purpose Transistor Arrays

Monolithic Silicon

The CA3045 and CA3046 each consist of five general purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3045 and CA3046 are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

The CA3045 is supplied in an hermetic 14-lead Dual-In-Line ceramic package rated for operation over the full military temperature range.

The CA3046 is electrically identical to the CA3045 but is supplied in a dual-in-line plastic package for applications requiring only a limited temperature range.

APPLICATIONS

- General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.

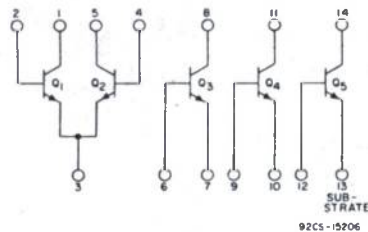
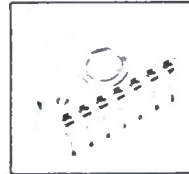
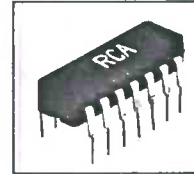


Fig.1 - Schematic diagram.



CA3045



CA3046

**THREE ISOLATED TRANSISTORS
AND ONE DIFFERENTIALLY-CONNECTED
TRANSISTOR PAIR**

For Low-Power Applications at Frequencies
from DC through the VHF Range

FEATURES

- Two matched pairs of transistors
 V_{BE} matched ± 5 mV
Input offset current $2 \mu A$ max. at $I_C = 1$ mA
- 5 general purpose monolithic transistors
- Operation from DC to 120 MHz
- Wide operating current range
- Low noise figure - - 3.2 dB typ. at 1 kHz
- Full military temperature range for CA3045
-55 to +125°C

ABSOLUT

Power Dis

 At T_A

 At T_A

 At T_A

 At T_A

 At T_A

Collector-

Collector-

Collector-

Emitter-to-

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Temperatu

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CA3046 i

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ELECTRICAL

Characteristics

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STATIC CHARACTERISTICS

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Collector-to-Emitte

Collector-to-Substr

Emitter-to-Base Br

Collector-Cutoff Cu

Collector-Cutoff Cu

Static Forward Curr

(Static Beta)

Input Offset Curren

 Q_1 and Q_2 , I_{IQ1}

Base-to-Emitter Vol

Magnitude of Input

 ential Pair $|V_{BE}$

Magnitude of Input

lated Transistor

 $|V_{BE4} - V_{BE5}|$

Temperature Coeffic

Base-to-Emitter Vol

Collector-to-Emitter

Temperature Coeffic

Magnitude of Input

ABSOLUTE MAXIMUM RATINGS AT $T_A = 25^\circ\text{C}$:

	CA3045		CA3046		
	Each Transistor	Total Package	Each Transistor	Total Package	
Power Dissipation:					
At $T_A = 25^\circ\text{C}$	300	750	300	750	mW
At $T_A = 25^\circ\text{C}$ to 55°C	-	-	300	750	mW
At $T_A > 55^\circ\text{C}$	-	-	Derate at 6.67		mW/ $^\circ\text{C}$
At $T_A = 25^\circ\text{C}$ to 75°C	300	750	-	-	mW
At $T_A > 75^\circ\text{C}$	Derate at 8		-	-	mW/ $^\circ\text{C}$
Collector-to-Emitter Voltage, V_{CE0} ..	15	-	15	-	V
Collector-to-Base Voltage, V_{CBO}	20	-	20	-	V
Collector-to-Substrate Voltage, V_{CIO}^* ..	20	-	20	-	V
Emitter-to-Base Voltage, V_{EBO}	5	-	5	-	V
Collector Current, I_C	50	-	50	-	mA
Temperature Range:					
Operating	-55 to +125		0 to +85		$^\circ\text{C}$
Storage	-65 to +150		-25 to +85		$^\circ\text{C}$

* The collector of each transistor of the CA3045 and CA3046 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected

to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

ELECTRICAL CHARACTERISTICS, at $T_A = 25^\circ\text{C}$

Characteristics apply for each transistor in the CA3045 and CA3046 as specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS			UNITS	CHARACTERISTIC CURVES
			Type CA3045 Type CA3046				
			MIN.	TYP.	MAX.		
STATIC CHARACTERISTICS							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10 \mu A, I_E = 0$	20	60	-	V	-
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1 \text{ mA}, I_B = 0$	15	24	-	V	-
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10 \mu A, I_{C1} = 0$	20	60	-	V	-
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10 \mu A, I_C = 0$	5	7	-	V	-
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10 \text{ V}, I_E = 0$	-	0.002	40	nA	2
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10 \text{ V}, I_B = 0$	-	See curve	0.5	μA	3
Static Forward Current-Transfer Ratio (Static Beta)	h_{FE}	$V_{CE} = 3 \text{ V} \begin{cases} I_C = 10 \text{ mA} \\ I_C = 1 \text{ mA} \\ I_C = 10 \mu A \end{cases}$	- 40 -	100 100 54	- - -	- - -	4
Input Offset Current for Matched Pair Q_1 and Q_2 : $ I_{O1} - I_{O2} $		$V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$	-	0.3	2	μA	5
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 3 \text{ V} \begin{cases} I_E = 1 \text{ mA} \\ I_E = 10 \text{ mA} \end{cases}$	- -	0.715 0.800	- -	V	6
Magnitude of Input Offset Voltage for Differ- ential Pair $ V_{BE1} - V_{BE2} $		$V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$	-	0.45	5	mV	6,8
Magnitude of Input Offset Voltage for Iso- lated Transistors $ V_{BE3} - V_{BE4} $, $ V_{BE4} - V_{BE5} $, $ V_{BE5} - V_{BE3} $		$V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$	-	0.45	5	mV	6,8
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	$V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$	-	-1.9	-	mV/ $^{\circ}C$	7
Collector-to-Emitter Saturation Voltage	V_{CES}	$I_B = 1 \text{ mA}, I_C = 10 \text{ mA}$	-	0.23	-	V	-
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{ \Delta V_{IO} }{\Delta T}$	$V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$	-	1.1	-	$\mu V/^{\circ}C$	8

ELECTRICAL CHARACTERISTICS (Cont'd.)

DYNAMIC CHARACTERISTICS							
Low-Frequency Noise Figure	NF	$f = 1 \text{ kHz}, V_{CE} = 3 \text{ V}, I_C = 100 \mu\text{A}$ Source Resistance = $1 \text{ k}\Omega$	-	3.25	-	dB	9(b)
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:							
Forward Current-Transfer Ratio	h_{fe}	$f = 1 \text{ kHz}, V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$	-	110	-	-	10
Short-Circuit Input Impedance	h_{ie}		-	3.5	-	$\text{k}\Omega$	
Open-Circuit Output Impedance	h_{oe}		-	15.6	-	μmho	
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	1.8×10^{-4}	-	-	
Admittance Characteristics:							
Forward Transfer Admittance	Y_{fe}	$f = 1 \text{ MHz}, V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$	-	$31-j1.5$	-	-	11
Input Admittance	Y_{ie}		-	$0.3+j0.04$	-	-	12
Output Admittance	Y_{oe}		-	$0.001+j0.03$	-	-	13
Reverse Transfer Admittance	Y_{re}		-	See curve	-	-	14
Gain-Bandwidth Product	f_T	$V_{CE} = 3 \text{ V}, I_C = 3 \text{ mA}$	300	550	-	-	15
Emitter-to-Base Capacitance	C_{EB}	$V_{EB} = 3 \text{ V}, I_E = 0$	-	0.6	-	pF	-
Collector-to-Base Capacitance	C_{CB}	$V_{CB} = 3 \text{ V}, I_C = 0$	-	0.58	-	pF	-
Collector-to-Substrate Capacitance	C_{CI}	$V_{CS} = 3 \text{ V}, I_C = 0$	-	2.8	-	pF	-

STATIC CHARACTERISTICS

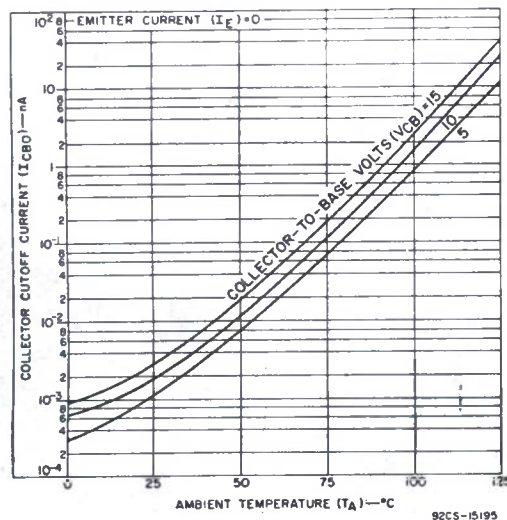


Fig.2 - Typical collector-to-base cutoff current vs ambient temperature for each transistor.

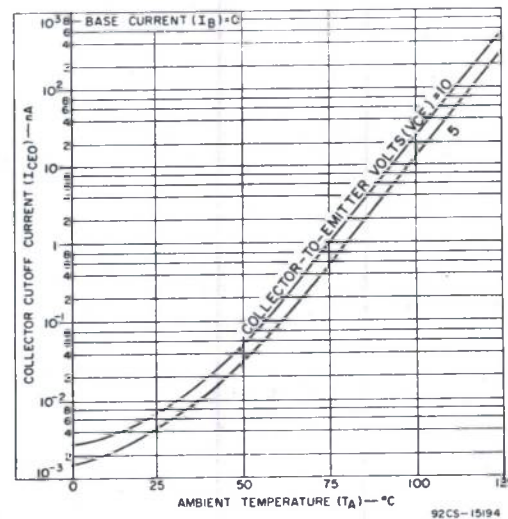


Fig.3 - Typical collector-to-emitter cutoff current vs ambient temperature for each transistor.

STATIC FORWARD CURRENT - TRANSFER RATIO (h_{FE})

120
110
100
90
80
70
60
50
40
30
20
10
0

Fig.4 - beta at

BASE-TO-EMITTER VOLTS (V_{BE})

0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0

Fig.6 - 1
istic a
pai

INPUT OFFSET MILLIVOLTS (V_{IO})

0.7
0.6
0.5
0.4
0.3
0.2
0.1
0

Transistor Array

Monolithic Silicon

The CA3026 and CA3054 each consists of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six n-p-n transistors which comprise the amplifiers are general purpose devices which exhibit low $1/f$ noise and a value of f_T in excess of 300 MHz. These features make the CA3026 and CA3054 useful from dc to 120 MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3026 and CA3054 provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual channel applications where matched performance of the two channels is required.

The CA3026 is supplied in a hermetic 12-lead TO-5 style package and is rated for full military operating-temperature range of -55°C to $+125^{\circ}\text{C}$.

The CA3054 is supplied in a 14-lead plastic Dual-in-line package with a limited temperature range. The availability of extra terminals allows the introduction of an independent substrate connection for maximum flexibility.

APPLICATIONS

- Dual sense amplifiers
- Dual Schmitt triggers
- Multifunction combinations -- RF Mixer, Oscillator, Converter, IF
- IF amplifiers (differential and/or cascode)
- Product detectors
- Doubly balanced modulators and demodulators
- Balanced quadrature detectors
- Cascode limiters
- Synchronous detectors
- Pairs of balanced mixers
- Synthesizer mixers
- Balanced (push-pull) cascode amplifiers

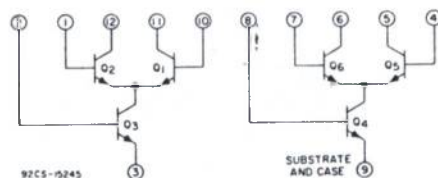


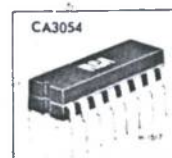
Fig. 1a - Schematic Diagram for CA3026.

**DUAL INDEPENDENT
DIFFERENTIAL AMPLIFIERS**

For Low-Power Applications
at Frequencies from DC
to 120 MHz



12-Lead TO-5


 14-Lead
Dual-In-Line
Plastic Package

FEATURES

- Two differential amplifiers on a common substrate
- Independently accessible inputs and outputs
- Maximum input offset voltage -- ± 5 mV
- Full military temperature range capability -- -55°C to $+125^{\circ}\text{C}$
- Limited temperature range -- 0°C to 85°C for CA3054

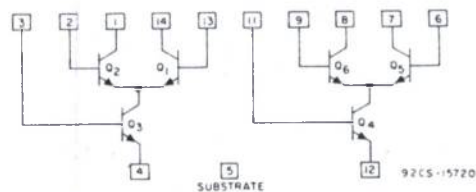


Fig. 1b - Schematic Diagram for CA3054.

CAUTION: Substrate **MUST** be maintained negative with respect to all collector terminals of this device. See Maximum Voltage Ratings chart.

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES, AT $T_A = 25^\circ\text{C}$

Power Dissipation, P:	CA3026	CA3054	
Any one transistor	300	300	mW
Total package	600	750	mW
For $T_A > 55^\circ\text{C}$	Derate at 5	6.67	mW/ $^\circ\text{C}$
Temperature Range:			
Operating	-55 to +125	-40 to +85	$^\circ\text{C}$
Storage	-65 to +150	-65 to +150	$^\circ\text{C}$

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CISO}^*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

* The collector of each transistor of the CA3026 and CA3054 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide

for normal transistor action. The substrate should be maintained at signal (AC) ground by means of a suitable grounding capacitor, to avoid undesired coupling between transistors.

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 1[†] and horizontal terminal 3[†] is +15 to -5 volts.

[†] For CA3026; corresponding terminals for CA3054 are vertical terminal 2 and horizontal terminal 4.

CA3054 TERMINAL No.	→	13	14	1	2	3	4	6	7	8	9	11	12	5
↓	CA3026 TERMINAL No.	10	11	12	1	2	3	4	5	6	7	8	Note 1 9	Note 1 9
13	10		0 -20	*	+5 -5	*	+15 -5	*	*	*	*	*	*	*
14	11			*	*	*	+20 0	*	*	*	*	*	*	+20 0
1	12				+20 0	*	+20 0	*	*	*	*	*	*	+20 0
2	1					*	+15 -5	*	*	*	*	*	*	*
3	2						+1 -5	*	*	*	*	*	*	*
4	3							*	*	*	*	*	*	*
6	4							0 -20	*	+5 -5	*	+15 -5	*	*
7	5								*	*	*	*	*	+20 0
8	6									+20 0	*	*	*	+20 0
9	7										*	+15 -5	*	*
11	8											+1 -5	*	*
12	9													*
5	9													Ref Sub- strate

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

Note 1: In the CA3026 terminal No.9 is connected to the emitter of Q_4 , the reference substrate, and the case; therefore, the case should not be grounded. Two terminal 9 columns (CA3026) appear in the voltage rating chart because it is a composite chart for both the CA3026 and the CA3054. Wherever an asterisk is shown in one column 9 and a rating is shown in the other column 9, the asterisk should be ignored.

Maximum Current Ratings

CA3054 TERMINAL No.	CA3026 TERMINAL No.	I_{IN} mA	I_{OUT} mA
13	10	5	0.1
14	11	50	0.1
1	12	50	0.1
2	1	5	0.1
3	2	5	0.1
4	3	0.1	-50
6	4	5	0.1
7	5	50	0.1
8	6	50	0.1
9	7	5	0.1
11	8	5	0.1
12	9	0.1	50

* Terminal No.10 of CA3054 is not used

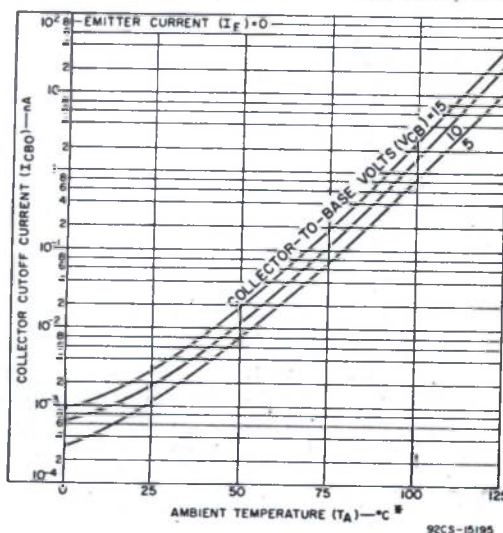
ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIRCUIT	CA3026 CA3054 LIMITS			UNITS	TYPICAL CHARACTERISTICS CURVES
			FIG.	MIN.	TYP.	MAX.		FIG.
STATIC CHARACTERISTICS								
For Each Differential Amplifier								
Input Offset Voltage	V_{IO}	$V_{CB} = 3\text{ V}$ $I_{E(Q3)} = I_{E(Q4)} = 2\text{ mA}$	-	-	0.45	5	mV	6
Input Offset Current	I_{IO}		-	-	0.3	2	μA	7
Input Bias Current	I_I		-	-	10	24	μA	3
Quiescent Operating Current Ratio	$\frac{I_{C(Q1)} \text{ or } I_{C(Q2)}}{I_{C(Q3)} \text{ or } I_{C(Q4)}}$		-	-	0.98 to 1.02	-	-	3
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{ \Delta V_{IO} }{\Delta T}$		-	-	1.1	-	$\mu\text{V}/^\circ\text{C}$	5
For Each Transistor								
DC Forward Base-to-Emitter Voltage	V_{BE}	$V_{CB} = 3\text{ V}$ $I_C = 50\text{ }\mu\text{A}$ 1 mA 3 mA 10 mA	-	-	0.630 0.715 0.750 0.800	0.700 0.800 0.850 0.900	V	6
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	$V_{CB} = 3\text{ V}, I_C = 1\text{ mA}$	-	-	-1.9	-	$\mu\text{V}/^\circ\text{C}$	4
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10\text{ V}, I_E = 0$	-	-	0.002	100	nA	2
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1\text{ mA}, I_B = 0$	-	15	24	-	V	-
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\text{ }\mu\text{A}, I_E = 0$	-	20	60	-	V	-
Collector-to-Substrate Breakdown Voltage	$V_{(BR)C10}$	$I_C = 10\text{ }\mu\text{A}, I_{C1} = 0$	-	20	60	-	V	-
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\text{ }\mu\text{A}, I_C = 0$	-	5	7	-	V	-
DYNAMIC CHARACTERISTICS								
Common-Mode Rejection Ratio For Each Amplifier	CMR	$V_{CC} = 12\text{ V}$ $V_{EE} = -6\text{ V}$ $V_x = -3.3\text{ V}$ $f = 1\text{ kHz}$	8a	-	100	-	dB	8b
AGC Range, One Stage	AGC		9a	-	75	-	dB	9b
Voltage Gain, Single Stage Double-Ended Output	A		9a	-	32	-	dB	9b
AGC Range, Two Stage	AGC		10a	-	105	-	dB	10b
Voltage Gain, Two Stage Double-Ended Output	A		10a	-	60	-	dB	10b
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: (For Single Transistor)								
Forward Current-Transfer Ratio	h_{fe}	$f = 1\text{ kHz}, V_{CE} = 3\text{ V}, I_C = 1\text{ mA}$	-	-	110	-	-	11
Short-Circuit Input Impedance	h_{ie}		-	-	3.5	-	k Ω	11
Open-Circuit Output Impedance	h_{oe}		-	-	15.6	-	μmho	11
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	-	1.8×10^{-4}	-	-	11

DYNAMIC CHARACTERISTICS CONT'D.

1/f Noise Figure (For Single Transistor)	NF	$f = 1 \text{ kHz}, V_{CE} = 3 \text{ V}$	-	-	3.25	-	dB	-
Gain-Bandwidth Product (For Single Transistor)	f_T	$V_{CE} = 3 \text{ V}, I_C = 3 \text{ mA}$	-	-	550	-	MHz	12
Admittance Characteristics; Differential Circuit Configuration: (For Each Amplifier)								
Forward Transfer Admittance	y_{21}	$V_{CB} = 3 \text{ V}$ Each Collector $I_C \approx 1.25 \text{ mA}$ $f = 1 \text{ MHz}$	-	-	$-20 + j0$	-	mmho	13a
Input Admittance	y_{11}		-	-	$0.22 + j0.1$	-	mmho	13b
Output Admittance	y_{22}		-	-	$0.01 + j0$	-	mmho	13c
Reverse Transfer Admittance	y_{12}		-	-	$-0.003 + j0$	-	mmho	13d
Admittance Characteristics; Cascode Circuit Configuration: (For Each Amplifier)								
Forward Transfer Admittance	y_{21}	$V_{CB} = 3 \text{ V}$ Total Stage $I_C \approx 2.5 \text{ mA}$ $f = 1 \text{ MHz}$	-	-	$68 - j0$	-	mmho	14a
Input Admittance	y_{11}		-	-	$0.55 + j0$	-	mmho	14b
Output Admittance	y_{22}		-	-	$0 + j0.02$	-	mmho	14c
Reverse Transfer Admittance	y_{12}		-	-	$0.004 - j0.005$	-	μmho	14d
Noise Figure	NF	$f = 100 \text{ MHz}$	-	-	8	-	dB	-

TYPICAL STATIC CHARACTERISTICS



* For CA3054: use data from 0°C to 85°C only

Fig.2 - Collector-to-base cutoff current vs ambient temperature for each transistor.

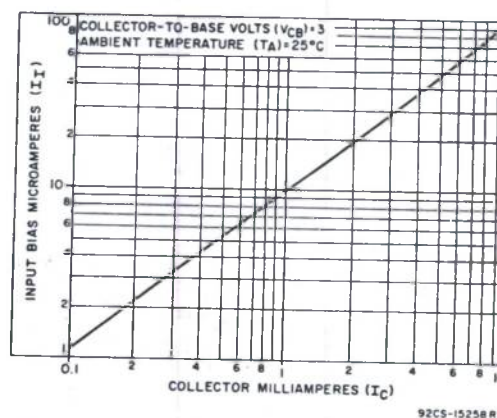


Fig.3 - Input bias current characteristic vs collector current for each transistor.



LM117/LM217/LM317 3-terminal adjustable regulator

general description

The LM117/LM217/LM317 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5A over a 1.2V to 37V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM117 is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM117 series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

features

- Adjustable output down to 1.2V
- Guaranteed 1.5A output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- 100% electrical burn-in
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection

Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejections ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM117 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117 can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

The LM117K, LM217K and LM317K are packaged in standard TO-3 transistor packages while the LM117H, LM217H and LM317H are packaged in a solid Kovar base TO-5 transistor package. The LM117 is rated for operation from -55°C to $+150^{\circ}\text{C}$, the LM217 from -25°C to $+150^{\circ}\text{C}$ and the LM317 from 0°C to $+125^{\circ}\text{C}$. The LM317T and LM317MP, rated for operation over a 0°C to $+125^{\circ}\text{C}$ range, are available in a TO-220 plastic package and a TO-202 package, respectively.

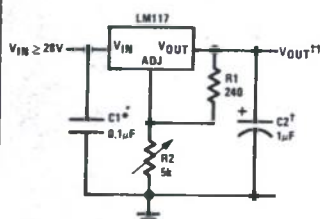
For applications requiring greater output current in excess of 3A and 5A, see LM150 series and LM138 series data sheets, respectively. For the negative complement, see LM137 series data sheet.

LM117 Series Packages and Power Capability

DEVICE	PACKAGE	RATED POWER DISSIPATION	DESIGN LOAD CURRENT
LM117	TO-3	20W	1.5A
LM217 LM317	TO-5	2W	0.5A
LM317T	TO-220	15W	1.5A
LM317M	TO-202	7.5W	0.5A

typical applications

1.2V–25V Adjustable Regulator

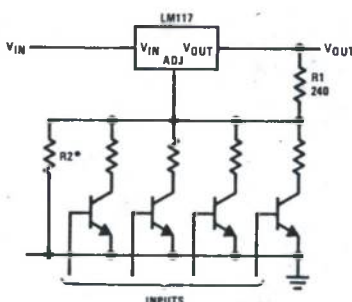


†Optional—improves transient response

*Needed if device is far from filter capacitors

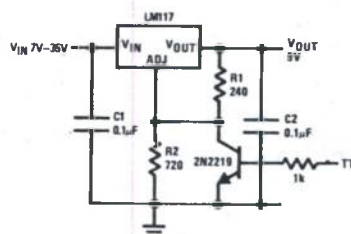
$$\dagger\dagger V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right)$$

Digitally Selected Outputs



*Sets maximum V_{OUT}

5V Logic Regulator with Electronic Shutdown*



*Min output $\approx 1.2V$

absolute maximum ratings

Power Dissipation	Internally limited
Input-Output Voltage Differential	40V
Operating Junction Temperature Range	
LM117	-55°C to +150°C
LM217	-25°C to +150°C
LM317	0°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

preconditioning

Burn-In in Thermal Limit	100% All Devices
--------------------------	------------------

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	LM117/217			LM317			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Line Regulation	$T_A = 25^\circ\text{C}$, $3\text{V} \leq V_{\text{IN}} - V_{\text{OUT}} \leq 40\text{V}$ (Note 2)		0.01	0.02		0.01	0.04	%/V
Load Regulation	$T_A = 25^\circ\text{C}$, $10\text{mA} \leq I_{\text{OUT}} \leq I_{\text{MAX}}$							
	$V_{\text{OUT}} \leq 5\text{V}$, (Note 2)		5	15		5	25	mV
	$V_{\text{OUT}} \geq 5\text{V}$, (Note 2)		0.1	0.3		0.1	0.5	%
Thermal Regulation	$T_A = 25^\circ\text{C}$, 20 ms Pulse		0.03	0.07		0.04	0.07	%/W
Adjustment Pin Current			50	100		50	100	μA
Adjustment Pin Current Change	$10\text{mA} \leq I_L \leq I_{\text{MAX}}$ $2.5\text{V} \leq (V_{\text{IN}} - V_{\text{OUT}}) \leq 40\text{V}$		0.2	5		0.2	5	μA
Reference Voltage	$3 \leq (V_{\text{IN}} - V_{\text{OUT}}) \leq 40\text{V}$, (Note 3) $10\text{mA} \leq I_{\text{OUT}} \leq I_{\text{MAX}}$, $P \leq P_{\text{MAX}}$	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation	$3\text{V} \leq V_{\text{IN}} - V_{\text{OUT}} \leq 40\text{V}$, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	$10\text{mA} \leq I_{\text{OUT}} \leq I_{\text{MAX}}$, (Note 2)							
	$V_{\text{OUT}} \leq 5\text{V}$		20	50		20	70	mV
	$V_{\text{OUT}} \geq 5\text{V}$		0.3	1		0.3	1.5	%
Temperature Stability	$T_{\text{MIN}} \leq T_j \leq T_{\text{MAX}}$		1			1		%
Minimum Load Current	$V_{\text{IN}} - V_{\text{OUT}} = 40\text{V}$		3.5	5		3.5	10	mA
Current Limit	$V_{\text{IN}} - V_{\text{OUT}} \leq 15\text{V}$							
	K and T Package	1.5	2.2		1.5	2.2		A
	H and P Package	0.5	0.8		0.5	0.8		A
	$V_{\text{IN}} - V_{\text{OUT}} = 40\text{V}$							
	K and T Package		0.4			0.4		A
	H and P Package		0.07			0.07		A
RMS Output Noise, % of V_{OUT}	$T_A = 25^\circ\text{C}$, $10\text{Hz} \leq f \leq 10\text{kHz}$		0.003			0.003		%
Ripple Rejection Ratio	$V_{\text{OUT}} = 10\text{V}$, $f = 120\text{Hz}$		65			65		dB
	$\text{CADJ} = 10\mu\text{F}$	66	80		66	80		dB
Long-Term Stability	$T_A = 125^\circ\text{C}$		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	H Package		12	15		12	15	$^\circ\text{C/W}$
	K Package		2.3	3		2.3	3	$^\circ\text{C/W}$
	T Package					4		$^\circ\text{C/W}$
	P Package					12		$^\circ\text{C/W}$

Note 1: Unless otherwise specified, these specifications apply: $-55^\circ\text{C} \leq T_j \leq +150^\circ\text{C}$ for the LM117, $-25^\circ\text{C} \leq T_j \leq +150^\circ\text{C}$ for the LM217 and $0^\circ\text{C} \leq T_j \leq +125^\circ\text{C}$ for the LM317; $V_{\text{IN}} - V_{\text{OUT}} = 5\text{V}$ and $I_{\text{OUT}} = 0.1\text{A}$ for the TO-5 and TO-202 packages and $I_{\text{OUT}} = 0.5\text{A}$ for the TO-3 package and TO-220 package. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-5 and TO-202 and 20W for the TO-3 and TO-220. I_{MAX} is 1.5A for the TO-3 and TO-220 package and 0.5A for the TO-5 and TO-202 package.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

Note 3: Selected devices with tightend tolerance reference voltage available.



**National
Semiconductor**

Voltage Comparators

LM119/LM219/LM319 High Speed Dual Comparator

General Description

The LM119 series are precision high speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the LM710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25 mA. Outstanding features include:

Features

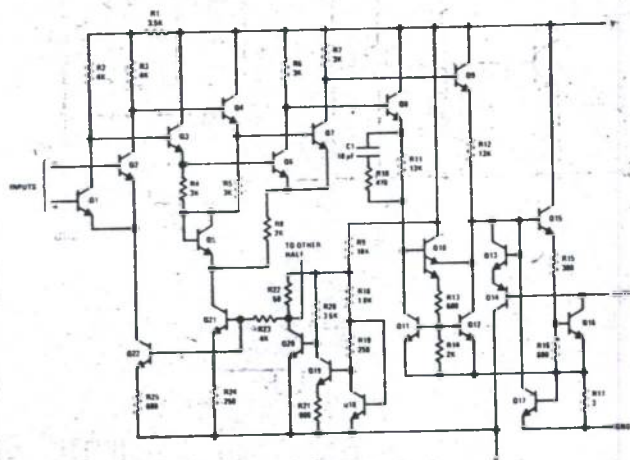
- Two independent comparators
- Operates from a single 5V supply
- Typically 80 ns response time at $\pm 15V$
- Minimum fan-out of 2 each side

- Maximum input current of $1 \mu A$ over temperature
- Inputs and outputs can be isolated from system ground
- High common mode slew rate

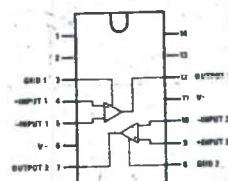
Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to $\pm 15V$. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the LM711.

The LM119 is specified from $-55^{\circ}C$ to $+125^{\circ}C$, the LM219 is specified from $-25^{\circ}C$ to $+85^{\circ}C$, and the LM319 is specified from $0^{\circ}C$ to $+70^{\circ}C$.

Schematic and Connection Diagrams



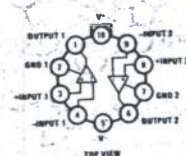
Dual-In-Line-Package



Order Number LM319N
See NS Package N14A

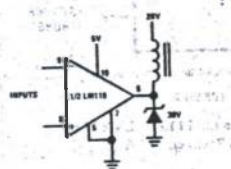
Order Number LM119J, LM219J
or LM319J
See NS Package J14A

Metal Can Package

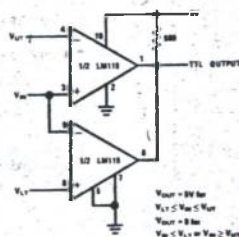


Order Number LM119H, LM219H
or LM319H
See NS Package H10C

Typical Applications



Relay Driver



Window Detector

Absolute Maximum Ratings LM319

Total Supply Voltage	36V	Power Dissipation (Note 2)	500 mW
Output to Negative Supply Voltage	36V	Output Short Circuit Duration	10 sec
Ground to Negative Supply Voltage	25V	Operating Temperature Range LM319	0°C to 70°C
Ground to Positive Supply Voltage	18V	Storage Temperature Range	-65°C to 150°C
Differential Input Voltage	±5V	Lead Temperature (Soldering, 10 sec)	300°C
Input Voltage (Note 1)	±15V		

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25^\circ\text{C}$, $R_S \leq 5k$		2.0	8.0	mV
Input Offset Current (Note 4)	$T_A = 25^\circ\text{C}$		80	200	nA
Input Bias Current	$T_A = 25^\circ\text{C}$		250	1000	nA
Voltage Gain	$T_A = 25^\circ\text{C}$	8	40		V/mV
Response Time (Note 5)	$T_A = 25^\circ\text{C}$, $V_S = \pm 15V$		80		ns
Saturation Voltage	$V_{IN} \leq -10\text{ mV}$, $I_{OUT} = 25\text{ mA}$ $T_A = 25^\circ\text{C}$		0.75	1.5	V
Output Leakage Current	$V_{IN} \geq 10\text{ mV}$, $V_{OUT} = 35V$, $V^- = V_{GND} = 0V$, $T_A = 25^\circ\text{C}$		0.2	10	μA
Input Offset Voltage (Note 4)	$R_S \leq 5k$			10	mV
Input Offset Current (Note 4)				300	nA
Input Bias Current				1200	nA
Input Voltage Range	$V_S = \pm 15V$ $V^+ = 5V$, $V^- = 0$	1	±13	3	V
Saturation Voltage	$V^- \geq 4.5V$, $V^+ = 0$ $V_{IN} \leq -10\text{ mV}$, $I_{SINK} \leq 3.2\text{ mA}$		0.3	0.4	V
Differential Input Voltage				±5	V
Positive Supply Current	$T_A = 25^\circ\text{C}$, $V^+ = 5V$, $V^- = 0$		4.3		mA
Positive Supply Current	$T_A = 25^\circ\text{C}$, $V_S = \pm 15V$		8	12.5	mA
Negative Supply Current	$T_A = 25^\circ\text{C}$, $V_S = \pm 15V$		3	5	mA

Note 1: For supply voltages less than $\pm 15V$ the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum junction temperature of the LM319 is 85°C . For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W , junction to ambient, or 45°C/W , junction to case. The thermal resistance of the dual-in-line package is 100°C/W , junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to $\pm 15V$ supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

LM124/LM224/LM324, LM124A/LM224A/LM324A, LM2902

Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ± 15 V_{DC} power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

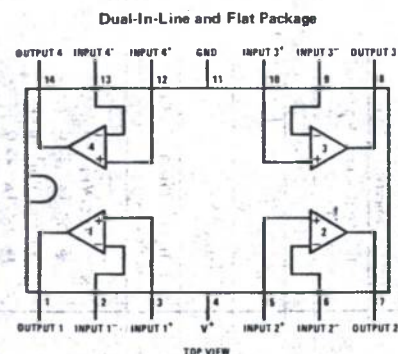
Advantages

- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
 - Single supply 3 V_{DC} to 30 V_{DC}
 - or dual supplies ± 1.5 V_{DC} to ± 15 V_{DC}
- Very low supply current drain (800 μ A) — essentially independent of supply voltage (1 mW/op amp at +5 V_{DC})
- Low input biasing current 45 nA_{DC} (temperature compensated)
- Low input offset voltage 2 mV_{DC} and offset current 5 nA_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V_{DC} to V* - 1.5 V_{DC}

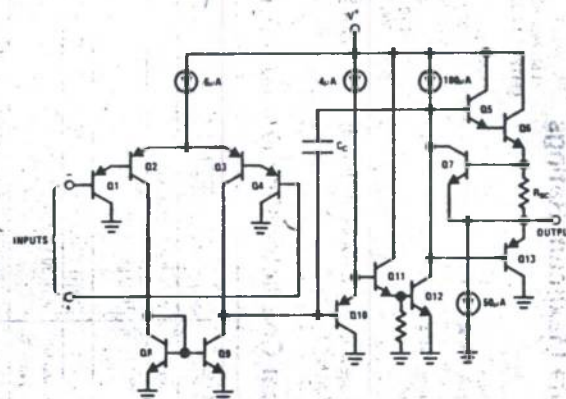
Connection Diagram



Order Number LM124J, LM124AJ,
LM224J, LM224AJ, LM324J,
LM324AJ or LM2902J
See NS Package J14A

Order Number LM324N, LM324AN
or LM2902N
See NS Package N14A

Schematic Diagram (Each Amplifier)



LM124/LM224/LM324, LM124A/LM224A/LM324A, LM2902

Absolute Maximum Ratings

PARAMETER	CONDITIONS	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+		32 VDC or ± 16 VDC	26 VDC or ± 13 VDC	50 mA	50 mA
Differential Input Voltage		32 VDC	26 VDC	0°C to +70°C	-40°C to +85°C
Input Voltage		-0.3 VDC to +26 VDC	-0.3 VDC to +26 VDC	-25°C to +85°C	-65°C to +150°C
Power Dissipation (Note 1)		570 mW	570 mW	0°C to +70°C	0°C to +70°C
Molded DIP		900 mW	800 mW	-25°C to +85°C	-25°C to +85°C
Cavity DIP		800 mW	Continuous	-55°C to +125°C	-55°C to +125°C
Flat Pack		Continuous	Continuous	-65°C to +150°C	-65°C to +150°C
Output Short-Circuit to GND (One Amplifier) (Note 2)				300°C	300°C
$V^- \leq 15$ VDC and $T_A = 25^\circ\text{C}$					

Electrical Characteristics ($V^+ = +5.0$ VDC, Note 4)

PARAMETER	CONDITIONS	LM124A	LM224A	LM324A	LM124/LM224	LM324	LM2902	UNITS
Input Offset Voltage	$T_A = 25^\circ\text{C}$, (Note 5)	1	2	3	2	3	2	mV
Input Bias Current (Note 6)	$I_{IN(+)} \text{ or } I_{IN(-)}$, $T_A = 25^\circ\text{C}$	20	50	80	45	100	45	nADC
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25^\circ\text{C}$	2	10	15	5	30	5	nADC
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30$ VDC, $T_A = 25^\circ\text{C}$	0	$V^+ - 1.5$	$V^+ - 1.5$	0	$V^+ - 1.5$	0	VDC
Supply Current	$R_L = \infty$, $V_{CC} = 30$ V, (LM2902 $V_{CC} = 26$ V) $R_L = \infty$ On All Op Amps Over Full Temperature Range	1.5	3	3	1.5	3	1.5	3
		0.7	1.2	1.2	0.7	1.2	0.7	1.2
Large Signal Voltage Gain	$V^+ = 15$ VDC (For Large V_O Swing) $R_L \geq 2$ k Ω , $T_A = 25^\circ\text{C}$	50	100	100	50	100	50	100
Output Voltage Swing	$R_L = 2$ k Ω , $T_A = 25^\circ\text{C}$ (LM2902 $R_L \geq 10$ k Ω)	0	$V^+ - 1.5$	$V^+ - 1.5$	0	$V^+ - 1.5$	0	$V^+ - 1.5$
Common-Mode Rejection Ratio	DC, $T_A = 25^\circ\text{C}$	70	85	85	70	85	70	85
Power Supply Rejection Ratio	DC, $T_A = 25^\circ\text{C}$	65	100	100	65	100	65	100
Amplifier-to-Amplifier Coupling (Note 8)	$f = 1$ kHz to 20 kHz, $T_A = 25^\circ\text{C}$ (Input Referred)	-120	-120	-120	-120	-120	-120	-120
Output Current Source	$V_{IN}^+ = 1$ VDC, $V_{IN}^- = 0$ VDC, $V^+ = 15$ VDC, $T_A = 25^\circ\text{C}$	20	40	40	20	40	20	40
Sink	$V_{IN}^+ = 1$ VDC, $V_{IN}^- = 0$ VDC, $V^+ = 15$ VDC, $T_A = 25^\circ\text{C}$	10	20	20	10	20	10	20
	$V_{IN}^+ = 1$ VDC, $V_{IN}^- = 0$ VDC, $V^+ = 15$ VDC, $T_A = 25^\circ\text{C}$	12	50	50	12	50	12	50
	$V_{IN}^+ = 1$ VDC, $V_{IN}^- = 0$ VDC, $V^+ = 15$ VDC, $T_A = 25^\circ\text{C}$							

Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	LM124A	LM224A	LM324A	LM124/LM224	LM324	LM2902	UNITS
Input Offset Voltage (Note 5)		1	2	3	2	3	2	mV
Input Offset Voltage Drift	$R_S = 0\Omega$	7	20	20	7	20	7	mV/°C
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$							nADC

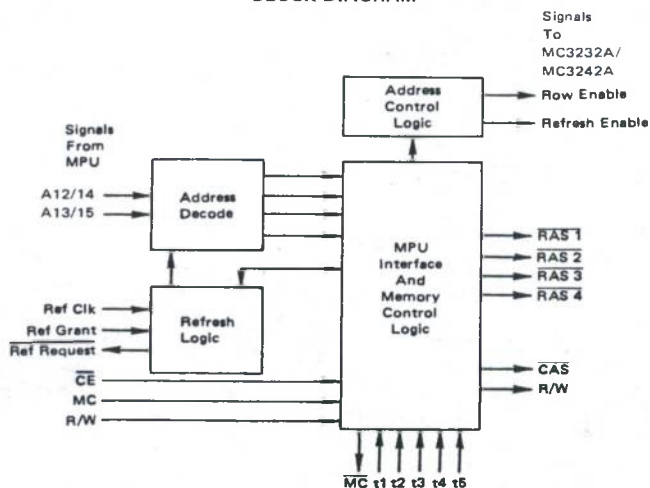
Specifications and Applications Information

MEMORY CONTROLLER FOR 16 PIN 4K, 16K AND 64K DYNAMIC RAMs

The memory controller chip is designed to greatly simplify the interface logic required to control the popular 16 pin multiplexed dynamic NMOS RAMs in a microprocessor system such as the M6800. The controller will generate, on command from the microprocessor, the proper timing signals required to successfully transfer data between the microprocessor and the NMOS memories. The controller, in conjunction with an oscillator, will also generate the necessary signals required to insure that the dynamic memories are refreshed for the retention of data.

- Greatly Simplify the MPU-Dynamic Memory Interface
- Reduce Package Count and System Access/Cycle Times 30%
- Chip Enable for Expansion to Larger Word Capacity
- Generate 1 of 4 RAS Signals for an Optimum 16K/64K Memory System
- High Input Impedance for Minimum Loading of MPU Bus
- Schottky TTL Technology for High Performance
- Useful with 4K and 16K and Future Expanded Dynamic RAMs

BLOCK DIAGRAM



Several methods may be employed to generate the required time delay:

1. One shots
2. High frequency counters
3. High frequency shift registers
4. Delay lines
5. Signals from MPU Clock

DYNAMIC MEMORY CONTROLLER

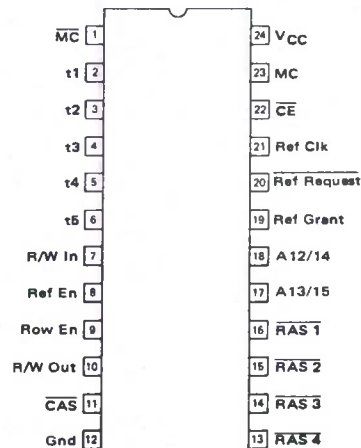
SCHOTTKY MONOLITHIC INTEGRATED CIRCUIT

L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 649

PIN CONNECTIONS



See Pin Descriptions

ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	-0.5 to +7.0	Vdc
Output Voltage	V_O	-0.5 to +7.0	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J		°C
Ceramic Package		175	
Plastic Package		150	

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

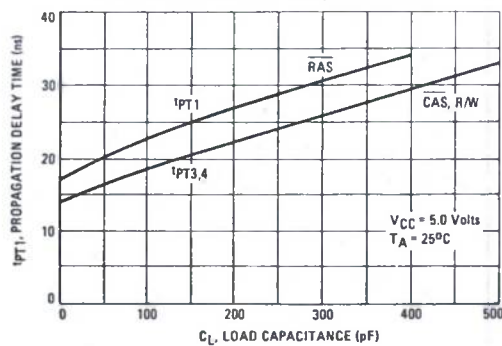
RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+4.50 to +5.50	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply over recommended power supply and temperature ranges.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — Low Logic State	V_{IL}	—	—	0.8	V
Input Voltage — High Logic State	V_{IH}	2.0	—	—	V
Input Current — Low Logic State ($V_{IL} = 0.5$ V)	I_{IL}	—	—	-250	μA
Input Current — High Logic State ($V_{IH} = 2.7$ V) ($V_{IH} = 5.5$ V)	I_{IH}	—	—	40 100	μA
Input Clamp Voltages ($I_{IK} = 18$ mA)	V_{IK}	—	—	-1.5	V
Output Voltage — Low Logic State ($I_{OL} = 24$ mA for RAS, CAS, and R/W) ($I_{OL} = 8.0$ mA for Row En, Ref En, MC, Ref Req)	V_{OL}	—	—	0.5 0.5	V
Output Voltage — High Logic State ($I_{OH} = -1.0$ mA for RAS, CAS, and R/W) ($I_{OH} = -0.4$ mA for Row En, Ref En, and MC) ($I_{OH} = -0.2$ mA for Ref Req (Note: Ref Req output has internal 5.0 k resistive pullup to V_{CC} .)	V_{OH}	3.0 2.4 2.4	— — —	— — —	V
Power Supply Current — During R/W or Refresh — During Idle	I_{CC}	—	—	65 40	mA
Output Short-Circuit Current ($V_{OL} = 0$ V for Row En, Ref En, and MC)	I_{OS}	-10	—	-55	mA

FIGURE 1 — TYPICAL $t_{PT1,3, \text{ and } 4}$ (HIGH TO LOW) versus LOAD CAPACITANCE — RAS, CAS and R/W



SWITCHING CHARACTERISTICS (Unless otherwise noted, $4.5 \leq V_{CC} \leq 5.5$ V, and $0 \leq T_A \leq 70^\circ\text{C}$)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times (Full AC Load — All Outputs)					
MC to $\overline{\text{MC}}$ — Low to High	$t_{PLH}(\overline{\text{MC}})$	—	—	14	ns
MC to $\overline{\text{MC}}$ — High to Low	$t_{PHL}(\overline{\text{MC}})$	—	—	17	
t1 to $\overline{\text{RAS}}$	t_{PT1}	18	—	40	
t2 to Row En	t_{PT2}	16	—	35	
t3 to $\overline{\text{CAS}}$	t_{PT3}	17	—	45	
t4 to R/W	t_{PT4}	16	—	45	
t5 to $\overline{\text{CAS}}$	t_{PT5C}	22	—	42	
to $\overline{\text{RAS}}$	t_{PT5R}	19	—	40	
to R/W	t_{PT5W}	30	—	58	
to Row En (Refresh)	t_{PT5ER}	30	—	65	
to Row En (R/W)	t_{PT5E}	25	—	48	
to Refresh En	t_{PT5F}	22	—	46	
Ref Clk to Ref Req	t_{PCQ}	10	—	27	
Ref Grant to Row En	t_{PGS}	20	—	43	
to Ref En					
t1 to Ref Req (Ref only)	t_{PTQ}	22	—	60	
Propagation Delay Times (AC Load, 15 pF — All Outputs)					
t1 to $\overline{\text{RAS}}$	t_{PT1}	10	—	30	ns
t2 to Row En	t_{PT2}	16	—	35	
t3 to $\overline{\text{CAS}}$	t_{PT3}	8.0	—	25	
t4 to R/W	t_{PT4}	8.0	—	25	
t5 to $\overline{\text{CAS}}$	t_{PT5C}	14	—	35	
to $\overline{\text{RAS}}$	t_{PT5R}	14	—	35	
to R/W	t_{PT5W}	22	—	45	
to Row En (Refresh)	t_{PT5ER}	30	—	65	
to Row En (R/W)	t_{PT5E}	25	—	48	
to Refresh En	t_{PT5F}	22	—	46	
Setup Times (Full AC Load — All Pins)					
Ref Clk before Ref Grant	$t_{su}(\text{RC})$	35	—	—	ns
A12, A13 before t1	$t_{su}(\text{A})$	10	—	—	
R/W Input before t4	$t_{su}(\text{R/W})$	33	—	—	
$\overline{\text{CE}}$ before t1	$t_{su}(\overline{\text{CE}})$	30	—	—	
Ref Grant before t1	$t_{su}(\text{RG})$	25	—	—	
Hold Times (Full AC Load — All Pins)					
A12, A13 after t5	$t_h(\text{A})$	15	—	—	ns
$\overline{\text{CE}}$ after t1	$t_h(\overline{\text{CE}})$	0	—	—	
R/W after t4	$t_h(\text{R/W})$	0	—	—	
MC Rising after t1 Rising	$t_h(\text{MC})$	30	—	—	
Minimum Delay Times (Note 2 — Full AC Load — All Pins)					
t1 Low to High to t2 Low to High	$t_d(1-2)$	30	—	—	ns
t1 Low to High to t4 Low to High	$t_d(1-4)$	33	—	—	
t2 Low to High to t3 Low to High	$t_d(2-3)$	30	—	—	
t3 Low to High to t5 Low to High	$t_d(3-5)$	30	—	—	
Minimum Pulse Widths					
t1 through t5					ns
Low	$t_{WL}(t)$	30	—	—	
High	$t_{WH}(t)$	30	—	—	
MC	$t_{W}(\text{MC})$	30	—	—	
Ref Grant	$t_{W}(\text{RG})$	25	—	—	

Note 2: If delays between t1—t5 are less than the minimum specified, the succeeding outputs may not switch.

AC LOADS (Note 3)

R/W and $\overline{\text{CAS}}$ Outputs	450 pF to Gnd*
RAS Outputs	150 pF to Gnd*
MC, Row En, Ref En, and Ref Req Outputs	15 pF to Gnd*

*Includes probe and jig capacitance.

NOTE 3: All outputs can drive larger capacitive loads than those shown with a small decrease in speed. See Figure 1.

PIN DESCRIPTION TABLE

Name	No.	Function
RAS1 RAS2 RAS3 RAS4	16 15 14 13	Row Address Strobe pins which connect to each of the dynamic RAMs to latch in row address on memory chips. Decoded to 1 of 4 during R/W cycle. All 4 go low during refresh cycle.
CAS	11	Column Address Strobe pin which connects to each dynamic RAM to latch in column address.
R/W Out	10	This pin signals the dynamic RAM whether the RAM is to be read from or written into.
Row En	9	Row Enable output which goes to the MC3232A (MC3242A). It signals the Address Multiplexer that the lower half (Row Addresses) or the upper half (Column Addresses) of the address lines are to be multiplexed into the dynamic RAM address inputs. A Logic 1 on this output indicates the Row Addresses, and a Logic 0 indicates Column Addresses.
Ref En	8	Refresh Enable output. A Logic 1 signals the Address Multiplexer that a refresh cycle is to be done, and a Logic 0 indicates that address multiplexing should be done.
CE	22	Chip Enable Input. A Logic 1 on this pin disables all chip functions, except that of Refresh and the MC output. CE must be low during t1 low to high transition to initiate R/W cycle. Once t1 is initiated, the cycle is independent of CE.
R/W In	7	The Read/Write input pin receives information from the M6800 MPU as to the direction of data exchange in the dynamic RAM. It transmits a Logic 0 to the R/W output for a Write Cycle and a Logic 1 for a Read Cycle.
A13 (A15) A12 (A14)	17 18	Upper Order Address lines from the M6800. These two inputs decode to four signals controlling the four RAS outputs. A14 and A15 apply to 16K RAMs.
MC	23	Memory Clock input from MC6875 clock or other signal source. The rising edge of MC must occur after the rising edge of t1 to avoid aborting the refresh cycle. When MC rises, it resets an internal flag that will terminate refresh at the end of the current cycle. Failure to reset the flag forces the 3480 to refresh every cycle thereafter. MC can be connected to t2 or t3 in noncritical applications.
MC	1	The buffered complement output of MC. It is a buffered output which may be used to drive the circuitry creating the time delays used on inputs t1 through t5.
t1 t2 t3 t4 t5	2 3 4 5 6	These pins use external timing inputs to sequentially select the outputs to be enabled. They are positive-edge triggered inputs. Assuming a Read/Write cycle is to be executed, a positive edge on t1 forces a logic 0 on one of the four RAS outputs as determined by the A12/14, A13/15 inputs. After a delay, a positive edge on t2 causes Row En to go to a Logic 0, providing address-multiplexing information to the MC3232A or MC3242A. t3 enables the CAS output and it goes low. t4 enables the R/W output and it goes low, assuming the R/W input was low. t5 resets all the outputs to a Logic 1 (with the exception of MC, Ref En, and Ref Req). The inputs t1, t2, t3, and t5 are daisy-chained, so they must be sequentially driven to obtain the desired output signals. t4 can be driven at any time after t1.
Ref Clk	21	The 32 kHz (64 kHz) Refresh Clock signals this pin that another refresh cycle is required. It is a positive-edge triggered input, and upon triggering, the Ref Req pin goes to a Logic 0.
Ref Req	20	The Refresh Request output acts as an input to the MPU system, requesting a refresh cycle. This output has a 5 k Ω pullup resistor to the VCC supply to allow wire-ORing if desired.
Ref Grant	19	Through the Refresh Grant input, the MC6875 initiates a refresh cycle. This input is positive-edge triggered and is enabled only after the Ref Req pin has gone low. This allows the MC3480 to discern between a Refresh Grant or a DMA Grant even though they appear on the same line. When employing both dynamic memory (refresh) and DMA in a microprocessor-based system with a combined Refresh/DMA Request control on the clock, provision must be made for holding off a DMA request during a refresh period (and visa versa). If this provision is not made, clock stretching (cycle stealing) will continue indefinitely and dynamic microprocessor data will be lost. The positive edge on Ref Grant causes Row En output to go low and Ref En output to go high. This signals the MC3232A (MC3242A) that a refresh address is required. The refresh cycle occurs with the succeeding pulses on t1-t5. A positive edge on t1 causes Ref Req to go high and all the RAS outputs to go low. A positive going edge on t2 causes no change in the outputs, since it controls the address multiplexing (Row En) during the Read/Write cycles. There is no output change when t3 and t4 go high because no CAS or R/W signal is needed during refresh. A positive edge on t5 resets the RAS and Row En to a Logic 1 state, and Ref En to a Logic 0 state, ready for the next Read/Write cycle.
VCC	24	+5.0 V supply. A 0.1 μ F capacitor is recommended to bypass pin 24 to ground.
Gnd	12	System Ground.

*These outputs are designed to drive the highly capacitive inputs of multiple dynamic RAMs (150 pF for RAS outputs, and 450 pF for CAS and R/W outputs). Consequently, these outputs have no short-circuit limit and must be handled accordingly. Good high capacitance load driving techniques usually include a 10 Ω or greater series damping resistor. It is highly recommended that this be done on RAS, CAS and R/W outputs of the MC3480. The effect of these series damping resistors on rise and fall times must be included in timing considerations.

NOTE: All other outputs are LS/TTL totem-pole configuration unless otherwise noted.



MOTOROLA

MC3487

QUAD LINE DRIVER WITH THREE-STATE OUTPUTS

Motorola's Quad RS-422 Driver features four independent driver chains which comply with EIA Standards for the Electrical Characteristics of Balanced Voltage Digital Interface Circuits. The outputs are three-state structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power up and power down. A summary of MC3487 features include:

- Four Independent Driver Chains
- Three-State Outputs
- PNP High Impedance Inputs (PIA Compatible)
- Fast Propagation Times (Typ 15 ns)
- TTL Compatible
- Single 5 V Supply Voltage
- Output Rise and Fall Times Less Than 20 ns
- DS 3487 Second Source

QUAD RS-422 LINE DRIVER WITH THREE-STATE OUTPUTS

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

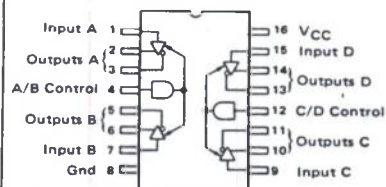


L SUFFIX
CERAMIC PACKAGE
CASE 620

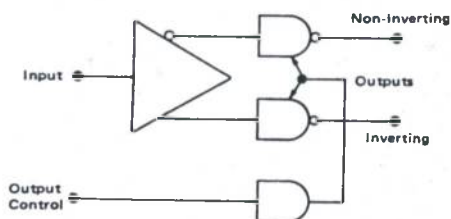


P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



DRIVER BLOCK DIAGRAM



TRUTH TABLE

Input	Control Input	Non-Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

*ABSOLUTE MAXIMUM RATINGS			
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	$^{\circ}\text{C}$
Operating Junction Temperature Range	T_J	175 150	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}\text{C}$

*"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Table of Electrical Characteristics" provides conditions for actual device operation.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply $4.75\text{ V} < V_{CC} < 5.25\text{ V}$ and $0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$. Typical values measured at $V_{CC} = 5.0\text{ V}$, and $T_A = 25^{\circ}\text{C}$.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — Low Logic State	V_{IL}	—	—	0.8	Vdc
Input Voltage — High Logic State	V_{IH}	2.0	—	—	Vdc
Input Current — Low Logic State ($V_{IL} = 0.5\text{ V}$)	I_{IL}	—	—	-400	μA
Input Current — High Logic State ($V_{IH} = 2.7\text{ V}$) ($V_{IH} = 5.5\text{ V}$)	I_{IH}	— —	— —	+50 +100	μA
Input Clamp Voltage ($I_{IK} = -18\text{ mA}$)	V_{IK}	—	—	-1.5	V
Output Voltage — Low Logic State ($I_{OL} = 48\text{ mA}$)	V_{OL}	—	—	0.5	V
Output Voltage — High Logic State ($I_{OH} = -20\text{ mA}$)	V_{OH}	2.5	—	—	V
Output Short-Circuit Current ($V_{IH} = 2.0\text{ V}$) ²	I_{OS}	-40	—	-140	mA
Output Leakage Current — Hi-Z State ($V_{IL} = 0.5\text{ V}$, $V_{IL}(Z) = 0.8\text{ V}$) ($V_{IH} = 2.7\text{ V}$, $V_{IL}(Z) = 0.8\text{ V}$)	$I_{OL}(Z)$	— —	— —	± 100 ± 100	μA
Output Leakage Current — Power OFF ($V_{OH} = 6.0\text{ V}$, $V_{CC} = 0\text{ V}$) ($V_{OL} = -0.25\text{ V}$, $V_{CC} = 0\text{ V}$)	$I_{OL}(\text{off})$	— —	— —	+100 -100	μA
Output Offset Voltage Difference ¹	$V_{OS} - V_{OS}$	—	—	± 0.4	V
Output Differential Voltage 1	V_T	2.0	—	—	V
Output Differential Voltage Difference 1	$V_T - V_T$	—	—	± 0.4	V
Power Supply Current (Control Pins = Gnd) ³ (Control Pins = 2.0 V)	I_{CCX} I_{CC}	— —	— —	105 85	mA

1. See EIA Specification RS-422 for exact test conditions.

2. Only one output may be shorted at a time.

3. Circuit in three-state condition.

SWITCHING CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $T_A = 25^{\circ}\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times					ns
High to Low Output	t_{PHL}	—	—	20	
Low to High Output	t_{PLH}	—	—	20	
Output Transition Times — Differential					ns
High to Low Output	t_{THL}	—	—	20	
Low to High Output	t_{TLH}	—	—	20	
Propagation Delay — Control to Output ($R_L = 200\ \Omega$, $C_L = 50\text{ pF}$) ($R_L = 200\ \Omega$, $C_L = 50\text{ pF}$) ($R_L = \infty$, $C_L = 50\text{ pF}$) ($R_L = 200\ \Omega$, $C_L = 50\text{ pF}$)	$t_{PHZ}(E)$ $t_{PLZ}(E)$ $t_{PZH}(E)$ $t_{PZL}(E)$	— — — —	— — — —	25 25 30 30	

Keyboard Encoder

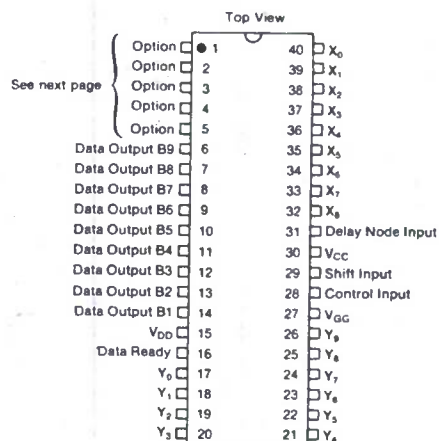
FEATURES

- One integrated circuit required for complete keyboard assembly
- N key rollover or lock out operation
- Quad mode operation
- Lock out/rollover selection under external control (option)
- Self-contained or slave oscillator circuit
- 10 output data bits available
- Outputs directly compatible with TTL/DTL or MOS logic arrays
- Output data buffer register included
- Output enable provided (option)
- External data complement control provided (option)
- Pulse or level data ready output signal provided (option)
- "Any Key Down" output provided (option)
- Externally controlled delay network provided to eliminate the effect of contact bounce
- Programmable coding with a single mask change
- Static charge protection on all input and output terminals
- Entire circuit protected by a layer of glass passivation

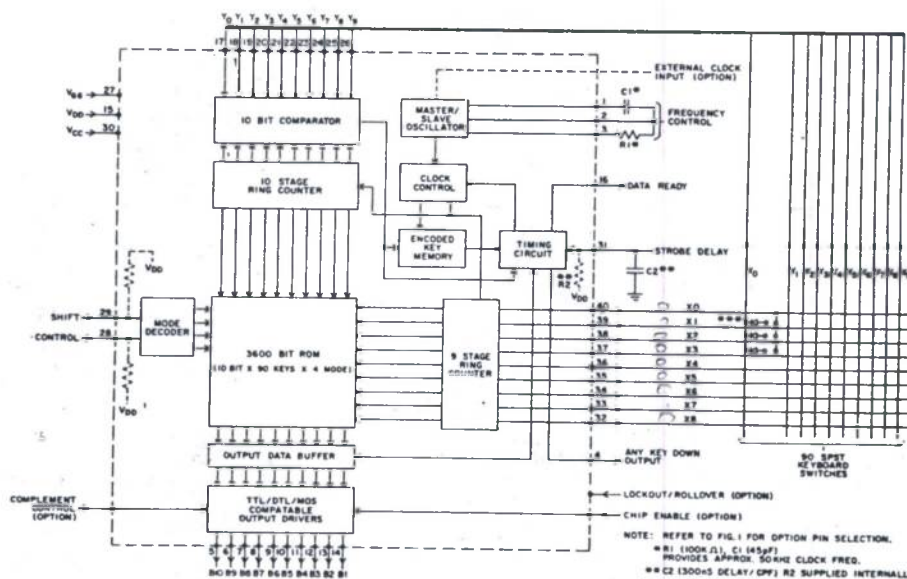
DESCRIPTION

The General Instrument AY-5-3600 is a Keyboard Encoder containing a 3600 bit Read Only Memory and all the logic necessary to encode single pole single throw keyboard closures into a usable 10 bit code. Data, Any Key Down and Data Ready outputs are directly compatible with TTL/DTL or MOS logic arrays without the need for any special interface components. The AY-5-3600 is fabricated with MTNS technology and contains 5000 P channel enhancement mode transistors on a single monolithic chip.

PIN CONFIGURATION 40 LEAD DUAL IN LINE



BLOCK DIAGRAM





CUSTOM CODING INFORMATION

The custom coding information for General Instrument's AY-5-3600 Keyboard Encoder ROM should be transmitted to General Instrument in the form of 80 column punched cards. Each ROM pattern requires 92 cards (1 title card, 1 circuit option card and 90 ROM pattern cards). (See Note 1)

If it is not possible to supply punched cards, then the Truth Table should be completed (See Note 1). However, there would be a

substantial savings in both the coding charge and turn-around time if punched cards were used. Upon receipt of the punched cards or the Truth Table, General Instrument will prepare a computer-generated Truth Table which will be returned to the user for verification.

NOTE 1: Card and Truth Table format available upon request.

PIN OPTIONS

Pins 6-40 of the AY-5-3600 are permanently assigned. The functions assigned to pins 1-5 depend on which functional options are selected from the following:

External Clock

—requires one package pin to input an external clock source.

Internal Oscillator

—requires three package pins interconnected with an external RC network to develop the clock required.

Lockout/Rollover (LO/RO)

—requires one package pin to externally select N-Key Lockout or N-Key Rollover. LO = +5V, RO = GND.

Complement Control (CC)

—requires one package pin to externally control the logic state of the data bits (B1-B10) and, if required, the Data Ready output.

Chip Enable (CE)

—requires one package pin to control the data bits (B1-B10) and, if required, the Data Ready and Any Key Output.

Any Key Output (AKO)

—requires one package pin to indicate a key depression.

Output Data Bit 10 (B10)

—requires one package pin when ten data bits are required to encode each key.

Select the pin options desired:

External Clock + 4 of the following functions

OR

Internal Oscillator + 2 of the following functions

LO/RO, CC, CE, AKO, BIO

The following chart lists the pin assignments according to the functions selected above:

PIN 1	PIN 2	PIN 3	PIN 4	PIN 5
External Clock	LO/RO	CC	CE	AKO
External Clock	LO/RO	CC	CE	BIO
External Clock	LO/RO	CC	AKO	BIO
External Clock	LO/RO	CE	AKO	BIO
External Clock	CC	CE	AKO	BIO
Internal Oscillator			LO/RO	CC
			LO/RO	CE
			LO/RO	AKO
			LO/RO	BIO
			CC	CE
			CC	AKO
			CC	BIO
			CE	AKO
			CE	BIO
			AKO	BIO

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} and V_{GG} (with respect to V_{CC}) -20V to +0.3V
 Logic input voltages (with respect to V_{CC}) -20V to +0.3V
 Storage Temperature -65°C to +150°C
 Operating Temperature Range. 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.5 Volts
 V_{GG} = -12 Volts ±1.0 Volts, V_{DD} = GND
 (V_{CC} = Substrate Voltage)
 Operating Temperature (T_A) = 0°C to +70°C

Clock

Extern
Clock

Data I

(Shi

Co

Loc

Ch

& Ex

Lo

Lo

St

Co

X Outp

Logi

Logi

Y Inpu

Trip

Hyst

Sele

Unse

Input C

X-Y Pr

Char

Switch

Mini

Cont

Re

Strobe

Trip

Hyst

Quie

Data C

Any Ke

Data R

Logi

Logi

Power

I_{CC}I_{GG}

**Typi

NOTE

1. Hyst

2. Pre

ELECTRICAL CHARACTERISTICS

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
Clock Frequency	f	10	50	100	kHz	See Block diagram footnote* for typical R-C values
External Clock Width		7	—	—	μs	
Clock Input	V _{IO} V _{II}	V _{DD} V _{CC} - 1.4	—	.15 V _{CC} + 0.3	V V	
Data Input (Shift, Control, Complement Control, Lockout/Rollover, Chip Enable & External Clock)	V _{ID} V _{II}	V _{DD} V _{CC} - 1.1	—	+0.75 V _{CC} + 0.3	V V	
Logic "0" Level						
Logic "1" Level						
Shift & Control Input Current	I _{INSC}	75	95	120	μA	V _I = +5V
X Output (X₀-X₈)						
Logic "1" Output Current	I _{XI}	40 600 900 1500 3000	170 1300 1600 3800 6000	400 2500 3500 6000 10000	μA μA μA μA μA	V _{OUT} = V _{CC} (See Note 2) V _{OUT} = V _{CC} - 1.3V V _{OUT} = V _{CC} - 2.0V V _{OUT} = V _{CC} - 5V V _{OUT} = V _{CC} - 10V
Logic "0" Output Current	I _{XO}	8 6 5 2 —	15 11 10 5 0.5	50 35 30 15 5	μA μA μA μA μA	V _{OUT} = V _{CC} V _{OUT} = V _{CC} - 1.3V V _{OUT} = V _{CC} - 2.0V V _{OUT} = V _{CC} - 5V V _{OUT} = V _{CC} - 10V
Y Input (Y₀-Y₈)						
Trip Level	V _Y	V _{CC} - 5	V _{CC} - 3	V _{CC} - 2	V	Y Input Going Positive (See Note 2)
Hysteresis	ΔV _Y	0.5	0.9	1.4	V	(See Note 1)
Selected Y Input Current	I _{YS}	18 14 13 6 —	36 28 25 12 1	100 90 80 60 30	μA μA μA μA μA	V _{IN} = V _{CC} V _{IN} = V _{CC} - 1.3V V _{IN} = V _{CC} - 2.0V V _{IN} = V _{CC} - 5V V _{IN} = V _{CC} - 10V
Unselected Y Input Current	I _{YU}	9 7 6 3 —	18 14 13 6 0.5	50 45 40 30 15	μA μA μA μA μA	V _{IN} = V _{CC} V _{IN} = V _{CC} - 1.3V V _{IN} = V _{CC} - 2.0V V _{IN} = V _{CC} - 5V V _{IN} = V _{CC} - 10V
Input Capacitance	C _{IN}	—	3	10	pF	at 0V (All Inputs)
X-Y Precharge						
Characteristics	φP	1500 200	3500 600	5000 1500	μA μA	V = V _{CC} V = V _{CC} - 5 (See Note 2)
Switch Characteristics						
Minimum Switch Closure	—	—	—	—	—	See Timing Diagram
Contact Closure						
Resistance	Z _{CC} Z _{CO}	— 1 × 10 ⁷	— —	300 —	Ω Ω	
Stroke Delay						
Trip Level (Pin 31)	V _{SD}	V _{CC} - 4	V _{CC} - 3	V _{CC} - 2	V	
Hysteresis	V _{SD}	0.5	0.9	1.4	V	(See Note 1)
Quiescent Voltage (Pin 31)		-3	-5	-9	V	With Internal Switched Resistor
Data Output (B1-B10), Any Key Down Output, Data Ready						
Logic "0"	—	—	—	.55	V	I _{OL} = .25mA
Logic "1"	—	—	—	0.8	V	I _{OL} = 1.6mA
Power	—	V _{CC} - 1.3	—	—	V	I _{OH} = .95mA
Power						
I _{CC}	—	—	8	13	mA	V _{CC} = +5V
I _{GG}	—	—	8	13	mA	V _{GG} = -12V

**Typical values are at +25°C and nominal voltages.

NOTE

1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Precharge of X outputs and Y inputs occurs during each scanned clock cycle.

OPERATION

The AY-5-3600 contains (see Block Diagram) a 3600 bit ROM, 9-stage and 10-stage ring counters, a 10 bit comparator, timing circuitry, a 90 bit memory to store the location of encoded keys for n key rollover operation, an externally controllable delay network for eliminating the effect of contact bounce, an output data buffer, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 360 by 10 bit memory arranged into four 90-word by 10-bit groups. The appropriate levels on the Shift and Control Inputs selects one of the four 90-word groups; the 90-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

The external outputs of the 9-stage ring counter and the external inputs to the 10-bit comparator are wired to the keyboard to form an X-Y matrix with the 90-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM, thereby scanning the key switches for key closures.

When a key is depressed, a single path is completed between one output of the 9-stage ring counter (X_0 thru X_8) and one input of the 10-bit comparator (Y_0 - Y_9). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 10-stage ring counter.

N KEY ROLLOVER

— When a match occurs, and the key has not been encoded, the switch bounce delay network is enabled. If the key is still de-

pressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears, a one is stored in the encoded key memory and the scan sequence is resumed. If a match occurs at another key location, the sequence is repeated thus encoding the next key. If the match occurs for an already encoded key, the match is not recognized. The code of the last key encoded remains in the output data buffer.

N KEY LOCKOUT

— When a match occurs, the delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears and the remaining keys are locked out by halting the scan sequence. The scan sequence is resumed upon key release. The output data buffer stores the code of the last key encoded.

SPECIAL PATTERNS

— Since the selected coding of each key and all the options are defined during the manufacture of the chip, the coding and options can be changed to fit any particular application of the keyboard. Up to 360 codes of up to 10 bits can be programmed into the AY-5-3600 ROM covering most popular codes such as ASCII, EBCDIC, Selectric, etc., as well as many specialized codes. The ASCII code in conjunction with internal oscillator, 10 data outputs and any key down output, is available as a standard pattern (See Figure 2).

TIMING DIAGRAM

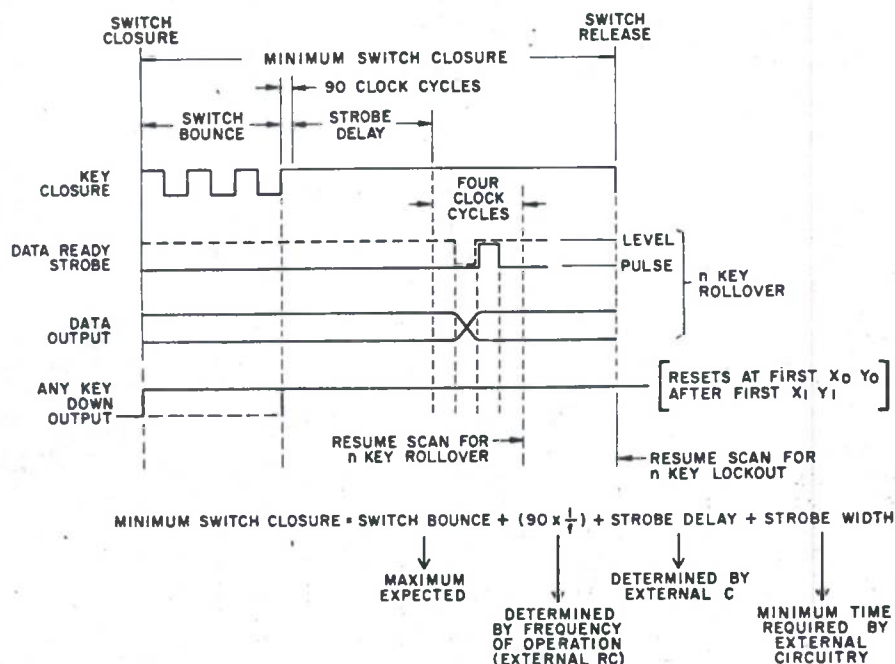


Fig.1

SYMBOL	MODE				SYMBOL	MODE			
	N	S	C	SC		N	S	C	SC
0		X1 Y0, X0 Y8		X1 Y2	SOH			X0 Y8	X5 Y0, X0 Y8
1		X0 Y2		X2 Y2	STX			X1 Y8	X4 Y0, X1 Y8
2		X3 Y2		X3 Y2	ETX	X4 Y4	X4 Y4	X4 Y4	X4 Y4, X8 Y0
3		X2 Y2		X4 Y2	END				X4 Y1
4		X2 Y1		X5 Y2	ACK			X2 Y8	X3 Y1
5		X3 Y2		X6 Y2	BEL			X2 Y8	X7 Y1, X2 Y8
6		X4 Y2		X7 Y2	BS			X3 Y8	X6 Y1, X3 Y8
7	X0 Y5	X0 Y5, X5 Y2	X0 Y5	X0 Y5	HT	X0 Y4	X0 Y4	X0 Y4, X8 Y8	X8 Y8
8		X7 Y1		X0 Y4	LF	X7 Y8	X7 Y8	X7 Y8	
9		X6 Y2		X6 Y8	VT	X3 Y7	X3 Y7	X3 Y7	X3 Y7
A		X7 Y2		X3 Y8	FF	X7 Y8	X7 Y8	X7 Y8	X7 Y8
B	X2 Y5	X2 Y5, X8 Y2	X2 Y5	X2 Y8	CR	X3 Y5	X3 Y5	X3 Y5, X1 Y8	X1 Y8
C		X7 Y3		X2 Y8	SO	X0 Y7	X0 Y7	X0 Y7, X1 Y8	X0 Y7, X1 Y8
D		X6 Y3		X4 Y5	SI	X1 Y7	X1 Y7	X1 Y7	X1 Y7
E		X8 Y1		X0 Y2, X0 Y3	DLE				X0 Y1
F		X6 Y5		X1 Y3	DC1				X0 Y1
G		X0 Y1		X2 Y3	DC2				X5 Y1
H		X3 Y1		X4 Y3	DC3				X6 Y7
I		X1 Y2		X5 Y3	DC4				X2 Y1
J		X4 Y1		X6 Y3	NAK				X3 Y0
K		X5 Y1		X7 Y3	SYN				X2 Y0
L		X4 Y2		X8 Y3	ETB				X5 Y4
M		X1 Y1		X6 Y5	CAN	X3 Y4		X3 Y4	X1 Y0
N		X1 Y2		X8 Y2	EM				X8 Y0
O		X5 Y1		X5 Y5	SUB				X0 Y0
P		X0 Y2		X0 Y2	ESC				X7 Y0
Q		X5 Y3		X5 Y3	FS				X1 Y4
R		X2 Y3		X2 Y3	CS				X7 Y6
S		X2 Y2		X2 Y2	RS	X1 Y4	X1 Y4	X1 Y4	
T		X2 Y1		X2 Y1	US	X2 Y7	X2 Y7	X2 Y7	X2 Y7
U		X3 Y2		X3 Y2	SP	X3 Y3, X4 Y9	X4 Y9, X3 Y3	X4 Y9, X3 Y3	X4 Y9, X3 Y3
V		X4 Y2		X4 Y2	1	X5 Y9	X5 Y9	X5 Y9	X5 Y9
W		X5 Y2		X5 Y2	2	X3 Y8, X7 Y5, X1 Y8	X3 Y8	X3 Y8	X3 Y8, X7 Y5
X		X7 Y1		X7 Y1	3	X6 Y8	X6 Y8	X6 Y8	X6 Y8
Y		X6 Y2		X6 Y2	4	X2 Y5, X3 Y0	X2 Y5	X2 Y5	X2 Y5
Z		X7 Y2, X2 Y8		X7 Y2	5	X1 Y5, X4 Y0	X1 Y5	X1 Y5	X1 Y5
[		X8 Y2		X8 Y2	6	X6 Y8	X6 Y8, X8 Y8, X2 Y8	X6 Y8	X6 Y8
\		X7 Y3, X1 Y6		X7 Y3	7	X7 Y5	X7 Y5	X7 Y5	X7 Y5
]		X6 Y2, X1 Y8		X6 Y3	8	X7 Y8	X7 Y8, X3 Y4, X8 Y0	X7 Y8	X7 Y8
^		X8 Y1		X8 Y1	9	X4 Y8	X4 Y8, X6 Y7, X8 Y9	X4 Y8	X4 Y8
_		X6 Y5, X0 Y8		X6 Y6	-	X5 Y8	X5 Y8, X7 Y0, X5 Y4	X5 Y8	X5 Y8
0		X0 Y1		X0 Y1	.	X0 Y8	X0 Y8, X5 Y8, X7 Y7	X0 Y8	X0 Y8, X7 Y7
1		X3 Y1		X3 Y1	/	X8 Y2	X8 Y2	X8 Y2	X8 Y2
2		X1 Y2		X1 Y2	-	X2 Y4	X2 Y4, X8 Y7	X2 Y4	X2 Y4
3		X4 Y1		X4 Y1	=	X8 Y4	X8 Y4	X8 Y4	X8 Y4
4		X5 Y1		X5 Y1	>	X7 Y4	X7 Y4	X7 Y4	X7 Y4
5		X4 Y3		X4 Y3	0	X6 Y7, X8 Y8	X8 Y8	X8 Y7, X8 Y8	X8 Y8
6		X1 Y1		X1 Y1	1	X0 Y0, X0 Y5	X0 Y0	X0 Y0	X0 Y0
7		X1 Y3		X1 Y3	2	X1 Y0, X1 Y8	X1 Y0	X1 Y0	X1 Y0
8		X5 Y1		X5 Y1	3	X2 Y8	X2 Y8	X2 Y8	X2 Y8
9		X0 Y3		X0 Y3	4	X3 Y0	X3 Y0	X3 Y0	X3 Y0
A		X8 Y6, X2 Y8		X4 Y6, X8 Y6	5	X4 Y0	X4 Y0	X4 Y0	X4 Y0
B		X1 Y6		X8 Y6	6	X5 Y0, X2 Y8	X5 Y0	X5 Y0	X5 Y0
C		X1 Y8		X2 Y4	7	X6 Y0, X3 Y8	X6 Y0	X6 Y0	X6 Y0
D		X4 Y7, X8 Y7		X4 Y7	8	X7 Y0	X7 Y0	X7 Y0	X7 Y0
E		X3 Y6		X3 Y6	9	X8 Y0, X8 Y8	X8 Y0	X8 Y0	X8 Y0
F		X4 Y5		X4 Y5	.	X5 Y4	X5 Y4	X5 Y4	X5 Y4
G					/	X8 Y5, X5 Y8	X8 Y5	X8 Y5, X5 Y8	X8 Y5
H					-	X8 Y5	X7 Y8, X8 Y5, X0 Y0	X8 Y5	X8 Y5
I					=	X8 Y4, X7 Y7	X7 Y7, X8 Y4, X4 Y7	X8 Y4	X8 Y4
J					>	X5 Y5	X5 Y5, X5 Y0, X0 Y7	X5 Y5	X5 Y5
K					1	X4 Y6	X4 Y6, X7 Y4	X4 Y6	X4 Y6

Note 1. Bits 1 to 6 and bit 8 of the AY-5-3600 correspond to bits 1 to 7 of ASCII.

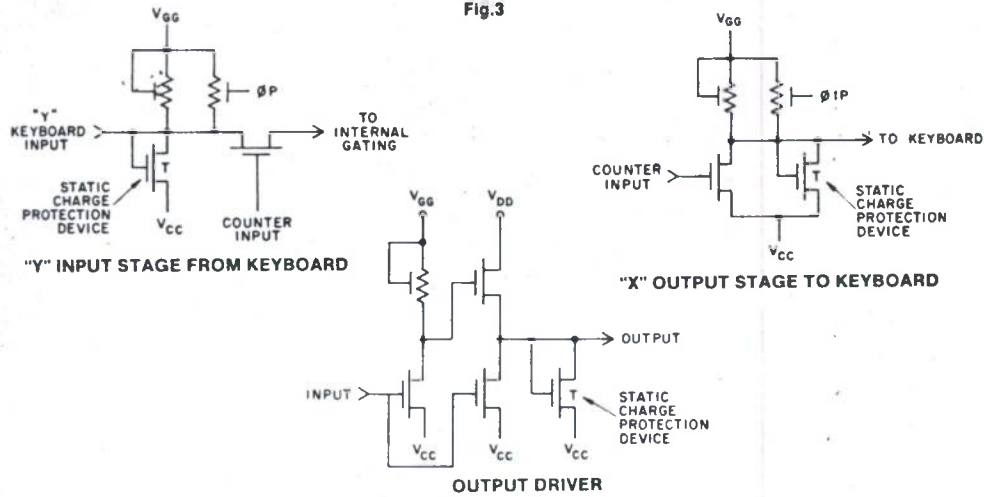
Note 2. Codes 00000111 and 00111111 are not present in the standard AY-5-3600 pattern.

Fig.2 STANDARD AY-5-3600 CODE ASSIGNMENTS ASCII CODE

OPTIONS PROVIDED WITH STANDARD ENCODER

- Device Marking: AY-5-3600
- Internal Oscillator on Pin Nos. 1, 2, 3
- Any Key Output on Pin No. 4
- Any Key Output True (Logic 1) During Key Depression
- Output Data Bit B10 on Pin No. 5
- N-Key Rollover Only
- True Outputs Only
- Pulse Data Ready Signal
- Internal Resistor to V_{DD} on Shift/Control Pin
- Plastic Package

Fig.3



NOTE: Output driver capable of driving one TTL load with no external resistor.
Capable of driving two TTL loads using an external 6.8K Ω resistor to V_{cc} .

TYPICAL CHARACTERISTIC CURVES

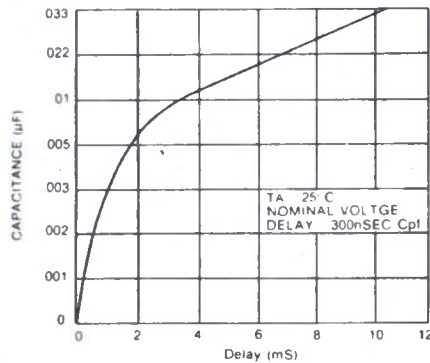
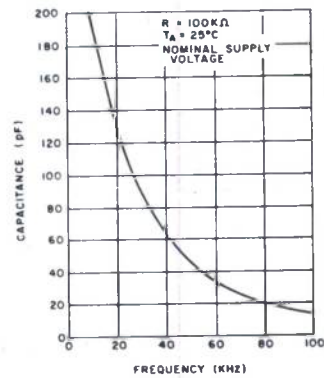
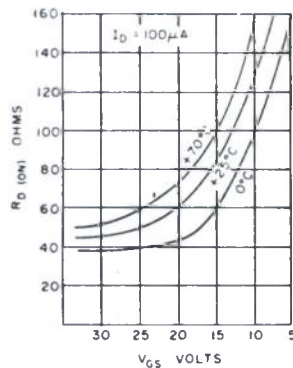
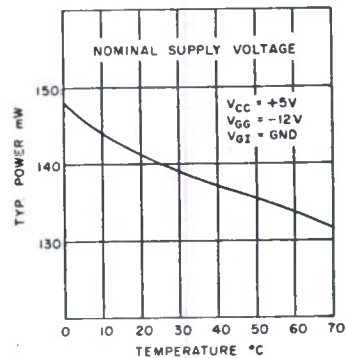
Fig.4 STROBE DELAY vs. C_1 Fig.5 OSCILLATOR FREQUENCY vs. C_2 Fig.6 TYPICAL OUTPUT ON RESISTANCE (R_{DON}) vs. GATE BIAS VOLTAGE (V_{GS})

Fig.7 TYPICAL POWER CONSUMPTION (mW)



Industrial/Automotive/Functional Blocks/Telecommunications

LM122/LM222/LM322, LM2905/LM3905 Precision Timers

General Description

The LM122 series are precision timers that offer great versatility with high accuracy. They operate with unregulated supplies from 4.5V to 40V while maintaining constant timing periods from microseconds to hours. Internal logic and regulator circuits complement the basic timing function enabling the LM122 series to operate in many different applications with a minimum of external components.

The output of the timer is a floating transistor with built-in current limiting. It can drive either ground referred or supply referred loads up to 40V and 50 mA. The floating nature of this output makes it ideal for interfacing, lamp or relay driving, and signal conditioning where an open collector or emitter is required. A "logic reverse" circuit can be programmed by the user to make the output transistor either "on" or "off" during the timing period.

The trigger input to the LM122 series has a threshold of 1.6V independent of supply voltage, but it is fully protected against inputs as high as $\pm 40V$ even when using a 5V supply. The circuitry reacts only to the rising edge of the trigger signal, and is immune to any trigger voltage during the timing periods.

An internal 3.15V regulator is included in the timer to reject supply voltage changes and to provide the user with a convenient reference for applications other than a basic timer. External loads up to 5 mA can be driven by the regulator. An internal 2V divider between the reference and ground sets the timing period to 1 RC. The timing period can be voltage controlled by driving this divider

with an external source through the V_{ADJ} pin. Timing ratios of 50:1 can be easily achieved.

The comparator used in the LM122 utilizes high gain PNP input transistors to achieve 300 pA typical input bias current over a common mode range of 0V to 3V. A boost terminal allows the user to increase comparator operating current for timing periods less than 1 ms. This lets the timer operate over a $3\mu s$ to multi-hour timing range with excellent repeatability.

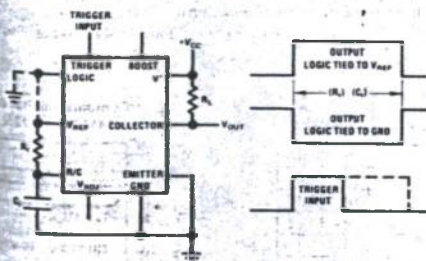
The LM122 operates over a temperature range of $-55^{\circ}C$ to $+125^{\circ}C$. An electrically identical LM222 is specified from $-25^{\circ}C$ to $+85^{\circ}C$, and the LM322 is specified from $0^{\circ}C$ to $+70^{\circ}C$. The LM2905/LM3905 are identical to the LM122 series except that the boost and V_{ADJ} pin options are not available, limiting minimum timing period to 1 ms.

Features

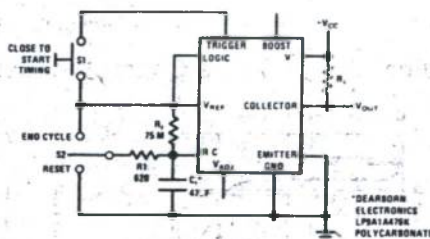
- Immune to changes in trigger voltage during timing interval
- Timing periods from microseconds to hours
- Internal logic reversal
- Immune to power supply ripple during the timing interval
- Operates from 4.5V to 40V supplies
- Input protected to $\pm 40V$
- Floating transistor output with internal current limiting
- Internal regulated reference
- Timing period can be voltage controlled
- TTL compatible input and output

LM122/LM222/LM322, LM2905/LM3905

Typical Applications



Basic Timer-Collector Output and Timing Chart



One Hour Timer with Reset and Manual Cycle End

Absolute Maximum Ratings

Power Dissipation	500 mW	Operating Temperature Range
V ⁺ Voltage	40V	LM122
Collector Output Voltage	40V	LM222
V _{REF} Current	5 mA	LM322
Trigger Voltage	±40V	LM2905
V _{ADJ} Voltage (Forced)	5V	LM3905
Logic Reverse Voltage	5.5V	
Output Short Circuit Duration (Note 1)		
Lead Temperature (Soldering, 10 sec)	300°C	

Electrical Characteristics (Note 2)

PARAMETER	CONDITIONS	LM122/LM222			LM322			LM2905/LM3905		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
Timing Ratio	T _A = 25°C, 4.5V ≤ V ⁺ ≤ 40V Boost Tied to V ⁺ , (Note 3)	0.626	0.632	0.638	0.620	0.632	0.644	0.620	0.632	0.644
Comparator Input Current	T _A = 25°C, 4.5V ≤ V ⁺ ≤ 40V Boost Tied to V ⁺		0.3	1.0		0.3	1.5		0.5	1.5
Trigger Voltage	T _A = 25°C, 4.5V ≤ V ⁺ ≤ 40V	1.2	1.6	2	1.2	1.6	2	1.2	1.6	2
Trigger Current	T _A = 25°C, V _{TRIG} = 2V		25			25			25	
Supply Current	T _A ≥ 25°C, 4.5V ≤ V ⁺ ≤ 40V		2.5	4		2.5	4.5		2.5	4.5
Timing Ratio	4.5V ≤ V ⁺ ≤ 40V Boost Tied to V ⁺	0.62		0.644	0.61		0.654	0.61		0.654
Comparator Input Current	4.5V ≤ V ⁺ ≤ 40V Boost Tied to V ⁺ , (Note 4)	-5		5	-2		2	-2.5		2.5
Trigger Voltage	4.5V ≤ V ⁺ ≤ 40V	0.8		2.5	0.8		2.5	0.8		2.5
Trigger Current	V _{TRIG} = 2.5V			200			200			200
Output Leakage Current	V _{CE} = 40V			1			5			5
Capacitor Saturation Voltage	R _T ≥ 1 MΩ R _T = 10 kΩ		2.5			2.5			2.5	
Reset Resistance			25			25			25	
Reference Voltage	T _A = 25°C		150			150			150	
Reference Regulation	0 ≤ I _{OUT} ≤ 3 mA 4.5V ≤ V ⁺ ≤ 40V	3	3.15	3.3	3	3.15	-3.3	3	3.15	3.3
Collector Saturation Voltage	I _L = 8 mA I _L = 50 mA		20	50		20	50		20	50
Emitter Saturation Voltage	T _A = 25°C, I _L = 3 mA T _A = 25°C, I _L = 50 mA		6	25		6	25		6	25
Average Temperature			0.25	0.4		0.25	0.4		0.25	0.4
Coefficient of Timing Ratio			0.7	1.4		0.7	1.4		0.7	1.4
Minimum Trigger Width	V _{TRIG} = 3V		1.8	2.2		1.8	2.2		1.8	2.2
			2.1	3		2.1	3		2.1	3
			0.003			0.003			0.003	

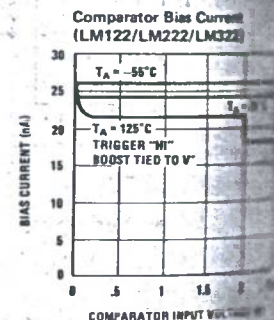
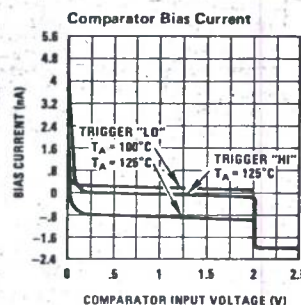
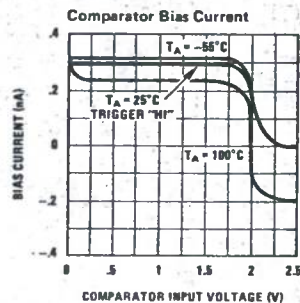
Note 1: Continuous output shorts are not allowed. Short circuit duration at ambient temperatures up to 40°C may be calculated from $t = (V_{CE}/I_{SC})$ seconds, where V_{CE} is the collector to emitter voltage across the output transistor during the short.

Note 2: These specifications apply for T_{MIN} ≤ T_A ≤ T_{MAX} unless otherwise noted.

Note 3: Output pulse width can be calculated from the following equation: $t = (R_T)(C_T)[1 - 2(0.632 - r) - V_C/V_{REF}]$ where r is timing ratio and V_C is capacitor saturation voltage. This reduces to $t = (R_T)(C_T)$ for all but the most critical applications.

Note 4: Sign reversal may occur at high temperatures (> 100°C) where comparator input current is predominately leakage. See typical curves.

Typical Performance Characteristics



MODEL 40J/K GENERAL PURPOSE LOW COST FET OP-AMP
SPECIFICATIONS (typical @ 25°C and ±15VDC unless otherwise noted)

MODEL	40J	40K
OPEN LOOP GAIN		
dc rated load, min	5x10 ⁴	*
dc 10k load	2x10 ⁵	*
RATED OUTPUT		
Voltage, min	±10V	*
Current, min	±5mA	*
Load capacitance range	0.005μF	*
FREQUENCY RESPONSE		
Unity gain, small signal	4MHz	*
Full power response, min	100kHz	*
Slewing rate, min	6V/μsec	*
Overload recovery	4μsec	*
INPUT OFFSET VOLTAGE		
External trim pot	1kΩ ¹	*
Initial offset, 25°C	±2mV(500Ω trim)	*
Avg. vs. temp (+10° to +60°C) max	±50μV/°C ³	±20μV/°C
vs. supply voltage	±50μV/%	*
vs. time	±250μV/month	*
INPUT BIAS CURRENT		
Input bias, 25°C, max	(0,-) 50pA	(0,-) 20pA
Avg. vs. temp	doubles every +10°C	*
vs. supply voltage	±1 pA/%	*
INPUT DIFFERENCE CURRENT		
Initial difference, 25°C	±25pA	±10pA
Avg. vs. temp	doubles every +10°C	*
INPUT IMPEDANCE		
Differential	10 ¹¹ Ω 3.5pF	*
Common mode	10 ¹¹ Ω 3.5pF	*
INPUT NOISE		
Voltage, 0.01 to 1Hz, p-p	6μV	*
5 to 50kHz, rms	3μV	*
Current, 0.01 to 1Hz, p-p	0.1pA	*
INPUT VOLTAGE RANGE		
Common mode voltage, min ² (1% error)	+8, -10V	*
Common mode rejection ² @+8, -10V	80dB	*
Max. safe differential voltage	±15V	*
POWER SUPPLY		
Voltage, rated specification	±15V	*
Voltage, derated specification	±(12 to 18)V	*
Current, quiescent	5.5mA	*
TEMPERATURE RANGE		
Rated performance	+10° to +60°C	*
Operating	-25° to +85°C	*
Storage	-55° to +125°C	*
MECHANICAL		
Case style - pin configuration	M-2	*
Mating socket	AC 1003	*
Weight	0.52 oz.	*
PRICE		
1-9	\$12.00	\$19.00
10-24	\$11.80	\$17.10

*Specifications same as for Model 40J.

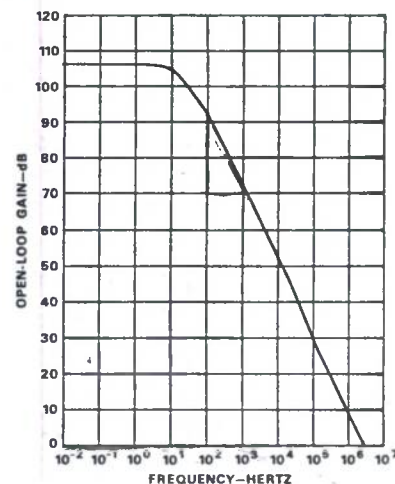
¹ Analog Devices part no. 79PR 1K \$3.00 (1-9)

² CMRR of 74dB min @ ±10V, specify model 40JV, \$3.00 additional (1-24)

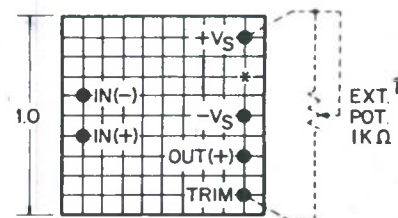
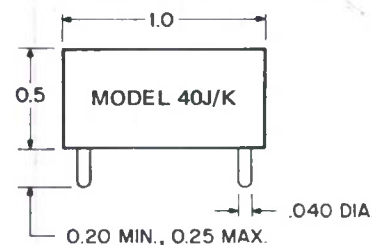
³ Same specification available -25°C to +85°C. Consult factory or your nearest Analog representative about Model 40A.

Specifications subject to change without notice.

**OPEN LOOP
FREQUENCY RESPONSE**



OUTLINE DIMENSIONS



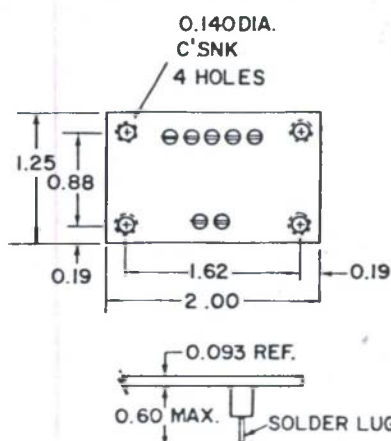
BOTTOM VIEW 0.1 GRID

*Note: Common supply connection not necessary within the amplifier.

¹ External variable resistor is used to zero the amplifier. Fixed 500-ohm resistor gives nominal zero (±2 mV). If no resistor desired, connect TRIM to +V_s. If TRIM left open, unit operates, but with considerable offset.

**MATING SOCKET
AC 1003**

PRICE (1-9) \$2.75



IH5009 — IH5024

Virtual Ground Analog Switches

FEATURES

- Switches Analog Signals up to 20 Volts Peak-to-Peak
- Each Channel Complete — Interfaces with Most Integrated Logic
- Switching Speeds Less than $0.5\mu s$
- $I_{D(OFF)}$ Less than 500pA Typical at $70^\circ C$
- Effective $r_{DS(ON)}$ — 5Ω to 50Ω
- Commercial and Military Temperature Range Operation

GENERAL DESCRIPTION

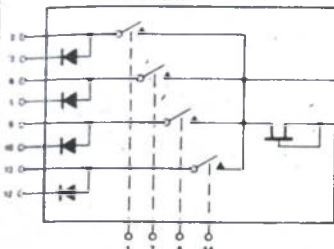
The IH5009 series of analog switches were designed to fill the need for an easy-to-use, inexpensive switch for both industrial and military applications. Although low cost is a primary design objective, performance and versatility have not been sacrificed.

Each package contains up to four channels of analog gating and is designed to eliminate the need for an external driver. The odd numbered devices are designed to be driven directly from T^2L open collector logic (15 volts) while the even numbered devices are driven directly from low level T^2L logic (5 volts). Each channel simulates a SPDT switch. SPST switch action is obtained by leaving the diode cathode unconnected; for SPDT action, the cathode should be grounded (0V). The parts are intended for high performance multiplexing and commutating usage. A logic "0" turns the channel ON and a logic "1" turns the channel OFF.

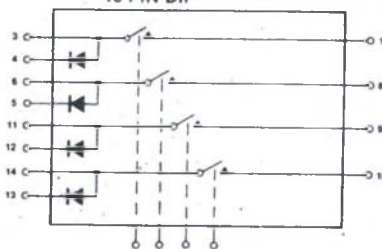
3

PIN CONNECTIONS

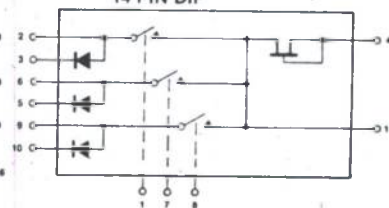
IH5009 ($r_{DS(ON)} \leq 100\Omega$)
IH5010 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP (OUTLINE DWGS DD, PD, JD)



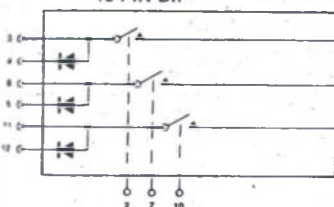
IH5011 ($r_{DS(ON)} \leq 100\Omega$)
IH5012 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP (OUTLINE DWGS DE, PE, JE)



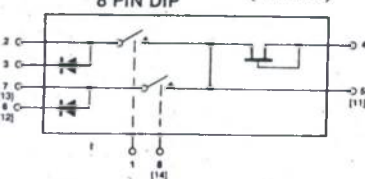
IH5013 ($r_{DS(ON)} \leq 100\Omega$)
IH5014 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP (OUTLINE DWGS DD, PE, JE)



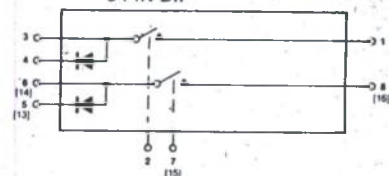
IH5015 ($r_{DS(ON)} \leq 100\Omega$)
IH5016 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP (OUTLINE DWGS DE, PE, JE)



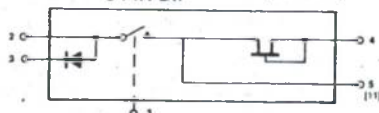
IH5017 ($r_{DS(ON)} \leq 100\Omega$)
IH5018 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP (OUTLINE DWGS DD, PA, JD)



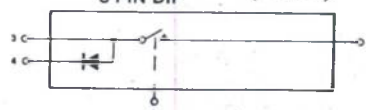
IH5019 ($r_{DS(ON)} \leq 100\Omega$)
IH5020 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP (OUTLINE DWGS DE, PA, JE)



IH5021 ($r_{DS(ON)} \leq 100\Omega$)
IH5022 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP (OUTLINE DWGS DD, PA, JD)



IH5023 ($r_{DS(ON)} \leq 100\Omega$)
IH5024 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP (OUTLINE DWGS DE, PA)



(Note: Numbers in brackets refer to Cerdip packages.)

IH5009 — IH5024

INTERMIL

IH5009 —
TYPICAL ELEC

ABSOLUTE MAXIMUM RATINGS

Positive Analog Signal Voltage.....	30V
Negative Analog Signal Voltage.....	-15V
Diode Current.....	10mA
Power Dissipation (Note).....	500mW
Storage Temperature.....	-65°C to +150°C
Lead Temperature (Soldering, 10 sec).....	300°C

Operating Temperature

5009C Series.....	0°C to +70°C
5009M Series.....	-55°C to +125°C
Lead Temperature (Soldering, 10 sec).....	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 75°C. For higher temperature, derate at rate of 5mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (per channel)

SYMBOL (Note 1)	CHARACTERISTIC	TYPE (Note 4)	TEST CONDITIONS (Note 2)	SPECIFICATION LIMIT			UNITS
				-55°C (M) 0°C (C)	25°C TYP.	+125°C (M) +70°C (C)	
$I_{IN(ON)}$	Input Current-ON	All	$V_{IN} = 0V, I_D = 2mA$	0.1	.01	0.1	μA
$I_{IN(OFF)}$	Input Current-OFF	5V Logic Ckts	$V_{IN} = +4.5V, V_A = \pm 10V$	0.2	.04	0.1	nA
$I_{IN(OFF)}$	Input Current-OFF	15V Logic Ckts	$V_{IN} = +11V, V_A = \pm 10V$	0.2	.04	0.2	nA
$V_{IN(ON)}$	Channel Control Voltage-ON	5V Logic Ckts	See Figure 5, Note 3	1.5		1.5	V
$V_{IN(ON)}$	Channel Control Voltage-ON	15V Logic Ckts	See Figure 5, Note 3	4.5		4.5	V
$V_{IN(OFF)}$	Channel Control Voltage-OFF	5V Logic Ckts	See Figure 5, Note 3	11.0		11.0	V
$V_{IN(OFF)}$	Channel Control Voltage-OFF	15V Logic Ckts	See Figure 5, Note 3	0.2	.02	0.2	nA
$I_{D(OFF)}$	Leakage Current-OFF	5V Logic Ckts	$V_{IN} = +4.5V, V_A = \pm 10V$	0.2	.02	0.2	nA
$I_{D(OFF)}$	Leakage Current-OFF	15V Logic Ckts	$V_{IN} = +11V, V_A = \pm 10V$	0.2	.02	0.2	nA
$I_{D(ON)}$	Leakage Current-ON	5V Logic Ckts	$V_{IN} = 0V, I_S = 1mA$	1.0	0.30	1.0	1000 (M) 200 (C)
$I_{D(ON)}$	Leakage Current-ON	15V Logic Ckts	$V_{IN} = 0V, I_S = 1mA$	0.5	0.10	0.5	500 (M) 100 (C)
$I_{D(ON)}$	Leakage Current-ON	5V Logic Ckts	$V_{IN} = 0V, I_S = 2mA$	1.0		1.0	μA
$I_{D(ON)}$	Leakage Current-ON	15V Logic Ckts	$V_{IN} = 0V, I_S = 2mA$	2.0		2.0	1000
$r_{DS(ON)}$	Drain-Source ON-Resistance	5V Logic Ckts	$I_D = 2mA, V_{IN} = 0.5V$	150	90	150	385 (M) 240 (C)
$r_{DS(ON)}$	Drain-Source ON-Resistance	15V Logic Ckts	$I_D = 2mA, V_{IN} = 1.5V$	100	60	100	250 (M) 160 (C)
t_{on}	Turn-ON Time	All	See Figures 3 & 4		150	500	ns
t_{off}	Turn-OFF Time	All	See Figures 3 & 4		300	500	ns
CT	Cross Talk	All	$f = 100Hz$		120		dB

NOTE 1: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

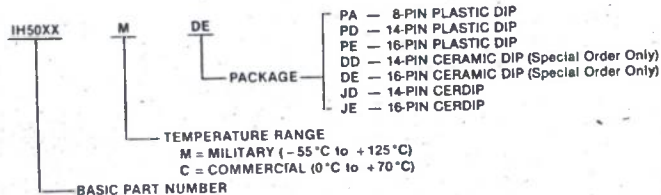
NOTE 2: Refer to Figure 2 for definition of terms.

NOTE 3: $V_{IN(ON)}$ and $V_{IN(OFF)}$ are test conditions guaranteed by the tests of respectively $r_{DS(ON)}$ and $I_{D(OFF)}$.

NOTE 4: "5V Logic CKTS" applies to even-numbered devices.

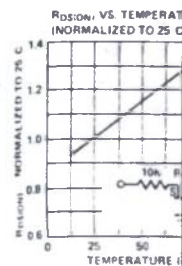
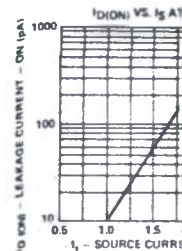
"15V Logic CKTS" applies to odd-numbered devices.

ORDERING INFORMATION



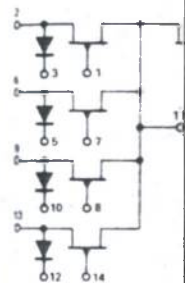
BASIC PART NUMBER	CHANNELS	LOGIC LEVEL	PACKAGES
IH5009	4	+15	JD,DD,PD
IH5010	4	+5	JD,DD,PD
IH5011	4	+15	JE,DE,PE
IH5012	4	+5	JE,DE,PE
IH5013	3	+15	JD,DD,PD
IH5014	3	+5	JD,DD,PD
IH5015	3	+15	JE,DE,PE
IH5016	3	+5	JE,DE,PE
IH5017	2	+15	JD,DD,PA
IH5018	2	+5	JD,DD,PA
IH5019	2	+15	JE,DE,PA
IH5020	2	+5	JE,DE,PA
IH5021	1	+15	JD,DD,PA
IH5022	1	+5	JD,DD,PA
IH5023	1	+15	JE,DE,PA
IH5024	1	+5	JE,DE,PA

NOTE: Mil-Temperature range (-55°C to +125°C) available ceramic packages only.

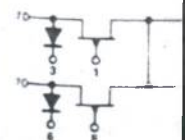


DEVICE SCHEM

IH5009 ($r_{DS(ON)} \leq$
IH5010 ($r_{DS(ON)} \leq$
14 PIN DIP



IH5017 ($r_{DS(ON)} \leq$
IH5018 ($r_{DS(ON)} \leq$
8 PIN DIP

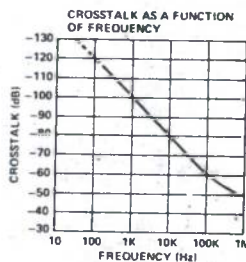
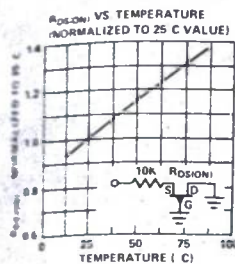
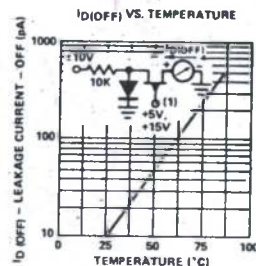
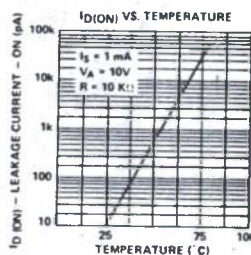
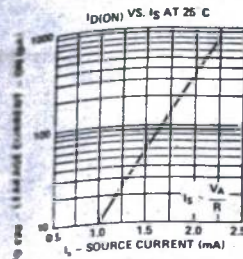


TYPICAL ELECTRICAL CHARACTERISTICS (per channel)

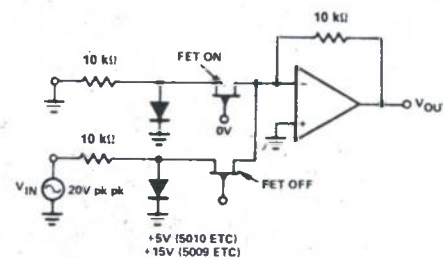
0°C to +70°C
-55°C to +125°C
10 sec) 300

ice is... with all leads...
board... ambient temperature...
rate of 5mW/°C.

ge to the device. These...
above those indicated in...
ing conditions for exten...



CROSSTALK MEASUREMENT CIRCUIT

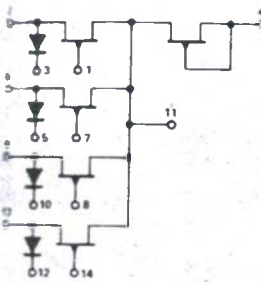


3

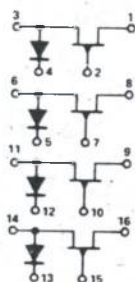
DEVICE SCHEMATICS AND PIN CONNECTIONS

FOUR CHANNEL

IH5009 ($r_{DS(ON)} \leq 100\Omega$)
IH5010 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

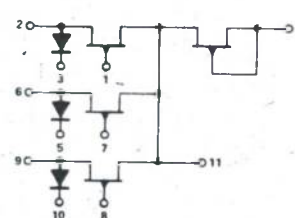


IH5011 ($r_{DS(ON)} \leq 100\Omega$)
IH5012 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP

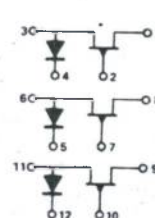


THREE CHANNEL

IH5013 ($r_{DS(ON)} \leq 100\Omega$)
IH5014 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

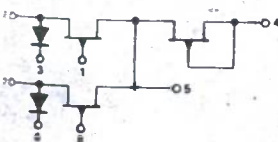


IH5015 ($r_{DS(ON)} \leq 100\Omega$)
IH5016 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP

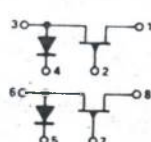


TWO CHANNEL

IH5017 ($r_{DS(ON)} \leq 100\Omega$)
IH5018 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

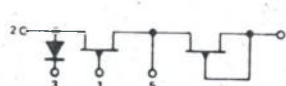


IH5019 ($r_{DS(ON)} \leq 100\Omega$)
IH5020 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

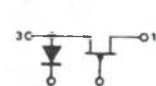


SINGLE CHANNEL

IH5021 ($r_{DS(ON)} \leq 100\Omega$)
IH5022 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



IH5023 ($r_{DS(ON)} \leq 100\Omega$)
IH5024 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

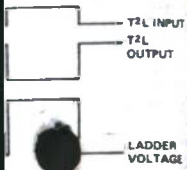
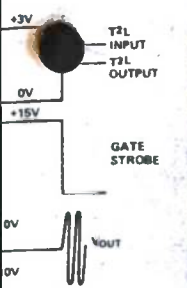


LOGIC LEVEL	PACKAGES
+15	JD,DD,PD
+5	JD,DD,PD
+15	JE,DE,PE
+5	JE,DE,PE
+15	JD,DD,PD
+5	JD,DD,PD
+15	JE,DE,PE
+5	JE,DE,PE
+15	JD,DD,PD
+5	JD,DD,PD
+15	JE,DE,PA
+5	JE,DE,PA
+15	JD,DD,PA
+5	JD,DD,PA
+15	JE,DE,PA
+5	JE,DE,PA

5°C to +125°C available

IH5040-IH5051 Family High Level CMOS Analog Gates

5043



OT to Drive
Switching (up to $\pm 10V$)

FEATURES

- Switches Greater Than 20Vpp Signals With $\pm 15V$ Supplies
- Quiescent Current Less Than $1\mu A$
- Overvoltage Protection to $\pm 25V$
- Break-Before-Make Switching t_{off} 200 nsec, t_{on} 300 nsec Typical
- T^2L , DTL, CMOS, PMOS Compatible
- Non-Latching With Supply Turn-Off
- Low $r_{DS(on)} - 35\Omega$
- New DPDT & 4PST Configurations
- Complete Monolithic Construction
IH5040 through IH5047

FUNCTIONAL DIAGRAM

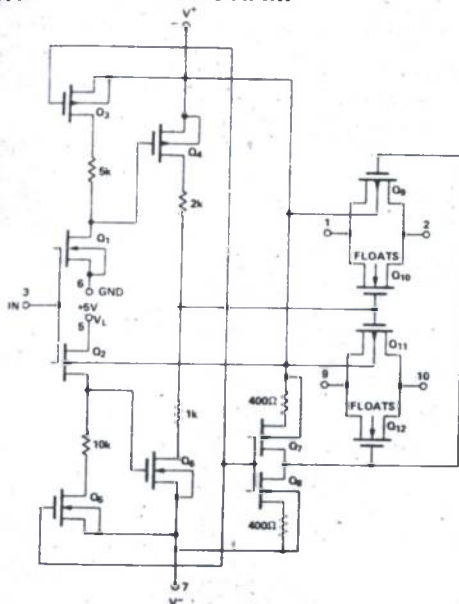
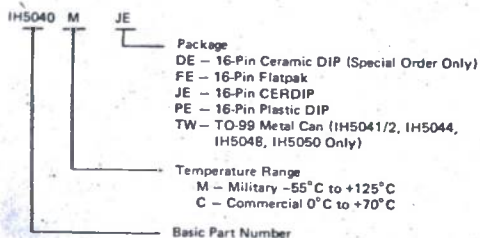


FIGURE 1. TYPICAL DRIVER, GATE - IH5042

ORDERING INFORMATION



GENERAL DESCRIPTION

The IH5040 family of solid state analog gates are designed using an improved, high voltage CMOS monolithic technology. These devices provide ease-of-use and performance advantages not previously available from solid state switches. This improved CMOS technology provides input overvoltage capability to ± 25 volts without damage to the device, and destructive latch-up of solid state analog gates has been eliminated. Early CMOS gates were destroyed when power supplies were removed with an input signal present. The IH5040 CMOS technology has eliminated this serious systems problem.

Key performance advantages of the 5040 series are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than $1\mu A$. Also designed into the 5040 is guaranteed Break-Before-Make switching, which is accomplished by extending the t_{on} time (300 nsec TYP.) so that it exceeds t_{off} time (200 nsec TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. This eliminates the need for external logic required to avoid channel to channel shorting during switching.

Many of the 5040 series improve upon and are pin-for-pin and electrical replacements for other solid state switches.

FUNCTIONAL DESCRIPTION

INTERSIL PART NO.	TYPE	$r_{DS(on)}$	PIN/FUNCTIONAL EQUIVALENT (Note 1)
IH5040	SPST	75 Ω	
IH5041	Dual SPST	75 Ω	
IH5042	SPDT	75 Ω	DG 188AA/BA
IH5043	Dual SPDT	75 Ω	DG 191AP/BP
IH5044	DPST	75 Ω	
IH5045	Dual DPST	75 Ω	DG 185AP/BP
IH5046	DPDT	75 Ω	
IH5047	4PST	75 Ω	
IH5048 Dual	SPST	35 Ω	
IH5049 Dual	DPST	35 Ω	DG 184AP/BP
IH5050	SPDT	35 Ω	DG 187AA/BA
IH5051 Dual	SPDT	35 Ω	DG 190AP/BP

NOTE 1. See Switching State diagrams for applicable package equivalency.

Pin and functional equivalent monolithic versions of the DG181, DG182, DG187 and DG188 are available. See data sheet for this and also IH181 to IH191.

ABSOLUTE MAXIMUM RATINGS

Current (Any Terminal) < 30mA
 Storage Temperature -65°C to +150°C
 Operating Temperature -55°C to +125°C
 Power Dissipation 450mW
 (All Leads Soldered to a P.C. Board)
 Derate 6mW/°C Above 70°C
 Lead Temperature (Soldering, 10 sec) 300°C

$V^+ - V^-$ < 33V
 $V^+ - V_D$ < 30V
 $V_D - V^-$ < 30V
 $V_D - V_S$ < ±22V
 $V_L - V^-$ < 33V
 $V_L - V_{IN}$ < 30V
 $V_L - GND$ < 20V
 $V_{IN} - GND$ < 20V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@ 25°C, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$)

PER CHANNEL		MIN./MAX. LIMITS							TEST CONDITIONS
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	-55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	
I _{IN(ON)}	Input Logic Current	1	1	1	1	1	1	μA	V _{IN} = 2.4 V Note 1
I _{IN(OFF)}	Input Logic Current	1	1	1	1	1	1	μA	V _{IN} = 0.8 V Note 1
r _{DS(on)}	Drain-Source On Resistance	75(35)	75(35)	150(60)	80(45)	80(45)	130(45)	Ω	(IH5048 thru IH5051) I _S = 1 mA, V _{ANALOG} = -10 V to +10 V
Δr _{DS(ON)}	Channel to Channel R _{DS(ON)} Match	25(15)	25(15)	25(15)	30(15)	30(15)	30(15)	Ω	(IH5048 thru IH5051) I _S (Each Channel) = 1 mA,
V _{ANALOG}	Min. Analog Signal Handling Capability	±11(±10)	±11(±10)	±11(±10)	±10(±10)	±10(±10)	±10(±10)	V	I _S = 10 mA (IH5048 thru IH5051)
I _{D(OFF)}	Switch OFF Leakage Current	1(1)	1(1)	100(100)	5(5)	5(5)	100(100)	nA	V _{ANALOG} = -10 V to +10 V (IH5048 thru IH5051)
I _{D(ON)} I _{S(ON)}	Switch On Leakage Current	2(2)	2(2)	200(200)	10(10)	10(10)	100(200)	nA	V _D = V _S = -10 V to +10 V (IH5048 thru IH5051)
t _{ON}	Switch "ON" Time		500(250)			500(300)		ns	R _L = 1 kΩ, V _{ANALOG} = -10 V to +10 V See Fig. A
t _{OFF}	Switch "OFF" Time		250(150)			250(150)		ns	R _L = 1 kΩ, V _{ANALOG} = -10 V to +10 V See Fig. A (IH5048 thru IH5051)
Q _(INJ)	Charge Injection		15(10)			20(10)		mV	See Fig. B (IH5048 thru IH5051)
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, R _L = 100Ω, C _L = 5 pF See Fig. C
I _{QA} ⁺	+ Power Supply Quiescent Current	1	1	10	10	10	100	μA	V ⁺ = +15 V, V ⁻ = -15 V, V _L = +5 V
I _{QA} ⁻	- Power Supply Quiescent Current	1	1	10	10	10	100	μA	V _L = +5 V
I _{LQ} ⁻	+5 V Supply Quiescent Current	1	1	10	10	10	100	μA	Switch Duty Cycle ≤ 10%
I _{GND}	Gnd Supply Quiescent Current	1	1	10	10	10	100	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off; Any Other Channel Switches as per Fig. E

TEST CIRCUITS

FIG. A

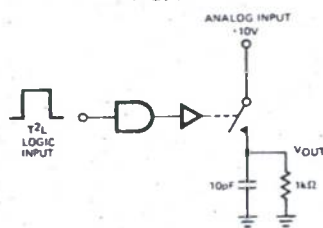


FIG. B

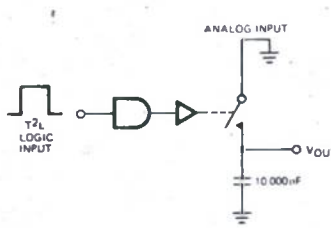
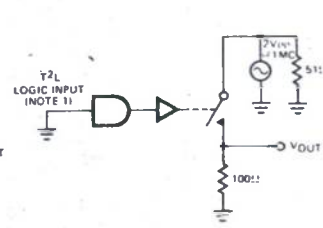


FIG. C



NOTE 1: Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

SWITCHING STATE DIAGRAMS

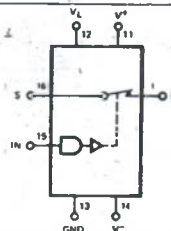
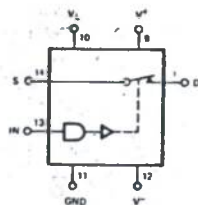
SWITCH STATES
ARE FOR LOGIC "1" INPUT

(OUTLINE DWG
FE-2)

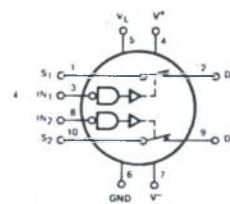
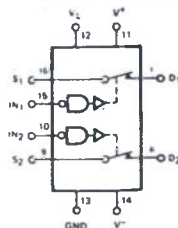
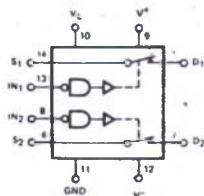
(OUTLINE DWGS
DE, JE, PE)

(OUTLINE DWG TO-100)

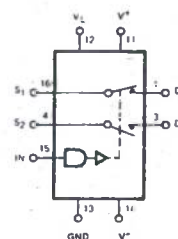
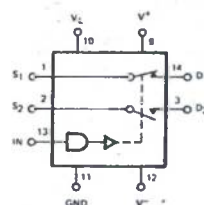
SPST
IH5040 ($r_{DS(on)} < 75\Omega$)



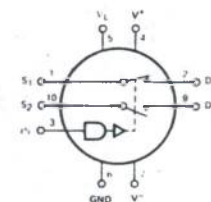
DUAL SPST
IH5041 ($r_{DS(on)} < 75\Omega$)



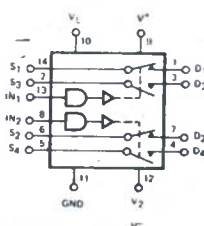
SPDT
IH5042 ($r_{DS(on)} < 75\Omega$)



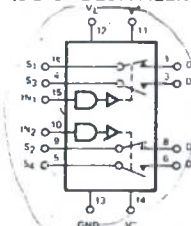
(DG188 EQUIVALENT)



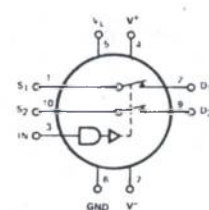
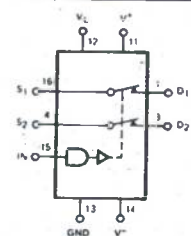
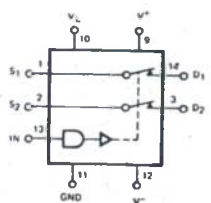
DUAL SPDT
IH5043 ($r_{DS(on)} < 75\Omega$)



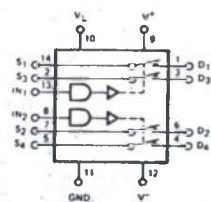
(DG191 EQUIVALENT)



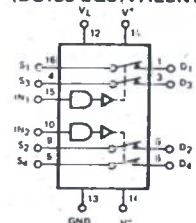
DPST
IH5044 ($r_{DS(on)} < 75\Omega$)

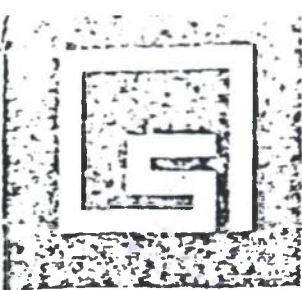


DUAL DPST
IH5045 ($r_{DS(on)} < 75\Omega$)



(DG185 EQUIVALENT)





HIGH SPEED ANALOG COMPARATOR

SIGNETICS MONOLITHIC LINEAR CIRCUITS

SEE26A
NE526A
SE526G
NE526G
SE526K
NE526K

DESCRIPTION

The 526 is a high speed analog comparator intended for use in systems where low propagation delay and fast recovery from common mode or differential input overdrive is required. The device is specifically designed to provide a wide input common mode range while operating from power supplies commonly found in digital logic systems.

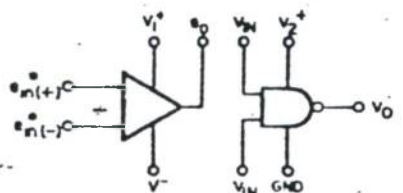
The 526 consists of a medium gain, high frequency differential amplifier and a high speed TTL gate fabricated within a single substrate by planar and epitaxial techniques. The output gate of the 526 has voltage and current capabilities compatible with DCL, DTL and TTL. The 526 output gate has a full fan-out of 10 to standard TTL loads.

The amplifier and gate may be used independently or cascaded for applications as a voltage comparator, digital line receiver or sense amplifier. The second gate input is used to provide strobe capability when operating the amplifier and gate in cascade. Additional applications information can be found under "Usage Information" in this data sheet.

FEATURES

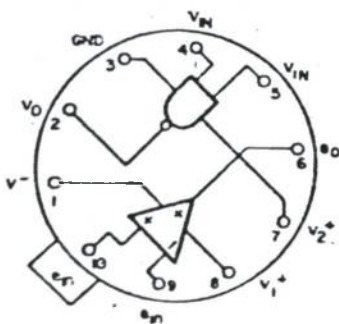
- PROPAGATION DELAY - 30ns
- INPUT COMMON MODE RANGE - +4.5V
-3.5V
- DIFFERENTIAL OVERDRIVE RECOVERY - 20ns
- OUTPUT COMPATIBLE WITH STANDARD LOGIC FORMS
- OPERATES FROM STANDARD $\pm 5V$ SUPPLIES

PIN CONFIGURATIONS

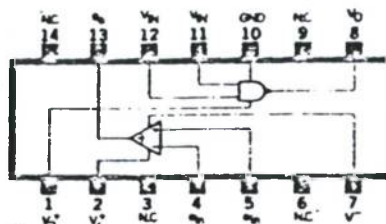


* INVERTING AND NON-INVERTING INPUTS ARE DEFINED RELATIVE TO AMPLIFIER OUTPUT, V_0

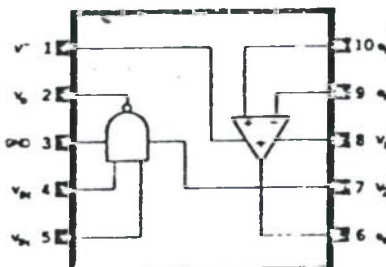
K PACKAGE



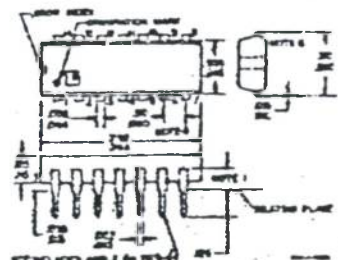
A PACKAGE



G PACKAGE



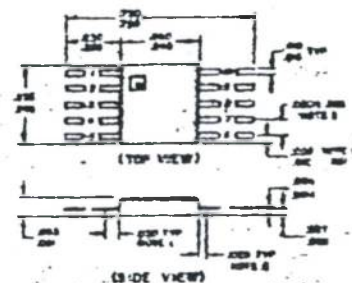
A PACKAGE (TO-116)



- NOTES: (1) Lead spacing shall be measured within this area.
(2) Standard Plastic Body.
(3) Solder Leads.
(4) Lead spacing intervals are non-uniform.
(5) Thermal resistance from junction to still air, $\theta_{JA} = 0.16^\circ C/W$.
(6) Leads shown as positioned by Signetics and in-line package series.
(7) All dimensions of plastic package include molding compound flash.

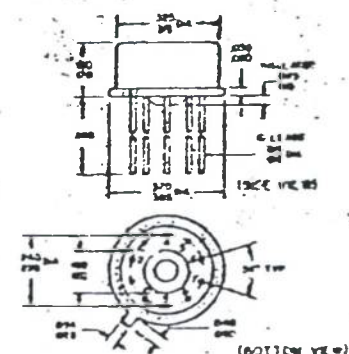
G PACKAGE (TO-91)

(RECTANGULAR GLASS-EPDM)



- NOTES: (1) Recommended minimums of lead height lead flat.
(2) AC leads available and solderable.
(3) Pin 1 internally connected to case.
(4) All dimensions in inches.
(5) Tolerances are non-uniform.
(6) Lead spacing dimensions apply to this area only.
(7) Signetics symbol on G package bottom lead flat.
(8) Thermal resistance (with G and K packages) from junction to case, $\theta_{JC} = 0.2^\circ C/mW$.

K PACKAGE (TO-100)



RECOMMENDED OPERATING SUPPLY VOLTAGES: $V_1^+ = V_2^+ = 5.0V$, $V^- = -5.0V$

ABSOLUTE MAXIMUM RATINGS*

SUPPLY VOLTAGE	±7.0V	STORAGE TEMPERATURE	-65°C to +150°C
GATE INPUT VOLTAGE	+6.0V	OPERATING TEMPERATURE	
DIFFERENTIAL INPUT VOLTAGE	+5.0V	SE526	-55°C to +125°C
COMMON MODE INPUT VOLTAGE	±5.0V	NE526	0°C to +75°C
GATE OUTPUT CURRENT	±100mA		

* Absolute Maximum Ratings are limiting values above which serviceability may be impaired

ELECTRICAL CHARACTERISTICS (NOTES 1, 2, 3, 4, 13, 14) - STANDARD CONDITIONS $V_1^+ = V_2^+ = 5.0V$, $V^- = -5.0V$

ACCEPTANCE TEST SUBGROUP	CHARACTERISTIC	SYMBOL	LIMITS				TEST CONDITIONS		NOTES	
							TEMPERATURE			TEST CIRCUIT
			MIN.	TYP.	MAX.	UNIT	SE526	NE526		
A-5	Input Offset Voltage	V_{io}		2.0	5.0	mV	-55°C	+ 0°C	Figure 1	5
A-7		V_{io}		2.0	5.0	mV	+25°C	+25°C	Figure 1	5
A-8		V_{io}		2.0	5.0	mV	+125°C	+75°C	Figure 1	5
A-4	Input Bias Current	I_{in}		30.0	35.0	μA	-55°C	0°C	Figure 2	6
A-7		I_{in}		25.0	35.0	μA	+25°C	+25°C	Figure 2	6
A-6		I_{in}		22.0	35.0	μA	+125°C	+75°C	Figure 2	6
A-4	Input Offset Current	I_{io}		0.8	5.0	μA	-55°C	0°C	Figure 2	
A-7		I_{io}		0.5	5.0	μA	+25°C	+25°C	Figure 2	
A-3		I_{io}		0.4	5.0	μA	+125°C	+75°C	Figure 2	
A-4	Input Common Mode Range	V_{cm}	+4.2	+4.7		V	-55°C	0°C	Figure 1	
A-2		V_{cm}	+4.2	+4.5		V	+25°C	+25°C	Figure 1	
A-6		V_{cm}	+4.2	+4.4		V	+125°C	+75°C	Figure 1	
A-4		V_{cm}	-3.2	-3.5		V	-55°C	0°C	Figure 1	
A-2		V_{cm}	-3.2	-3.5		V	+25°C	+25°C	Figure 1	
A-5		V_{cm}	-3.2	-3.5		V	+125°C	+75°C	Figure 1	
A-6	Amplifier Output Voltage	V_{ohi}	3.5			V	-55°C	0°C	Figure 3	
A-2		V_{ohi}	3.5			V	+25°C	+25°C	Figure 3	
A-4		V_{ohi}	3.5			V	+125°C	+75°C	Figure 3	
A-6		V_{olo}			0.8	V	-55°C	0°C	Figure 3	
A-2		V_{olo}			0.5	V	+25°C	+25°C	Figure 3	
A-4		V_{olo}			0.4	V	+125°C	+75°C	Figure 3	
A-1	Amplifier Power Consumption	P_d		90	120	mW	-55°C	0°C	Figure 4	
A-2		P_d		100	120	mW	+25°C	+25°C	Figure 4	
A-4		P_d		110	120	mW	+125°C	+75°C	Figure 4	
A-5	Gate Output Voltage	V_{1o}	2.8	3.5		V	-55°C	0°C	Figure 5	7, 8
A-3		V_{1o}	2.8	3.2		V	+25°C	+25°C	Figure 5	7, 8
A-4		V_{1o}	2.8	3.0		V	+125°C	+75°C	Figure 5	7, 8
A-6		V_{0o}		0.3	0.4	V	-55°C	0°C	Figure 5	7, 8
A-2		V_{0o}		0.2	0.4	V	+25°C	+25°C	Figure 5	7, 8
A-4		V_{0o}		0.3	0.4	V	+125°C	+75°C	Figure 5	7, 8
A-1	Gate Output Sink Current	I_{0o}	18.0			mA	+25°C	+25°C	Figure 5	8
A-2	Gate Output Source Current	I_{1o}	1.0			mA	+25°C	+25°C	Figure 5	7
A-3	Gate Input Threshold Voltage	V_{1i}	2.0			V	-55°C	0°C	Figure 5	9
A-4		V_{1i}	2.0			V	+25°C	+25°C	Figure 5	9
A-5		V_{1i}	2.0			V	+125°C	+75°C	Figure 5	9
A-6		V_{0i}			1.0	V	-55°C	0°C	Figure 5	10
A-2		V_{0i}			0.9	V	+25°C	+25°C	Figure 5	10
A-4		V_{0i}			0.8	V	+125°C	+75°C	Figure 5	10

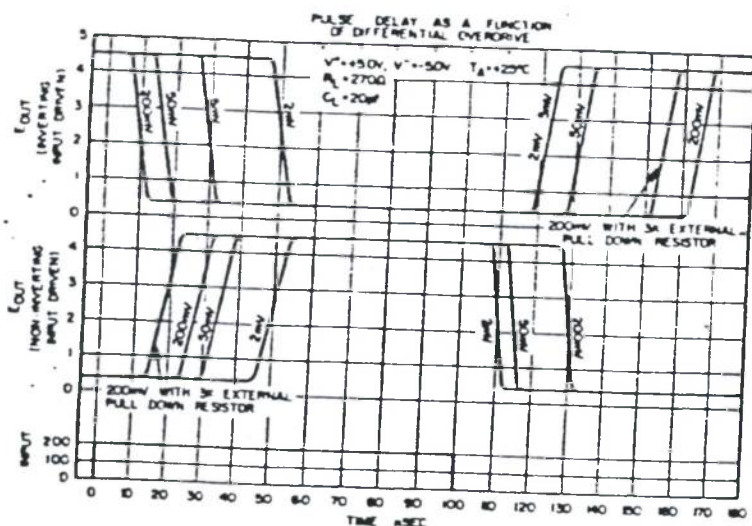
Comments

Notes

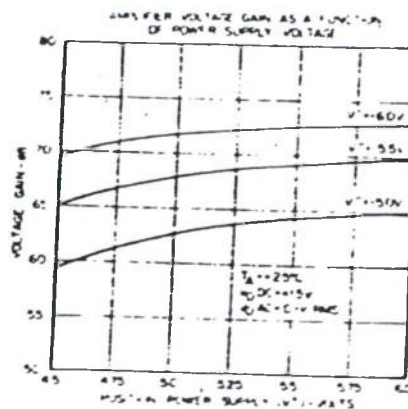
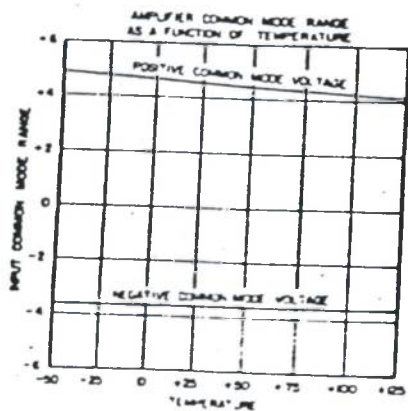
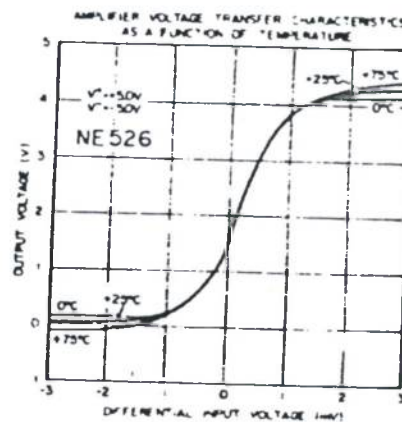
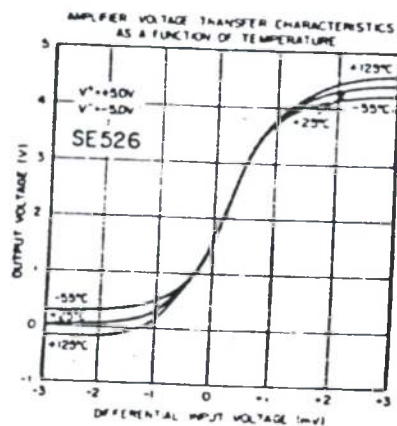
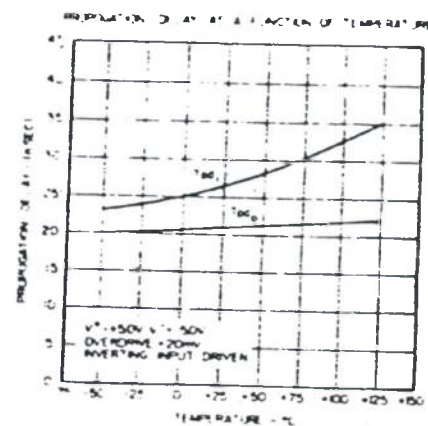
1. All measurements are referenced to the ground terminal.
2. Positive current is defined as into the pin referenced.
3. Pins not specifically referenced are left electrically open.
4. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
5. Input Offset Voltage is tested at guaranteed Input Common Mode Range voltage limits and includes the worst-case variations of voltage gain and input impedance. These are the maximum values required to drive the output down to "0" or up to "1".
6. Input Bias Current is defined as the maximum current required to bias either input.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{DD} .
9. These limits are guaranteed by Gate Output Voltage (V_{O1}) test.
10. These limits are guaranteed by Gate Output Voltage (V_{O2}) test.
11. Load capacitance includes test fixture and probe capacitance.
12. Differential Input Voltage = 500mV for this test.
13. Acceptance Test Subgroup A.7 provides end point parameters for linear devices processed to Signetics SURE Program. See Signetics SURE Bulletin 5001.
14. Manufacturer reserves the right to make design and process changes and improvements.

NOTES: COMPONENT VALUES ARE TYPICAL
 * 100V 100V DIODES

TYPICAL OPERATING LIMITS



Pulse delay curves illustrate propagation delay at the leading edge and differential overload recovery at the trailing edge



USAGE INFORMATION

The 526 is designed for use in voltage comparator and sense amplifier applications. Because of its high voltage gain and high speed, care must be taken in its circuit application to ensure stable operation. The power supplies must be bypassed for frequencies as high as 50MHz. The source impedances should be kept as small as feasible and the inputs should be kept well isolated from the output to avoid generating a positive feedback loop. To optimize the effective input offset voltage external resistance used in the bases of the input transistors should be kept equal (Figure 1).

The amplifier and gate circuits are completely independent, making their external connection very versatile and capable of performing a multitude of functions. For most applications, the amplifier will be connected directly to the gate. The parasitic capacitance at the interconnecting point must be minimized if the propagation delay of the circuit is to be optimized. It is permissible to connect an external discrete resistor from the amplifier output to the negative supply (Figure 2). The increased sink capability resulting from this connection tends to reduce the propagation delay. The external pull-down resistor should be no less than 5000 ohms. The remaining gate input may be used to strobe the output of the amplifier output.

An external NAND gate may be cross-coupled with the gate output of the 526 to provide a bi-stable latch or storage element. In this application, the differential inputs of the amplifier should be biased such that the amplifier output will be positive when no input signal is present, i.e. the non-inverting input should be biased with respect to the inverting input (Figure 3).

Amplifier outputs may be tied together to provide the logical OR of the amplifier outputs (Figure 4). This technique will tend to increase propagation delay because of the parasitic capacitances associated with the connection.

The amplifier of one 526 may be used to drive the second gate input (strobe) of another 526, performing the logical NAND of the amplifier outputs. This configuration removes the strobe capability of the output (Figure 5). In either of these configurations, the unused 526 gate may be used to implement other system logic requirements.

The power supply inputs for the gate and amplifier are independent. Where power consumption is critical, the amplifier may be disabled while maintaining a logical 1 output at the gate. Total power consumption is reduced to about 20% of the power required for normal operation.

FIGURE 1

MINIMIZING EFFECTIVE INPUT OFFSET VOLTAGE

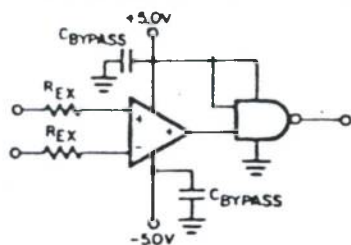


FIGURE 2

DECREASING PROPAGATION DELAY BY ADDITION OF EXTERNAL PULL DOWN RESISTOR

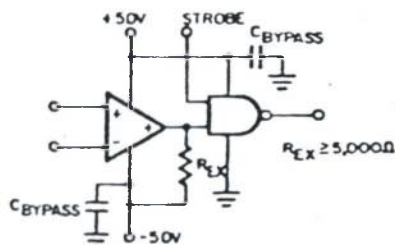


FIGURE 3

INCORPORATING EXTERNAL NAND GATE TO PROVIDE OUTPUT STORAGE

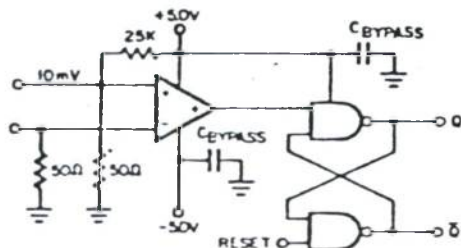


FIGURE 4

PARALLELING AMPLIFIER OUTPUTS PROVIDE THE LOGICAL OR OF THE AMPLIFIER OUTPUTS

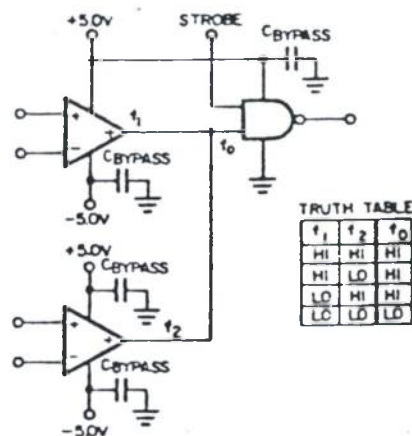
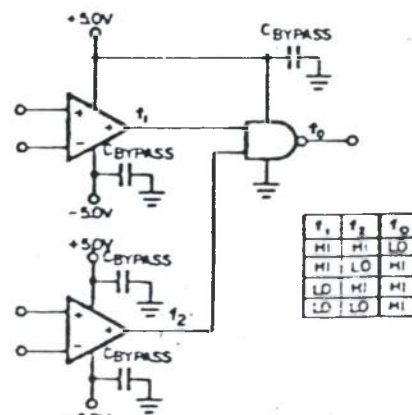
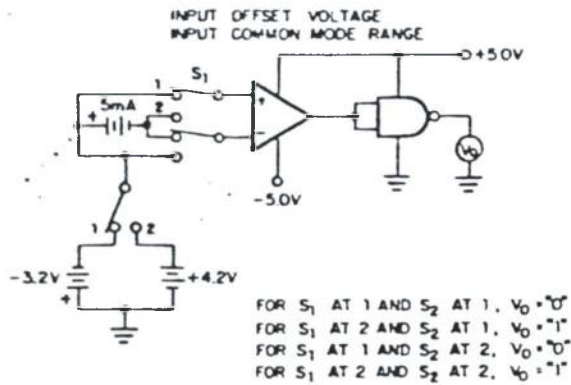


FIGURE 5

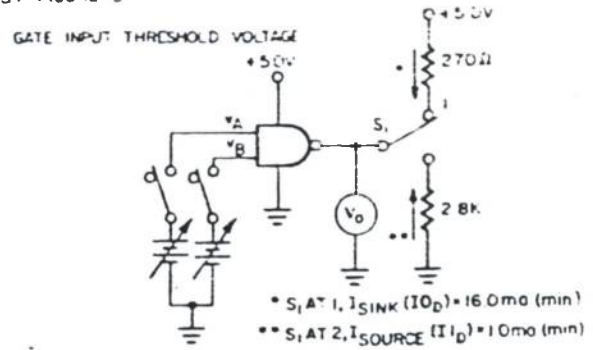
LOGICAL NAND OF THE AMPLIFIER OUTPUTS



TEST FIGURE 1

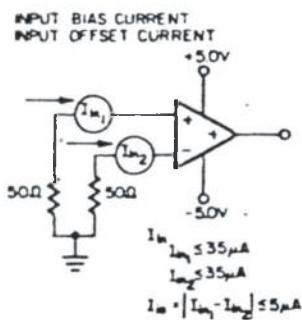


TEST FIGURE 5

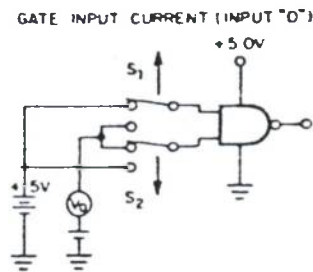


TEST NO	INPUT CONDITION	-55°C/0°C	+25°C	+125°C/75°C	OUTPUT
1	V_A V_B	2.0V 2.0V	2.0V 2.0V	2.0V 2.0V	V_{CC}
2	V_A V_B	1.0V OPEN	0.9V OPEN	0.8V OPEN	V_{IO}
3	V_A V_B	OPEN 1.0V	OPEN 0.9V	OPEN 0.8V	V_{IC}

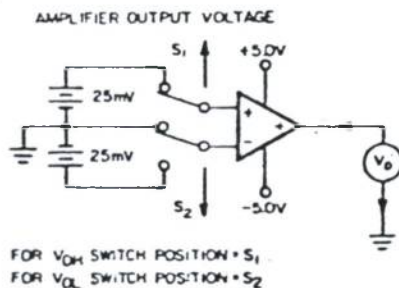
TEST FIGURE 2



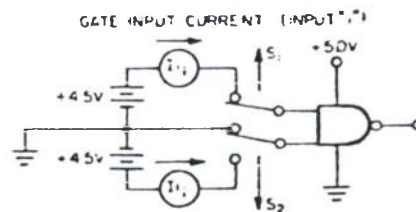
TEST FIGURE 6



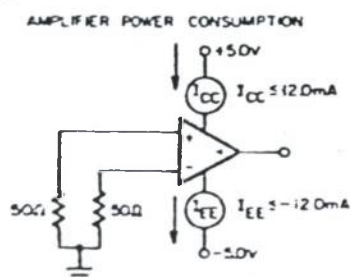
TEST FIGURE 3



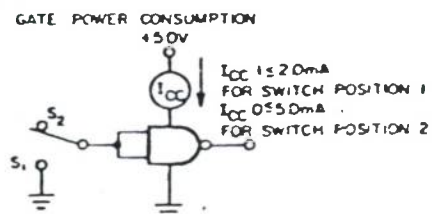
TEST FIGURE 7



TEST FIGURE 4

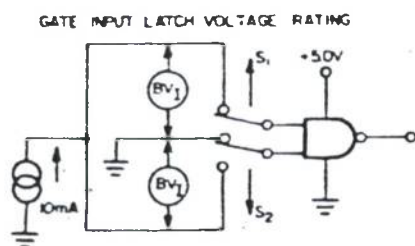


TEST FIGURE 8

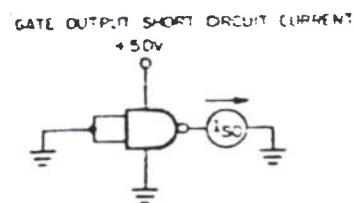


SE525A
NE526A
SE526G
NE526G
SE526K
NE526K

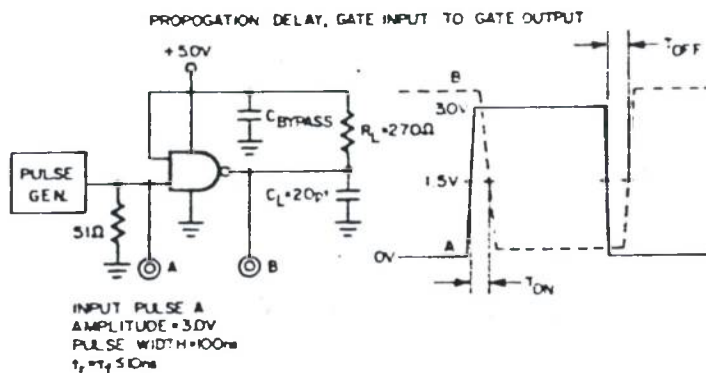
TEST FIGURE 9



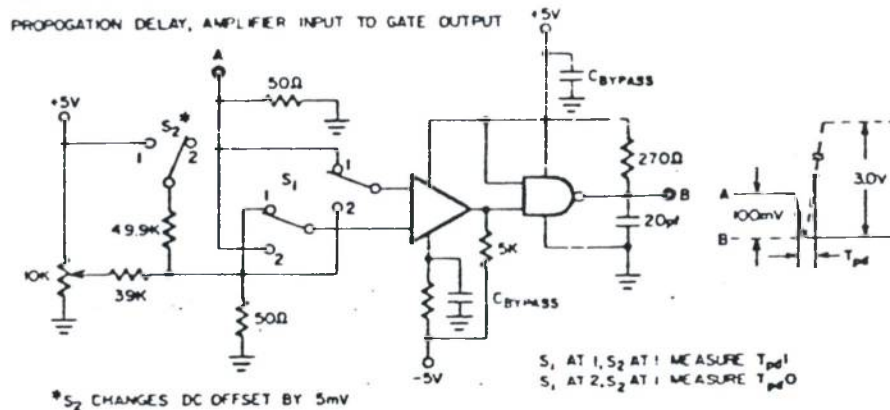
TEST FIGURE 10



TEST FIGURE 11

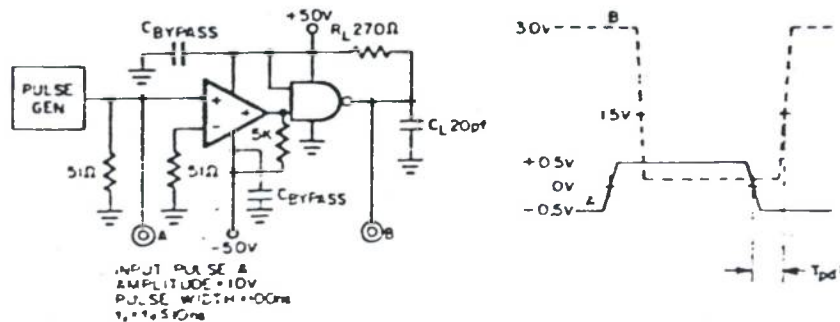


TEST FIGURE 12



TEST FIGURE 13

DIFFERENTIAL OVERLOAD RECOVERY TIME, AMPLIFIER INPUT TO GATE OUTPUT



DESCRIPTION

The 532 consists of two independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

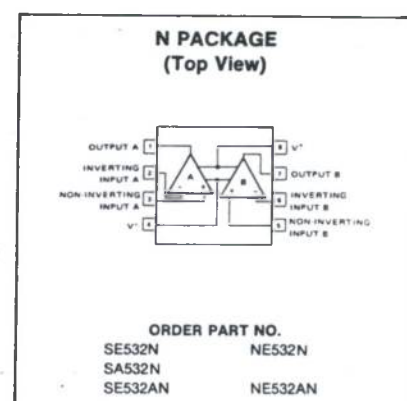
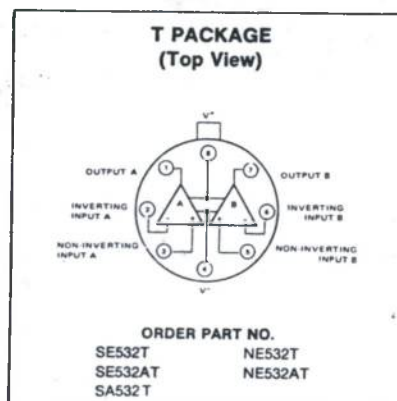
FEATURES

- Internally frequency compensated for unity gain
- Large dc voltage gain—(100dB)
- Wide bandwidth (unity gain)—1MHz (temperature compensated)
- Wide power supply range
single supply—(3Vdc to 30Vdc)
or dual supplies—(± 1.5 Vdc to ± 15 Vdc)
- Very low supply current drain (400 μ A)—essentially independent of supply voltage (1mW/op amp at +5Vdc)
- Low input biasing current—(45nA dc temperature compensated)
- Low input offset voltage—(2mVdc) and offset current—(5nA dc)
- Differential input voltage range equal to the power supply voltage
- Large output voltage—(0Vdc to $V^+ - 1.5$ Vdc swing)
- SE532 MII std 883A,B,C available

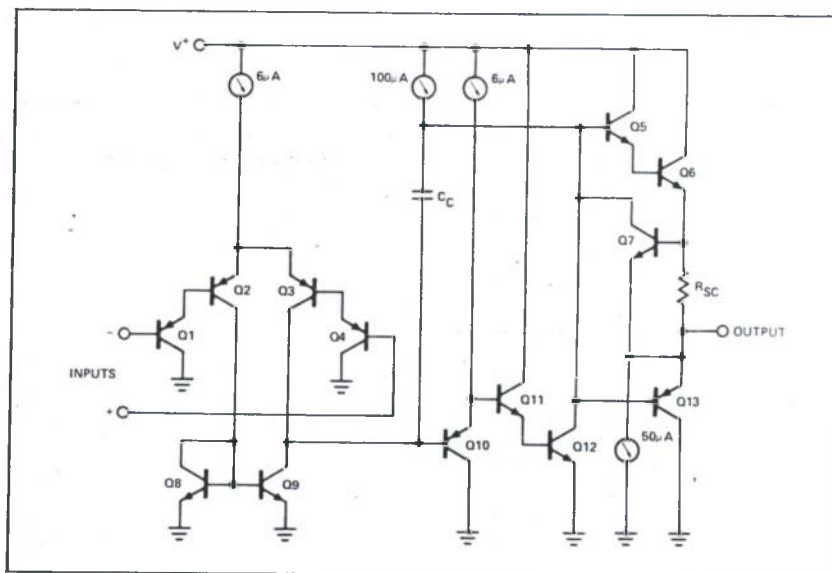
UNIQUE FEATURES

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature compensated. The input bias current is also temperature compensated.

PIN CONFIGURATIONS



EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, V^+	32 or ± 16	Vdc
Differential input voltage	32	Vdc
Input voltage	-0.3 to +32	Vdc
Power dissipation		
T package	680	mW
N package	625	mW
Output short-circuit to GND $V^+ < 15$ Vdc and $T_A = 25^\circ\text{C}$	Continuous	
Operating temperature range		
NE532	0 to +70	$^\circ\text{C}$
SA532	-40 to +85	$^\circ\text{C}$
SE532	-55 to +125	$^\circ\text{C}$
Storage temperature range	-65 to +150	$^\circ\text{C}$
Lead temperature (soldering, 10sec)	300	$^\circ\text{C}$

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_+ = +5\text{V}$ unless otherwise specified (see Notes on following page).

PARAMETER	TEST CONDITIONS	SE532			NE532			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{OS} Offset voltage ¹	$R_S \leq 10\text{k}$ $R_S \leq 10\text{k}\Omega$, over temp.		± 2	± 5 ± 7		± 2	± 6 ± 7.5	mV mV
V _{OS} Drift	$R_S = 0\Omega$, over temp.		7			7		$\mu\text{V}/^\circ\text{C}$
I _{OS} Offset current	I _{IN} (+) or I _{IN} (-)		± 3	± 30		± 5	± 50	nA
I _{OS} Offset current	Over temp.			± 100			± 150	nA
I _{OS} Drift	Over temp.		10			10		$\text{pA}/^\circ\text{C}$
I _{BIAS} Input current ²	I _{IN} (+) or I _{IN} (-) Over temp., I _{IN} (+) or I _{IN} (-)		45 40	150 300		45 40	250 500	nA nA
V _{CM} Common mode voltage range ³	$V_+ = 30\text{V}$ Over temp., $V_+ = 30\text{V}$	0		$V_+ - 1.5$ $V_+ - 2.0$	0		$V_+ - 1.5$ $V_+ - 2.0$	V V
CMRR Common mode rejection ratio	$R_S \leq 10\text{k}\Omega$	70	85		65	70		dB
V _{OUT} Output voltage swing (V _{OH})	$R_L \geq 2\text{k}\Omega$, $V_+ = 30\text{V}$	26			26			V
V _{OUT} Output voltage swing (V _{OL})	$R_L \geq 10\text{k}\Omega$, $V_+ = 30\text{V}$ $R_L \leq 10\text{k}\Omega$, over temp.	27	28 5	20	27	28 5	20	V mV
I _{CC} Supply current	$R_L = \infty$ on all amplifiers, over temp.		0.5	1.2		0.5	1.2	mA
A _{VOL} Large signal voltage Gain	$R_L \geq 2\text{k}\Omega$, V _{OUT} $\pm 10\text{V}$, V _S = $\pm 15\text{V}$ Over temp.	50 25	100		25 15	100		V/mV V/mV
PSRR Supply voltage rejection ratio	$R_S \leq 10\text{k}\Omega$	65	100		65	100		dB
Amplifier-to-amplifier coupling ⁴	f = 1kHz to 20kHz (input referred)		-120			-120		dB
Output current source	V _{IN} = 1Vdc, V _{IN} = 0Vdc, V ₊ = 15Vdc	20	40		20	40		mA
Output current sink	V _{IN} = 1Vdc, V _{IN} = 0Vdc, V ₊ = 15Vdc	10	20		10	20		mA
I _{SC} ⁵	V _{IN} = 1Vdc, V _{IN} = 0Vdc, V _{OUT} = 200mVdc	12	50 40	60	12	50 40	60	μA mA

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25^\circ\text{C}$, $V_+ = +5\text{V}$ unless otherwise specified (see Notes on following page).

PARAMETER	TEST CONDITIONS	SA532			SE532A			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{OS} Offset voltage ¹	$R_S \leq 10\text{k}$ $R_S \leq 10\text{k}\Omega$, over temp.		± 2	± 6 ± 7.5		1	2 4	mV mV
V _{OS} Drift	$R_S = 0\Omega$, over temp.		7			7	15	$\mu\text{V}/^\circ\text{C}$
I _{OS} Offset current	I _{IN} (+) or I _{IN} (-)		± 5	± 50		2	10	nA
I _{OS} Offset current	Over temp.			± 150			30	nA
I _{OS} Drift	Over temp.		10			10	200	$\text{pA}/^\circ\text{C}$
I _{BIAS} Input current ²	I _{IN} (+) or I _{IN} (-) Over temp., I _{IN} (+) or I _{IN} (-)		45 40	250 500		20 40	50 100	nA nA
V _{CM} Common mode voltage range ³	$V_+ = 30\text{V}$ Over temp., $V_+ = 30\text{V}$	0		$V_+ - 1.5$ $V_+ - 2.0$	0		$V_+ - 1.5$ $V_+ - 1.5$	V V
CMRR Common mode rejection ratio	$R_S \leq 10\text{k}\Omega$	65	70		70	85		dB
V _{OUT} Output voltage swing (V _{OH})	$R_L \geq 2\text{k}\Omega$, $V_+ = 30\text{V}$	26						V
V _{OUT} Output voltage swing (V _{OL})	$R_L \geq 10\text{k}\Omega$, $V_+ = 30\text{V}$ $R_L \leq 10\text{k}\Omega$, over temp.	27	28 5	20				V mV
I _{CC} Supply current	$R_L = \infty$ on all amplifiers, over temp.		0.5	1.2		0.5	1.2	mA
A _{VOL} Large signal voltage Gain	$R_L \geq 2\text{k}\Omega$, V _{OUT} $\pm 10\text{V}$, V _S = $\pm 15\text{V}$ Over temp.	25 15	100		50 25	100		V/mV V/mV
PSRR Supply voltage rejection ratio	$R_S \leq 10\text{k}\Omega$	65	100		65	100		dB
Amplifier-to-amplifier coupling ⁴	f = 1kHz to 20kHz (input referred)		-120			-120		dB
Output current source	V _{IN} = 1Vdc, V _{IN} = 0Vdc, V ₊ = 15Vdc	20	40		20	40		mA
Output current sink	V _{IN} = 1Vdc, V _{IN} = 0Vdc, V ₊ = 15Vdc	10	20		10	20		mA
I _{SC} ⁵	V _{IN} = 1Vdc, V _{IN} = 0Vdc, V _{OUT} = 200mVdc	12	50 40	60	12	50 40	60	μA mA

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25^\circ\text{C}$, $V_+ = +5\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	NE532A			UNIT
		Min	Typ	Max	
V_{OS} Offset voltage ¹	$R_S \leq 10\text{k}$ $R_S \leq 10\text{k}\Omega$, over temp.		2	3 5	mV mV
V_{OS} Drift	$R_S = 0\Omega$, over temp.		7	20	$\mu\text{V}/^\circ\text{C}$
I_{OS} Offset current	$I_{IN(+)} \text{ or } I_{IN(-)}$		5	30	nA
I_{OS} Offset current	Over temp.			75	nA
I_{OS} Drift	Over temp.		10	300	$\text{pA}/^\circ\text{C}$
I_{BIAS} Input current ²	$I_{IN(+)} \text{ or } I_{IN(-)}$ Over temp., $I_{IN(+)} \text{ or } I_{IN(-)}$		45 40	100 200	nA nA
V_{CM} Common mode voltage range ³	$V_+ = 30\text{V}$ Over temp., $V_+ = 30\text{V}$	0 0		$V_+ - 1.5$ $V_+ - 1.5$	V V
$CMRR$ Common mode rejection ratio	$R_S \leq 10\text{k}\Omega$	65	85		dB
V_{OUT} Output voltage swing (V_{OH})	$R_L \geq 2\text{k}\Omega$, $V_+ = 30\text{V}$				V
V_{OUT} Output voltage swing (V_{OL})	$R_L \geq 10\text{k}\Omega$, $V_+ = 30\text{V}$ $R_L \leq 10\text{k}\Omega$, over temp.				V mV
I_{CC} Supply current	$R_L = \infty$ on all amplifiers, over temp.		0.5	1.2	mA
A_{VOL} Large signal voltage Gain	$R_L \geq 2\text{k}\Omega$, $V_{OUT} \pm 10\text{V}$, $V_S = \pm 15\text{V}$ Over temp.	25 15	100		V/mV V/mV
$PSRR$ Supply voltage rejection ratio	$R_S \leq 10\text{k}\Omega$	65	100		dB
Amplifier-to-amplifier coupling ⁴	$f = 1\text{kHz}$ to 20kHz (input referred)		-120		dB
Output current source	$V_{IN+} = 1\text{Vdc}$, $V_{IN-} = 0\text{Vdc}$, $V_+ = 15\text{Vdc}$	20	40		mA
Output current sink	$V_{IN-} = 1\text{Vdc}$, $V_{IN+} = 0\text{Vdc}$, $V_+ = 15\text{Vdc}$	10	20		mA
I_{SC} ⁵	$V_{IN-} = 1\text{Vdc}$, $V_{IN+} = 0\text{Vdc}$, $V_{OUT} = 200\text{mVdc}$	12	50 40	60	μA mA

NOTES

- $V_O = 1.4\text{V}$, $R_S = 0\Omega$ with V_+ from 5V to 30V ; and over the full input common-mode range (9V to $V_+ - 1.5\text{V}$).
- The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
- The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V . The upper end of the common-mode voltage range

is $V_+ - 1.5\text{V}$, but either or both inputs can go to $+32\text{V}$ without damage.

- Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive coupling increases at higher frequencies.
- Short circuits from the output to V_+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V_+ . At values of supply voltage in excess of $+15\text{Vdc}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.

FEATURES

Pretrimmed to $\pm 0.25\%$ max 4-Quadrant Error (AD534L)
All Inputs (X, Y and Z) Differential, High Impedance for
 $[(X_1 - X_2)(Y_1 - Y_2)/10] + Z_2$ Transfer Function
Scale-Factor Adjustable to Provide up to X100 Gain
Low Noise Design: $90\mu\text{V rms}$, 10Hz-10kHz
Low Cost, Monolithic Construction
Excellent Long Term Stability

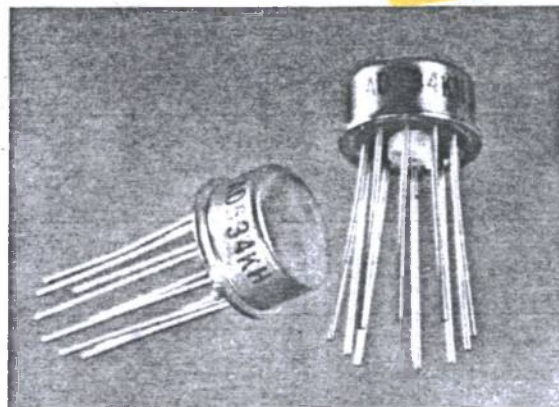
APPLICATIONS

High Quality Analog Signal Processing
Differential Ratio and Percentage Computations
Algebraic and Trigonometric Function Synthesis
Wideband, High-Crest rms-to-dc Conversion
Accurate Voltage Controlled Oscillators and Filters

PRODUCT DESCRIPTION

The AD534 is a monolithic laser trimmed four-quadrant multiplier divider having accuracy specifications previously found only in expensive hybrid or modular products. A maximum multiplication error of $\pm 0.25\%$ is guaranteed for the AD534L without any external trimming. Excellent supply rejection, low temperature coefficients and long term stability of the on-chip thin film resistors and buried zener reference preserve accuracy even under adverse conditions of use. It is the first multiplier to offer fully differential, high impedance operation on all inputs, including the Z-input, a feature which greatly increases its flexibility and ease of use. The scale factor is pretrimmed to the standard value of 10.00; by means of an external resistor, this can be reduced to values as low as 3, with corresponding reductions in bias current and noise level.

The wide spectrum of applications and the availability of several grades commend this multiplier as the first choice for all new designs. The AD534J ($\pm 1\%$ max error), AD534K ($\pm 0.5\%$ max) and AD534L ($\pm 0.25\%$ max) are specified for operation over the 0 to $+70^\circ\text{C}$ temperature range. The AD534S ($\pm 1\%$ max) and AD534T ($\pm 0.5\%$ max) are specified over the extended temperature range, -55°C to $+125^\circ\text{C}$. All grades are available in hermetically sealed TO-100 metal cans and TO-116 ceramic DIP packages.



PROVIDES GAIN WITH LOW NOISE

The AD534 is the first general purpose multiplier capable of providing gains up to X100, frequently eliminating the need for separate instrumentation amplifiers to precondition the inputs. The AD534 can be very effectively employed as a variable gain differential input amplifier with high common mode rejection. The gain option is available in all modes, and will be found to simplify the implementation of many function-fitting algorithms such as those used to generate sine and tangent. The utility of this feature is enhanced by the inherent low noise of the AD534: $90\mu\text{V rms}$ (depending on the gain), a factor of 10 lower than previous monolithic multipliers. Drift and feedthrough are also substantially reduced over earlier designs.

UNPRECEDENTED FLEXIBILITY

The precise calibration and differential Z-input provide a degree of flexibility found in no other currently available multiplier. Standard MDSSR functions (multiplication, division, squaring, square-rooting) are easily implemented while the restriction to particular input/output polarities imposed by earlier designs has been eliminated. Signals may be summed into the output, with or without gain and with either a positive or negative sense. Many new modes based on implicit-function synthesis have been made possible, usually requiring only external passive components. The output can be in the form of a current, if desired, facilitating such operations as integration.

SPECIFICATIONS

(typical at +25°C, with $\pm V_S = 15V$, $R_L \geq 2k$, unless otherwise stated)

PARAMETER	CONDITIONS	AD534J	AD534K	AD534L	AD534S	AD534T
MULTIPLIER PERFORMANCE						
Transfer Function		$(X_1 - X_2)(Y_1 - Y_2) \div Z_2$	•	•	•	•
Total Error ¹	-10V $\leq X, Y \leq$ +10V $T_A = \text{min to max}$ $V_S = \pm 14V \text{ to } \pm 16V$	$\pm 1.0\% \text{ max}$	$\pm 0.5\% \text{ max}$	$\pm 0.25\% \text{ max}$	•	•
vs. Temperature		$\pm 0.022\%/^{\circ}\text{C}$	$\pm 0.015\%/^{\circ}\text{C}$	$\pm 0.008\%/^{\circ}\text{C}$	$\pm 0.02\%/^{\circ}\text{C max}$	$\pm 0.01\%/^{\circ}\text{C max}$
Scale Factor Error	SF = 10.00 nominal ²	$\pm 0.25\%$	$\pm 0.1\%$	•	•	•
Temperature-Coefficient of						
Scaling-Voltage	$T_A = \text{min to max}$	$\pm 0.02\%/^{\circ}\text{C}$	$\pm 0.01\%/^{\circ}\text{C}$	$\pm 0.005\%/^{\circ}\text{C}$	•	$\pm 0.005\%/^{\circ}\text{C max}$
Supply Rejection	$\pm V_S = (15V) \pm 1V$	$\pm 0.01\%$	•	•	•	•
Nonlinearity, X	X = 20V pk-pk Y = $\pm 10V$	$\pm 0.4\%$	$\pm 0.2\% (0.3\% \text{ max})$	$\pm 0.1\% (0.12\% \text{ max})$	•	•
Nonlinearity, Y	Y = 20V pk-pk X = $\pm 10V$	$\pm 0.01\%$	$\pm 0.01\% (\pm 0.1\% \text{ max})$	$\pm 0.005\% (\pm 0.1\% \text{ max})$	•	•
Feedthrough ³ , X	Y nulled X = 20V pk-pk 50Hz	$\pm 0.3\%$	$\pm 0.15\% (0.3\% \text{ max})$	$\pm 0.05\% (0.12\% \text{ max})$	•	•
Feedthrough ³ , Y	X nulled Y = 20V pk-pk 50Hz	$\pm 0.01\%$	$\pm 0.01\% (\pm 0.1\% \text{ max})$	$\pm 0.003\% (\pm 0.1\% \text{ max})$	•	•
Output Offset Voltage		$\pm 5mV (\pm 30mV \text{ max})$	$\pm 2mV (\pm 15mV \text{ max})$	$\pm 2mV (\pm 10mV \text{ max})$	•	•
Drift	$T_A = \text{min to max}$	$200\mu V/^{\circ}\text{C}$	$100\mu V/^{\circ}\text{C}$	•	$500\mu V/^{\circ}\text{C max}$	$300\mu V/^{\circ}\text{C max}$
DYNAMICS						
Small-Signal BW	$V_{OUT} = 0.1V \text{ rms}$	1MHz	•	•	•	•
1% Amplitude Error	$C_{LOAD} = 1000pF$	50kHz	•	•	•	•
Slew Rate	$V_{OUT} = 20V \text{ pk-pk}$	20V/ μs	•	•	•	•
Settling Time to $\pm 1\%$	$\Delta V_{OUT} = 20V$	2 μs	•	•	•	•
NOISE						
Noise Spectral-Density	SF = 10	$0.8\mu V/\sqrt{Hz}$	•	•	•	•
	SF = 3 (Note 4)	$0.4\mu V/\sqrt{Hz}$	•	•	•	•
Wideband Noise	f = 10Hz to 5MHz	1mV rms	•	•	•	•
	f = 10Hz to 10kHz	90 μV rms	•	•	•	•
	f = 10Hz to 10kHz	•	•	•	•	•
	SF = 3 (Note 4)	60 μV rms	•	•	•	•
OUTPUT						
Output Voltage Swing	$T_A = \text{min to max}$	$\pm 11V \text{ min}$	•	•	•	•
Output Impedance	Unity-Gain, f $\leq$ 1kHz	0.1 Ω	•	•	•	•
Maximum Output Current	$R_L = 0, T_A = \text{min to max}$	30mA	•	•	•	•
Amplifier Open-Loop Gain	f = 50Hz	70dB	•	•	•	•
INPUT AMPLIFIERS (X, Y and Z)⁵						
Signal Voltage Range	Rated Accuracy (Diff. or CM)	$\pm 10V$	•	•	•	•
	Operating (Diff.)	$\pm 12V$	•	•	•	•
Offset Voltage, X, Y		$\pm 5mV (\pm 20mV \text{ max})$	$\pm 2mV (\pm 10mV \text{ max})$	•	•	•
Drift	$T_A = \text{min to max}$	$100\mu V/^{\circ}\text{C}$	$50\mu V/^{\circ}\text{C}$	•	•	$150\mu V/^{\circ}\text{C}$
Offset Voltage, Z		$\pm 5mV (\pm 30mV \text{ max})$	$\pm 2mV (\pm 15mV \text{ max})$	$\pm 2mV (\pm 10mV \text{ max})$	•	•
Drift	$T_A = \text{min to max}$	$200\mu V/^{\circ}\text{C}$	$100\mu V/^{\circ}\text{C}$	•	$500\mu V/^{\circ}\text{C max}$	$300\mu V/^{\circ}\text{C max}$
CMRR (X, Y, Z)	50Hz, 20V pk-pk	80dB (60dB min)	90dB (70dB min)	•	•	•
Bias Current	Diff. Input = 0	0.8 μA (2 μA max)	•	•	•	•
Offset Current	Diff. Input = 0	0.1 μA	•	0.05 μA (0.2 μA max)	•	•
Differential Resistance		10M Ω	•	•	•	•
DIVIDER PERFORMANCE⁶						
Transfer Function	$X_1 > X_2$	$10 \frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$	•	•	•	•
Total Error ¹	X = 10V -10V $\leq Z \leq$ +10V X = 1V -1V $\leq Z \leq$ +1V 0.1V $\leq X \leq$ 10V -10V $\leq Z \leq$ +10V (Note 7)	$\pm 0.75\%$ $\pm 2.0\%$ $\pm 2.5\%$	$\pm 0.35\%$ $\pm 1.0\%$ $\pm 1.0\%$	$\pm 0.2\%$ $\pm 0.8\%$ $\pm 0.8\%$	• • •	• • •
SQUARER PERFORMANCE						
Transfer Function		$\frac{(X_1 - X_2)^2}{10} + Z_2$	•	•	•	•
Total Error ¹	-10V $\leq X \leq$ +10V	$\pm 0.6\%$	$\pm 0.3\%$	$\pm 0.2\%$	•	•
SQUARE-ROOTER PERFORMANCE⁶						
Transfer Function	$Z_1 \leq Z_2$	$\sqrt{10(Z_2 - Z_1)} + X_2$	•	•	•	•
Total Error ¹	1V $\leq Z \leq$ 10V	$\pm 1.0\%$	$\pm 0.5\%$	$\pm 0.25\%$	•	•
POWER SUPPLY SPECIFICATIONS						
Supply Voltage	Rated Performance	$\pm 15V$	•	•	•	•
	Operating	$\pm 8V \text{ to } \pm 18V$	•	•	$\pm 8V \text{ to } \pm 22V$	$\pm 8V \text{ to } \pm 22V$
Supply Current	Quiescent	4mA (6mA max)	•	•	•	•

NOTES

¹Specifications same as AD534J.

²Specifications same as AD534K.

³Figures given are percent of full-scale, $\pm 10V$ (i.e., 0.01% = 1mV).

⁴May be reduced down to 3V using external resistor between $-V_S$ and SF.

⁵Irreducible component due to nonlinearity; excludes effect of offsets.

⁶Using external resistor adjusted to give SF = 3.

⁷See Functional Block Diagram, Figure 1, for definition of sections.

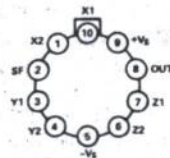
⁸The AD535 is a functional equivalent to the AD534, has guaranteed performance in the divider and square rooter modes and is recommended for such applications.

⁹With external Z-offset adjustment, $Z \leq +X$.

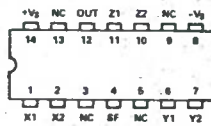
Specifications subject to change without notice.

PIN CONFIGURATION & DIMENSIONS

Dimensions shown in inches and (mm).

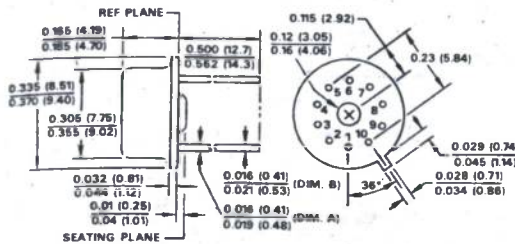


**H-PACKAGE
TO-100
(TOP VIEW)**

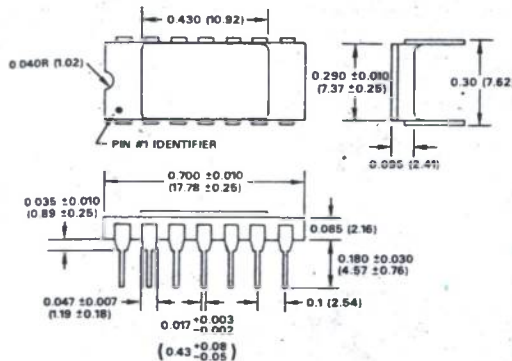


**D-PACKAGE
TO-116
(TOP VIEW)**

TO-100

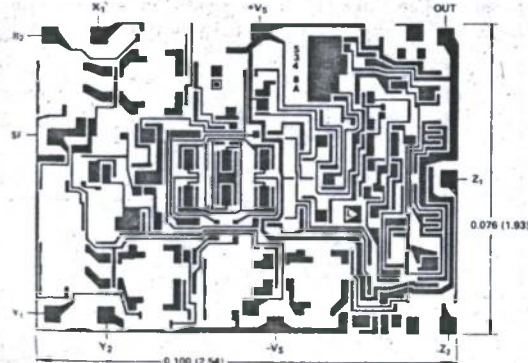


TO-116



CHIP DIMENSIONS & PAD LAYOUT

Dimensions shown in inches and (mm).



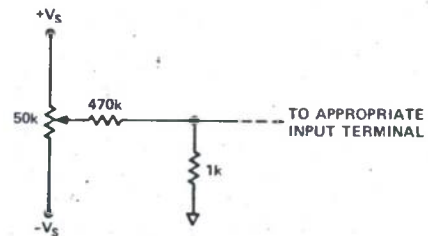
THE AD534 IS AVAILABLE IN LASER TRIMMED CHIP FORM. CONSULT THE CHIP CATALOG FOR DETAILS.

ABSOLUTE MAXIMUM RATINGS

	AD534J, K, L	AD534S, T
Supply Voltage	±18V	±22V
Internal Power Dissipation	500mW	•
Output Short-Circuit to Ground	Indefinite	•
Input Voltages, X ₁ X ₂ Y ₁ Y ₂ Z ₁ Z ₂	±V _S	•
Rated Operating Temperature Range	0 to +70°C	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C	•
Lead Temperature, 60s soldering	+300°C	•

*Same as AD534J specs.

OPTIONAL TRIMMING CONFIGURATION



FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the AD534. Inputs are converted to differential currents by three identical voltage-to-current converters, each trimmed for zero offset. The product of the X and Y currents is generated by a multiplier cell using Gilbert's translinear technique. An on-chip "Buried Zener" provides a highly stable reference, which is laser trimmed to provide an overall scale factor of 10.000V. The difference between XY/SF and Z is then applied to the high gain output amplifier. This permits various closed loop configurations and dramatically reduces nonlinearities due to the input amplifiers, a dominant source of distortion in earlier designs. The effectiveness of the new scheme can be judged from the fact that under typical conditions as a multiplier the nonlinearity on the Y input, with X at full scale (±10V), is ±0.005% of F.S.; even at its worst point, which occurs when X = ±6.4V, it is typically only ±0.025% of F.S. Nonlinearity for signals applied to the X input, on the other hand, is determined almost entirely by the multiplier element and is parabolic in form. This error is a major factor in determining the overall accuracy of the unit and hence is closely related to the device grade.

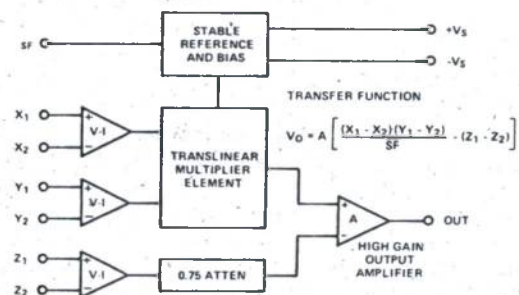


Figure 1. AD534 Functional Block Diagram

The generalized transfer function for the AD534 is given by:

$$V_{OUT} = A \frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)$$

where A = open loop gain of output amplifier, typically 70dB at dc

X, Y, Z = input voltages (full scale = $\pm SF$, peak = $\pm 1.25SF$)

SF = scale factor, pretrimmed to 10.00 but adjustable by the user down to 3.

In most cases the open loop gain can be regarded as infinite, and SF will be 10. The operation performed by the AD534, can then be described in terms of equation:

$$(X_1 - X_2)(Y_1 - Y_2) = 10(Z_1 - Z_2)$$

The user may adjust SF for values between 10.00 and 3 by connecting an external resistor in series with a potentiometer between SF and $-V_S$. The approximate value of the total resistance for a given value of SF is given by the relationship:

$$R_{SF} = 5.4K \frac{SF}{10 - SF}$$

Due to device tolerances, allowance should be made to vary R_{SF} by $\pm 25\%$ using the potentiometer. Considerable reduction in bias currents, noise and drift can be achieved by decreasing SF . This has the overall effect of increasing signal gain without the customary increase in noise. Note that the peak input signal is always limited to $1.25SF$ (i.e., $\pm 5V$ for $SF = 4$) so the overall transfer function will show a maximum gain of 1.25. The performance with small input signals, however, is improved by using a lower SF since the dynamic range of the inputs is now fully utilized. Bandwidth is unaffected by the use of this option.

Supply voltages of $\pm 15V$ are generally assumed. However, satisfactory operation is possible down to $\pm 8V$ (see curve 1). Since all inputs maintain a constant peak input capability of $\pm 1.25SF$ some feedback attenuation will be necessary to achieve output voltage swings in excess of $\pm 12V$ when using higher supply voltages.

OPERATION AS A MULTIPLIER

Figure 2 shows the basic connection for multiplication. Note that the circuit will meet all specifications without trimming.

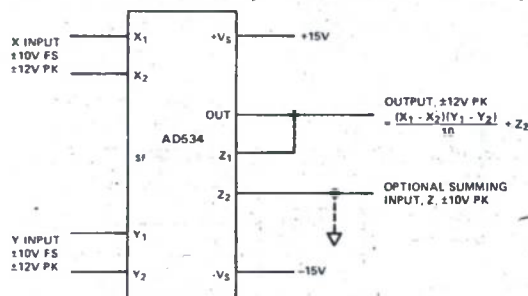


Figure 2. Basic Multiplier Connection

In some cases the user may wish to reduce ac feedthrough to a minimum (as in a suppressed carrier modulator) by applying an external trim voltage ($\pm 30mV$ range required) to the X or Y input (see Optional Trimming Configuration, previous page). Curve 4 shows the typical ac feedthrough with this adjustment mode. Note that the Y input is a factor of 10 lower than the X input and should be used in applications where null suppression is critical.

4-20 MULTIPLIERS & DIVIDERS

The high impedance Z_2 terminal of the AD534 may be used to sum an additional signal into the output. In this mode the output amplifier behaves as a voltage follower with a 1MHz small signal bandwidth and a 20V/ μs slew rate. This terminal should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise the differential inputs should be referenced to their respective ground potentials to realize the full accuracy of the AD534.

A much lower scaling voltage can be achieved without any reduction of input signal range using a feedback attenuator as shown in Figure 3. In this example, the scale is such that $V_{OUT} = XY$, so that the circuit can exhibit a maximum gain of 10. This connection results in a reduction of bandwidth to about 80kHz without the peaking capacitor $C_F = 200pF$. In addition, the output offset voltage is increased by a factor of 10 making external adjustments necessary in some applications. Adjustment is made by connecting a $4.7M\Omega$ resistor between Z_1 and the slider of a pot connected across the supplies to provide $\pm 300mV$ of trim range at the output.

Feedback attenuation also retains the capability for adding a signal to the output. Signals may be applied to the high imped-

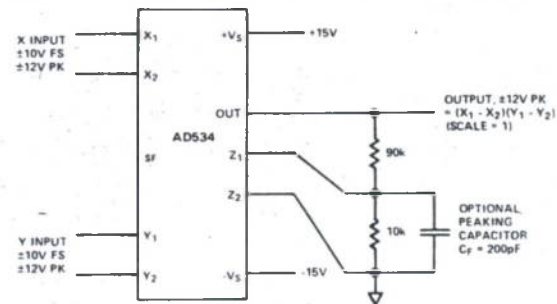


Figure 3. Connections for Scale-Factor of Unity

ance Z_2 terminal where they are amplified by $+10$ or to the common ground connection where they are amplified by $+1$. Input signals may also be applied to the lower end of the $10k\Omega$ resistor, giving a gain of -9 . Other values of feedback ratio, up to $X100$, can be used to combine multiplication with gain.

Occasionally it may be desirable to convert the output to a current, into a load of unspecified impedance or dc level. For example, the function of multiplication is sometimes followed by integration; if the output is in the form of a current, a simple capacitor will provide the integration function. Figure 4 shows how this can be achieved. This method can also be applied in squaring, dividing and square rooting modes by appropriate choice of terminals. This technique is used in the voltage-controlled low-pass filter and the differential-input voltage-to-frequency converter shown in the Applications Section.

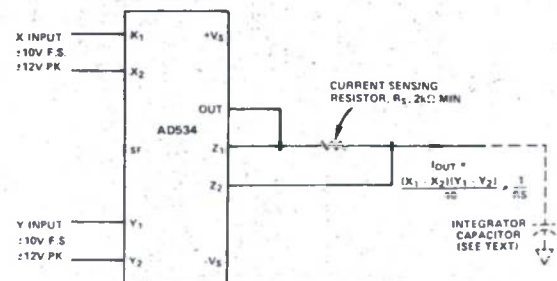


Figure 4. Conversion of Output to Current

OPERATION AS A SQUARER

Operation as a squarer is achieved in the same fashion as the multiplier except that the X and Y inputs are used in parallel. The differential inputs can be used to determine the output polarity (positive for $X_1 = Y_1$ and $X_2 = Y_2$, negative if either one of the inputs is reversed). Accuracy in the squaring mode is typically a factor of 2 better than in the multiplying mode, the largest errors occurring with small values of output for input below 1V.

If the application depends on accurate operation for inputs that are always less than $\pm 3V$, the use of a reduced value of SF is recommended as described in the FUNCTIONAL DESCRIPTION section (previous page). Alternatively, a feedback attenuator may be used to raise the output level. This is put to use in the difference-of-squares application to compensate for the factor of 2 loss involved in generating the sum term (see Figure 7).

The difference-of-squares function is also used as the basis for a novel rms-to-dc converter shown in Figure 14. The averaging filter is a true integrator, and the loop seeks to zero its input. For this to occur, $(V_{IN})^2 - (V_{OUT})^2 = 0$ (for signals whose period is well below the averaging time-constant). Hence V_{OUT} is forced to equal the rms value of V_{IN} . The absolute accuracy of this technique is very high; at medium frequencies, and for signals near full scale, it is determined almost entirely by the ratio of the resistors in the inverting amplifier. The multiplier scaling voltage affects only open loop gain. The data shown is typical of performance that can be achieved with an AD534K, but even using an AD534J, this technique can readily provide better than 1% accuracy over a wide frequency range, even for crest-factors in excess of 10.

OPERATION AS A DIVIDER

The AD535, a pin for pin functional equivalent to the AD534, has guaranteed performance in the divider and square-rooter configurations and is recommended for such applications.

Figure 5 shows the connection required for division. Unlike earlier products, the AD534 provides differential operation on both numerator and denominator, allowing the ratio of two floating variables to be generated. Further flexibility results from access to a high impedance summing input to Y_1 . As with all dividers based on the use of a multiplier in a feedback loop, the bandwidth is proportional to the denominator magnitude, as shown in curve 8.

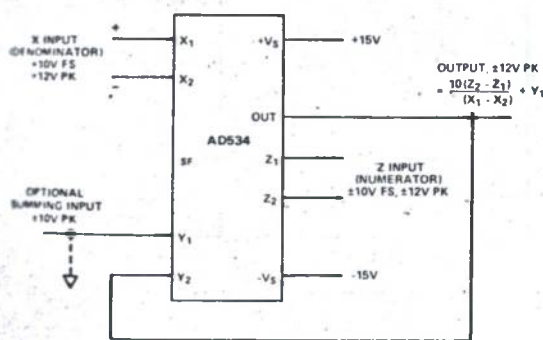


Figure 5. Basic Divider Connection

Without additional trimming, the accuracy of the AD534K and L is sufficient to maintain a 1% error over a 10V to 1V denominator range. This range may be extended to 100:1 by simply reducing the X offset with an externally generated trim voltage (range required is $\pm 3.5mV$ max) applied to the unused X input (see Optional Trimming Configuration, page 4-19). To trim, apply a ramp of +100mV to +V at 100Hz to both X_1 and Z_1 (if X_2 is used for offset adjustment, otherwise reverse the signal polarity) and adjust the trim voltage to minimize the variation in the output.*

Since the output will be near +10V, it should be ac-coupled for this adjustment. The increase in noise level and reduction in bandwidth preclude operation much beyond a ratio of 100 to 1.

As with the multiplier connection, overall gain can be introduced by inserting a simple attenuator between the output and Y_2 terminal. This option, and the differential-ratio capability of the AD534 are utilized in the percentage-computer application shown in Figure 11. This configuration generates an output proportional to the percentage deviation of one variable (A) with respect to a reference variable (B), with a scale of one volt per percent.

OPERATION AS A SQUARE ROOTER

The operation of the AD534 in the square root mode is shown in Figure 6. The diode prevents a latching condition which could occur if the input momentarily changes polarity. As shown, the output is always positive; it may be changed to a negative output by reversing the diode direction and interchanging the X inputs. Since the signal input is differential, all combinations of input and output polarities can be realized, but operation is restricted to the one quadrant associated with each combination of inputs.

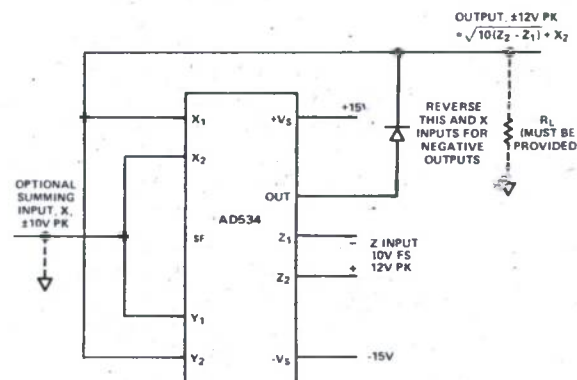


Figure 6. Square-Rooter Connection

In contrast to earlier devices, which were intolerant of capacitive loads in the square root modes, the AD534 is stable with all loads up to at least 1000pF. For critical applications, a small adjustment to the Z input offset (see Optional Trimming Configuration, page 4-19) will improve accuracy for inputs below 1V.

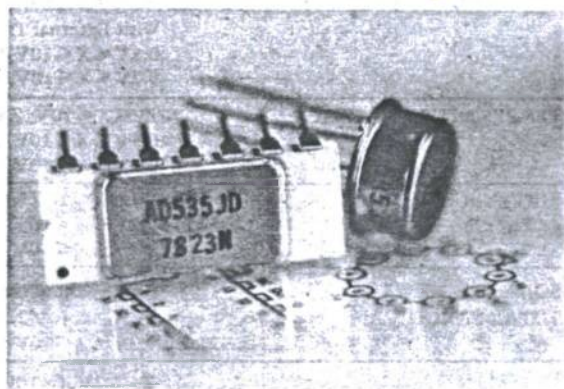
*See the AD535 Data Sheet for more details.

FEATURES

Pretrimmed to $\pm 0.5\%$ max Error, 10:1 Denominator Range (AD535K)
 $\pm 2.0\%$ max Error, 50:1 Denominator Range (AD535J)
 All Inputs (X, Y and Z) Differential
 Low Cost, Monolithic Construction

APPLICATIONS

General Analog Signal Processing
 Differential Ratio and Percentage Computations
 Precision AGC Loops
 Square-Rooting



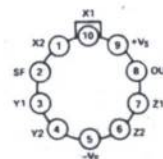
PRODUCT DESCRIPTION

The AD535 is a monolithic laser-trimmed two-quadrant divider having performance specifications previously found only in expensive hybrid or modular products. A maximum divider error of $\pm 0.5\%$ is guaranteed for the AD535K without any external trimming over a denominator range of 10:1; $\pm 2.0\%$ max error over a range of 50:1. A maximum error of $\pm 1\%$ over the 50:1 denominator range is guaranteed with the addition of two external trims. The AD535 is the first divider to offer fully differential, high impedance operation on all inputs, including the z -input, a feature which greatly increases its flexibility and ease of use. The scale factor is pretrimmed to the standard value of 10.00; by means of an external resistor, this can be reduced by any amount down to 3.

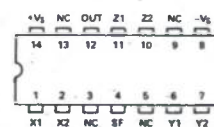
The extraordinary versatility and performance of the AD535 recommend it as the first choice in many divider and computational applications. Typical uses include square-rooting, ratio computation, "pin-cushion" correction and AGC loops. The device is packaged in a hermetically sealed, 10-pin TO-100 can or 14-pin TO-116 DIP and made available in a $\pm 1\%$ max error version (J) and a $\pm 0.5\%$ max error version (K). Both versions are specified for operation over the 0 to $+70^\circ\text{C}$ temperature range.

PRODUCT HIGHLIGHTS

1. Laser trimming at the wafer stage enables the AD535 to provide high accuracies without the addition of external trims ($\pm 0.5\%$ max error over a 10:1 denominator range for the AD535K).
2. Improved accuracies over a wider denominator range are possible with only two external trims ($\pm 0.5\%$ max error over a 20:1 denominator range for the AD535K).
3. Differential inputs on the X, Y and Z input terminals enhance the AD535's versatility as a generalized analog computational circuit.
4. Monolithic construction permits low cost and, at the same time, increased reliability.



**TO-100
(TOP VIEW)**



**TO-116
(TOP VIEW)**

SPECIFICATIONS (V_S = ±15V, R_L ≥ 2kΩ, T_A = +25°C unless otherwise stated)

PARAMETER	CONDITIONS	AD535J	AD535K
TRANSFER FUNCTION	Figure 2	$10 \frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$	*
TOTAL ERROR ¹	No External Trims, Figure 2		
	1V ≤ X ≤ 10V, Z ≤ X	1.0% max	0.5% max
	0.2V ≤ X ≤ 10V, Z ≤ X	5.0% max	2.0% max
	With External Trims, Figure 5		
	0.5V ≤ X ≤ 10V, Z ≤ X	1.0% max	0.5% max
	0.2V ≤ X ≤ 10V, Z ≤ X	2.0% max	1.0% max
TEMPERATURE COEFFICIENT	1V ≤ X ≤ 10V, Z ≤ X	0.01%/°C typ	*
	0.5V ≤ X ≤ 10V, Z ≤ X	0.02%/°C typ	*
	0.2V ≤ X ≤ 10V, Z ≤ X	0.05%/°C typ	*
SUPPLY RELATED Error V _S = ±14V to ±16V	1V ≤ X ≤ 10V	0.1%/V typ	*
	0.5V ≤ X ≤ 10V	0.2%/V typ	*
	0.2V ≤ X ≤ 10V	0.5%/V typ	*
SQUARE ROOTER	No External Trims, Figure 11		
TOTAL ERROR ¹	1V ≤ Z ≤ 10V	0.4% typ	*
	0.2V ≤ Z ≤ 10V	0.7% typ	*
NOISE ²	X = 0.2V, f = 10Hz to 10kHz	4.5mV rms typ	*
BANDWIDTH	X = 0.2V	20kHz typ	*
INPUT AMPLIFIERS ³			
CMRR	f = 50Hz, 20V p-p	60dB min	*
Bias Current		2.0μA max	*
Offset Current		0.1μA typ	*
Differential Resistance		10MΩ typ	*
OUTPUT AMPLIFIER ³			
Open-Loop Gain	f = 50Hz	70dB typ	*
Small Signal Gain-Bandwidth	V _{OUT} = 0.1V rms	1MHz typ	*
1% Amplitude Error	C _{LOAD} = 1000pF	50kHz typ	*
Output Voltage Swing	T _{min} to T _{max}	±11V min	*
Slew Rate	V _{OUT} = 20V p-p	20V/μs typ	*
Settling Time	V _{OUT} = 20V ±1%	2μs typ	*
Output Impedance	Unity Gain, f ≤ 1kHz	0.1Ω typ	*
Wide-band Noise	f = 10Hz to 5MHz	1mV rms typ	*
	f = 10Hz to 10kHz	90μV rms typ	*
OUTPUT CURRENT	T _{min} to T _{max} , R _L = 0	30mA max	*
POWER SUPPLIES			
Rated Performance		±15V	*
Operating		±8V min, ±18V max	*
Supply Current	Quiescent	6mA max	*

NOTES:

*Specifications same as AD535J.

¹Figures are given as a percent of full scale (i.e. 1.0% = 100mV).

²Noise may be reduced as shown in Figure 14.

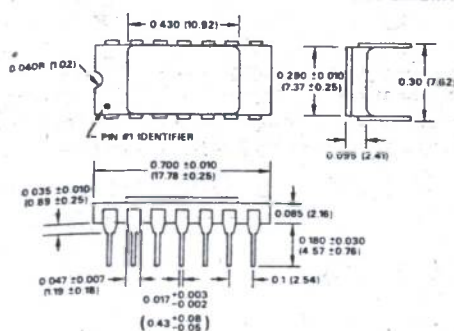
³See Figure 1 for definition of section.

Specifications subject to change without notice.

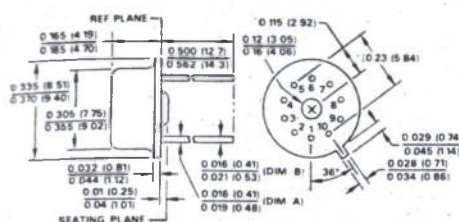
PHYSICAL DIMENSIONS

Dimensions shown in inches and (mm).

TO-116



TO-100



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation	500mW
Output Short-Circuit to Ground	Indefinite
Input Voltages, X_1 , X_2 , Y_1 , Y_2 , Z_1 , Z_2	±V _S
Rated Operating Temp Range	0 to +70°C
Storage Temp Range	-65°C to +150°C
Lead Temp, 60s soldering	+300°C

FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the AD535. Inputs are converted to differential currents by three identical voltage to current converters, each trimmed for zero offset. The product of the X and Y currents is generated by a multiplier cell using Gilbert's translinear technique with an internal scaling voltage.

The difference between XY/SF and Z is applied to the high gain output amplifier. The transfer function can then be expressed...

$$V_{OUT} = A \left[\frac{(X_1 - X_2)(Y_1 - V_{OUT})}{SF} - (Z_1 - Z_2) \right]$$

where A = open loop gain of output amplifier, typically 70dB at dc

X, Y, Z = input voltages

SF = scale factor, pretrimmed to 10.00V but adjustable by the user down to 3V.

In most cases the open loop gain can be regarded as infinite and SF will be 10V. Dividing both sides of the equation by A and solving the V_{OUT} , we get...

$$V_{OUT} = 10V \frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$$

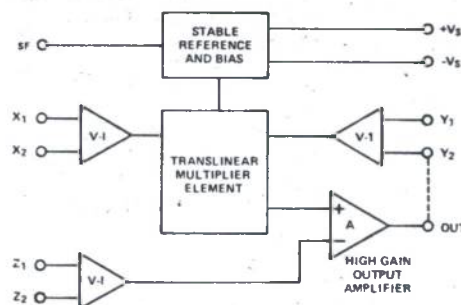


Figure 1. AD535 Functional Block Diagram

SOURCES OF ERROR

Divider error is specified as a percent of full scale (i.e. 10.00V) and consists primarily of the effects of X, Y and Z offsets and scale factor (which are trimmable) as shown in the generalized equation....

$$V_{OUT} = (SF + \Delta SF) \left[\frac{(Z_2 - Z_1) + Z_{OS}}{(X_1 - X_2) + X_{OS}} \right] + Y_1 + Y_{OS}$$

Note especially that divider error is inversely proportional to X, that is, the error increases rapidly with decreasing denominator values. Hence, the AD535 divider error is specified over several denominator ranges on previous page. (See also Figure 12, AD535 Total Error as a function of denominator values.)

Overall accuracy of the AD535 can be significantly improved by nulling out X and Z offset as described in the applications sections. Figure 13 illustrates a factor of 2 improvement in accuracy with the addition of these external trims. The remaining errors stem primarily from scale factor error and Y offsets which can be trimmed out as shown in Figure 6.

Figure 14 illustrates the bandwidth and noise relationships versus denominator voltage. Whereas noise increases with decreasing denominator, bandwidth decreases, the net result given by the expression...

$$E_{NOUT} (\text{wideband}) = \frac{1.26}{\sqrt{\left(\frac{X}{10}\right)}} \text{ mV rms}$$

External filtering can be added to limit output voltage noise even further. In this case...

$$E_{NOUT} \text{ (B.W. externally limited)} = \frac{0.9 \sqrt{f}}{\left(\frac{X}{10}\right)} \text{ mV rms}$$

where f = bandwidth in MHz of an external filter whose bandwidth is less than the noise bandwidth of the AD535. Table 1 provides calculated values of the typical output voltage noise, both filtered and unfiltered for several denominator values.

X	Noise 10Hz to 5MHz	Noise Limited by External Filtering 10Hz to 10kHz
0.2V	8.9mV rms	4.5mV rms
0.5V	5.6mV rms	1.8mV rms
1V	4.0mV rms	0.9mV rms
10V	1.3mV rms	0.09mV rms

Table 1. AD535 Calculated Voltage Noise

APPLICATIONS

Figure 2 shows the standard divider connection without external trims. The denominator X , is restricted to positive values in this configuration. X , Y and Z inputs are differential with high (80dB typical) CMRR permitting the application of differential signals on X and Z (see Figure 3).

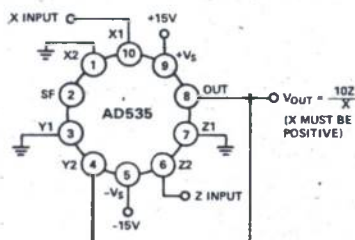


Figure 2. Divider Without External Trims

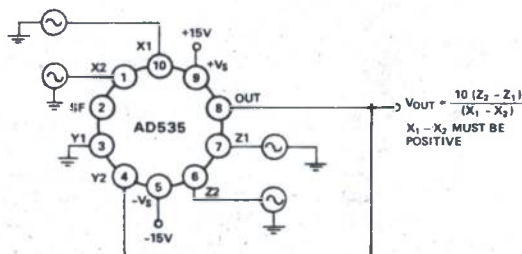


Figure 3. Differential Divider Connection

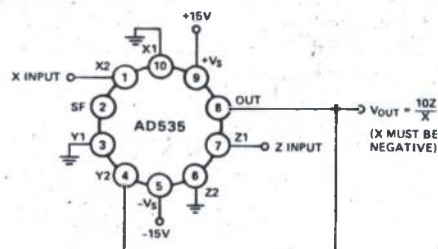


Figure 4. Divider Connection for Negative X Inputs

Negative denominator inputs are handled as shown in Figure 4. Note that in either configuration, operation is limited to two quadrants (i.e. Z is bipolar, X is unipolar).

A factor of two improvements in accuracy is possible by trimming the X and Z offsets as illustrated in Figure 5. To trim, set X to the smallest denominator value for which accurate computation is required (i.e., $X = 0.2V$). With $Z = 0$, adjust the X_0 trim for $V_{OUT} = 0$. Next, adjust the X_0 trim for the best compromise when $Z = +X$ ($V_{OUT} = +10V$) and $Z = -X$ ($V_{OUT} = -10V$). Finally, readjust Z_0 for the best compromise at $Z = +X$, $Z = -X$ and $Z = 0$. The remaining error (Figure 13) consists primarily of scale factor error, output offset and an irreducible nonlinearity component.

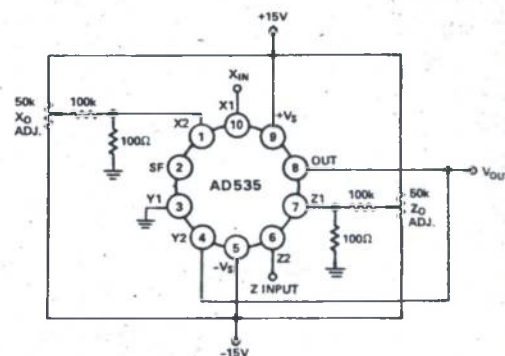


Figure 5. Precision Divider Using Two Trims

In certain applications, the user may elect to adjust SF for values between 10.00 and 3 by connecting an external resistor in series with a potentiometer between SF and $-V_S$. The approximate value of the total resistance for a given value of SF is given by the relationship:

$$R_{SF} = 5.4K \frac{SF}{10 - SF}$$

Due to device tolerances, allowance should be made to vary $R_{SF} \pm 25\%$ using the potentiometer. Note that the peak signal is always limited to 1.25 SF (i.e. $\pm 5V$ for $SF = 4$).

The scale factor may also be adjusted using a feedback attenuator between V_{OUT} and Y_2 as indicated in Figure 6. The input signal range is unaffected using this scheme.

Scale factor and output offset error can be minimized utilizing the four trim circuit of Figure 6. Adjustment is as follows:

1. Apply $X = +0.2V$ (or the smallest required denominator value), $Z = 0$ and adjust Z_0 for $V_{OUT} = 0$.
2. Apply $X = 0.2V$. Then adjust the X_0 trim for the best compromise when $Z = +X$ ($V_{OUT} = +10V$) and $Z = -X$ ($V_{OUT} = -10V$).
3. Apply $X = +10V$, $Z = 0$ and adjust Y_0 for $V_{OUT} = 0$.
4. Apply $X = +10V$. Then adjust the scale factor (SF) trim for the best compromise when $Z = +X$ ($V_{OUT} = +10V$) and $Z = -X$ ($V_{OUT} = -10V$).
5. Repeat steps 1 and 2.
6. Apply $X = 0.2V$. Then adjust the Z trim for the best compromise when $Z = X$ ($V_{OUT} = +10V$), $Z = 0$ ($V_{OUT} = 0$) and $Z = -X$ ($V_{OUT} = -10V$).

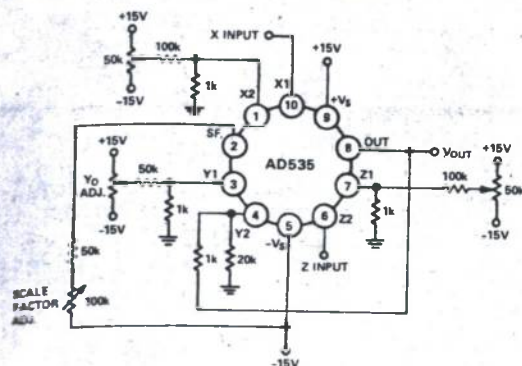


Figure 6. Precision Divider with Four External Adjustments

These trim adjustments can be made either by using two calibrated voltage sources and a DVM, or by using a differential scope, a low frequency generator, a voltage source and a precision attenuator. As shown in Figure 7, the differential scope subtracts the expected ideal output and thus displays only errors. Set the attenuation to $\frac{X}{10}$.

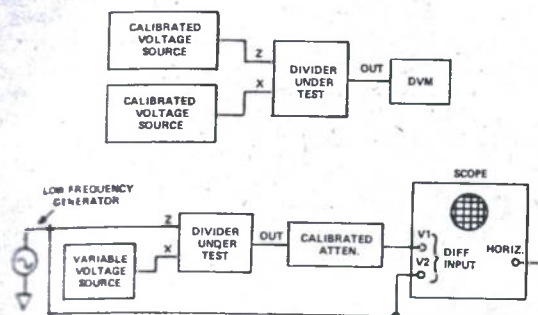


Figure 7. Alternate Trim Adjustment Set-Up

PIN-CUSHION CORRECTION

A pin-cushion corrector eliminates the distortion caused by flat screen CRT tubes. The correction equations are:

$$V_{OH} = \frac{V_{IH}}{\sqrt{V_{IH}^2 + V_{IV}^2 + L^2}}$$

$$\text{and } V_{OV} = \frac{V_{IV}}{\sqrt{V_{IH}^2 + V_{IV}^2 + L^2}}$$

where V_{OH} and V_{OV} are the horizontal and vertical output signals, respectively.

V_{IH} and V_{IV} are the horizontal and vertical input signals, respectively.

L is the length of the CRT tube.

In typical applications L (expressed in voltage) is roughly equal to full scale V_{IH} or V_{IV} . The result is that the expression, $\sqrt{(V_{IH}^2 + V_{IV}^2 + L^2)}$, varies less than 2:1 over the full range of values of V_{IH} and V_{IV} .

Major sources of divider error associated with small denominator values can thereby be minimized.

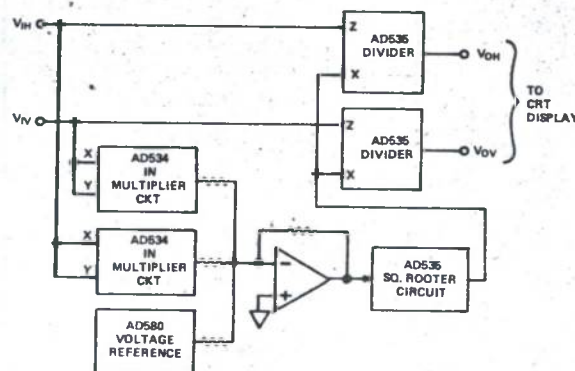


Figure 8. Pin-Cushion Corrector

Figure 9 shows an AGC loop using an AD535 divider. The AD535 lends itself naturally in this application since it is configured to provide gain rather than loss. Overall gain varies from 1 to ∞ as the denominator is servoed to maintain V_{OUT} at a constant level.

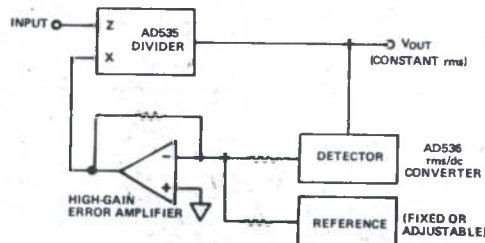


Figure 9. AGC Loop Using the AD536 rms/dc Converter as a Detector

Figure 10 shows a method for obtaining the time average as defined by:

$$\bar{X} = \frac{1}{T} \int_0^T X dt$$

where T is the time interval over which the average is to be taken. Conventional techniques typically provide only a crude approximation to the true time average, and furthermore, require a fixed time interval before the average can be taken. In Figure 10, the AD535 is used to divide the integrator output by the ramp generator output. Since the ramp is proportional to time, the integrator is divided by the time interval, thus allowing continuous, true time processing of signals over intervals varying by as much as 50:1.

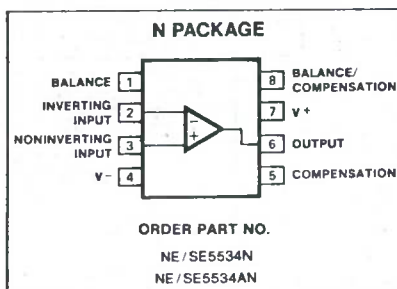
DESCRIPTION

The 5533/5534 are single and dual high-performance low noise operational amplifiers. Compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

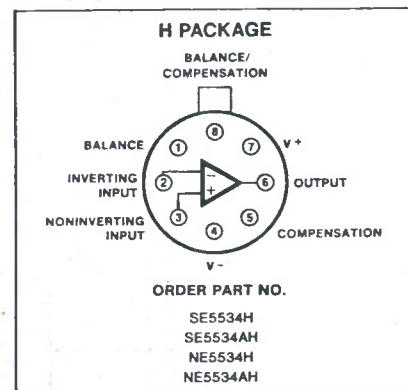
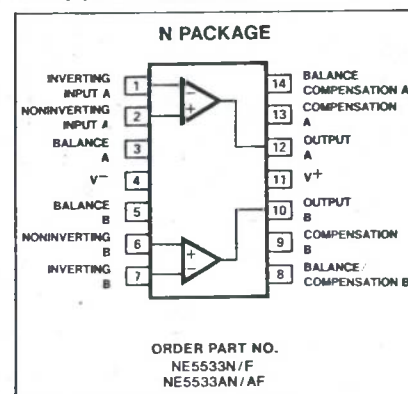
This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew-rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5533A/5534A version be used which has guaranteed noise specifications.

FEATURES

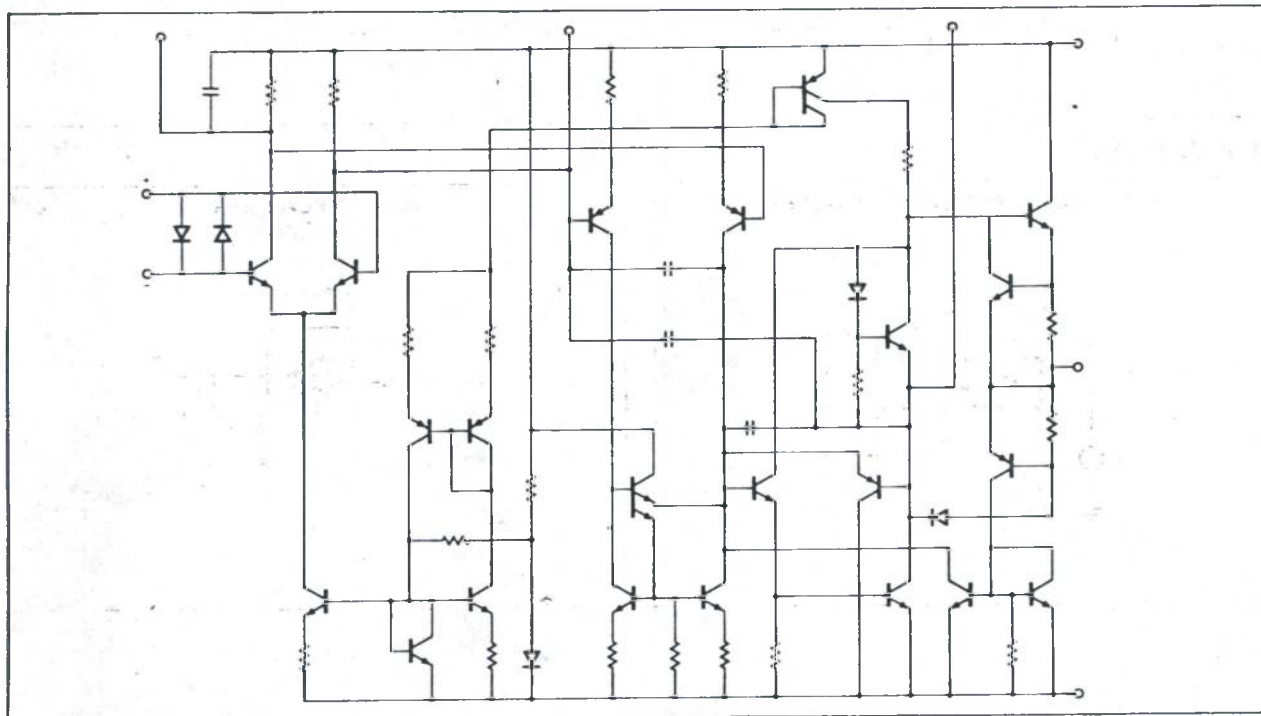
- Small-signal bandwidth: 10MHz
 - Output drive capability: 600Ω, 10V (rms) at $V_s = \pm 18V$
 - Input noise voltage: 4nV/√Hz
 - DC voltage gain: 100000
 - AC voltage gain: 6000 at 10kHz
 - Power bandwidth: 200kHz
 - Slew-rate: 13V/μs
 - Large supply voltage range: ± 3 to $\pm 20V$
- 5534
- Pin out 741
 - Configuration Single



PIN CONFIGURATION



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _S Supply voltage	±22	V
V _{IN} Input voltage	±V supply	V
V _{DIFF} Differential input voltage ¹	±5	V
T _A Operating temperature range		
SE 5534/5534A	-55 to +125	°C
NE5533/5533A/5534/5534A	0 to 70	°C
T _{STG} Storage temperature	-65 to +150	°C
T _J Junction temperature	150	°C
P _D Power dissipation at 25°C ²		
5533N 5534N	500	mW
5534T	800	mW
Output short circuit duration ³	indefinite	
Lead temperature (soldering 10 sec)	300	°C

NOTES

- Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
- For operation at elevated temperature T package must be derated based on a thermal resistance of 150°C/W junction to ambient, 45°C/W junction to case. Thermal resistance of the N package is 240°C/W junction to ambient.
- Output may be shorted to ground at V_S = ±15V, T_A = 25°C. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_S = ±15V unless otherwise specified.^{1,2}

PARAMETER	TEST CONDITIONS	SE5534/5534A			NE5533/5533A 5534/5534A			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{OS} Offset voltage	Over temperature		.5	2 3		.5	4 5	mV mV
I _{OS} Offset current	Over temperature		10	200 500		20	300 400	nA nA
I _B Input current	Over temperature		400	800 1500		500	1500 2000	nA nA
I _{CC} Supply current Per op amp	Over temperature		4	6.5 9		4	8	mA mA
V _{CM} Common mode input range		±12	±13		±12	±13		V
CMRR Common mode rejection ratio		80	100		70	100		dB
PSRR Power supply rejection ratio			10	50		10	100	μV/V
A _{VOL} Large signal voltage gain	R _L ≥ 600Ω, V _O = ±10V Over temperature	50 25	100		25 15	100		V/mV V/mV
V _{OUT} Output swing	R _L ≥ 600Ω R _L ≥ 600Ω V _S = ±18V	±12 ±15	±13 ±16		±12 ±15	±13 ±16		V V
R _{IN} Input resistance		50	100		30	100		kΩ
I _{SC} Output short circuit current			38			38		mA

NOTES

- For NE5533/5533A/5534/5534A, T_{MIN} = 0°C, T_{MAX} = 70°C
- For SE 5534/5534A, T_{MIN} = -55°C, T_{MAX} = +125°C

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE5534/5534A			NE5533/5533A 5534/5534A			UNIT
		Min	Typ	Max	Min	Typ	Max	
R_{OUT} Output resistance	$A_V = 30\text{dB}$ closed loop $f = 10\text{kHz}$, $R_L = 600\Omega$, $C_C = 22\text{pF}$		0.3			0.3		Ω
Transient response	Voltage follower, $V_{IN} = 50\text{mV}$ $R_L = 600\Omega$, $C_C = 22\text{pF}$, $C_L = 100\text{pF}$							
T_R Rise time			20			20		ns
Overshoot			20			20		%
Transient response	$V_{IN} = 50\text{mV}$, $R_L = 600\Omega$ $C_C = 47\text{pF}$, $C_L = 500\text{pF}$							
T_R Rise time			50			50		ns
Overshoot			35			35		%
AC Gain	$f = 10\text{kHz}$, $C_C = 0$ $f = 10\text{kHz}$, $C_C = 22\text{pF}$		6 2.2			6 2.2		V/mV V/mV
Gain bandwidth product	$C_C = 22\text{pF}$, $C_L = 100\text{pF}$		10			10		mHz
Slew rate	$C_C = 0$ $C_C = 22\text{pF}$		13 6			13 6		V/ μS V/ μS
Power bandwidth	$V_{OUT} = \pm 10\text{V}$, $C_C = 0$ $V_{OUT} = \pm 10\text{V}$, $C_C = 22\text{pF}$ $V_{OUT} = \pm 14\text{V}$, $R_L = 600\Omega$ $C_C = 22\text{pF}$, $V_{CC} = \pm 18\text{V}$		200 95 70			200 95 70		kHz kHz kHz

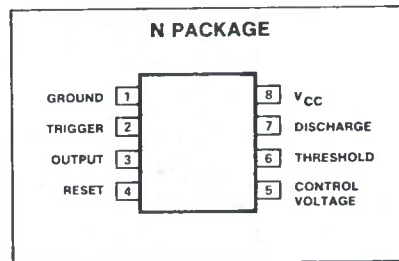
ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	5533/5534			5533A/5534A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input noise voltage	$f_o = 30\text{Hz}$ $f_o = 1\text{kHz}$		7 4			5.5 3.5	7 4.5	nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$
Input noise current	$f_o = 30\text{Hz}$ $f_o = 1\text{kHz}$		2.5 0.6			1.5 0.4		pA/ $\sqrt{\text{Hz}}$ pA/ $\sqrt{\text{Hz}}$
Broadband noise figure	$f = 10\text{Hz} - 20\text{kHz}$, $R_S = 5\text{k}\Omega$					0.9		dB
Channel separation	$f = 1\text{kHz}$, $R_S = 5\text{k}\Omega$		110			110		dB

FEATURES

- Turn off time less than $2\mu s$
- Maximum operating frequency greater than 500kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per $^{\circ}C$
- SE555 MII std 883A,B,C available M38510 (JAN) approved, M38510 processing available.

PIN CONFIGURATIONS



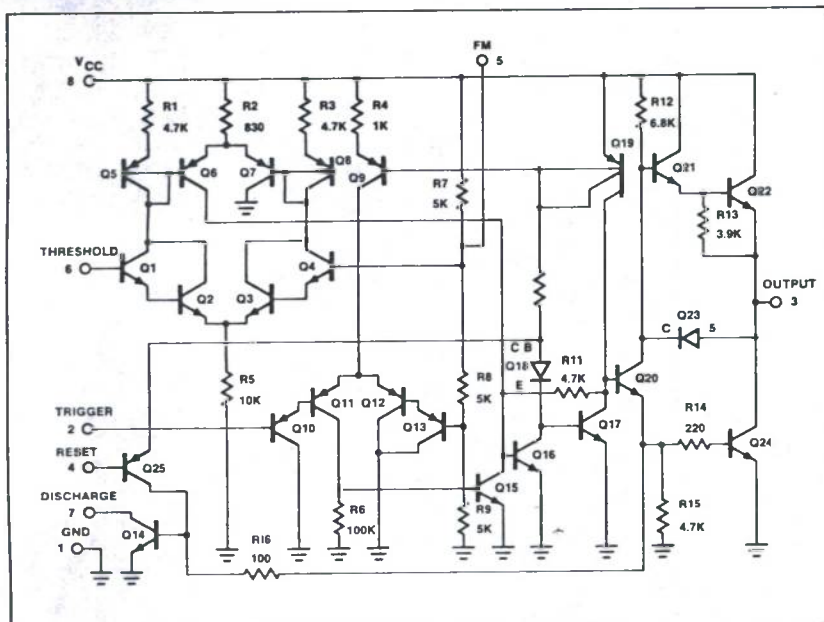
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector

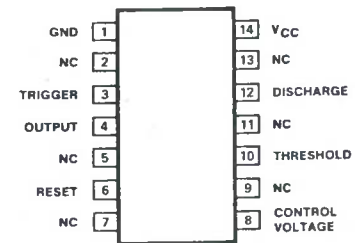
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE555	+18	V
NE555, SE555C,	+16	V
Power dissipation	600	mW
Operating temperature range		
NE555	0 to +70	$^{\circ}C$
SE555, SE555C	-55 to +125	$^{\circ}C$
Storage temperature range	-65 to +150	$^{\circ}C$
Load temperature (soldering, 60sec)	300	$^{\circ}C$

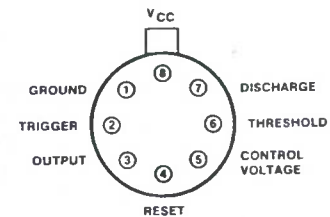
EQUIVALENT SCHEMATIC



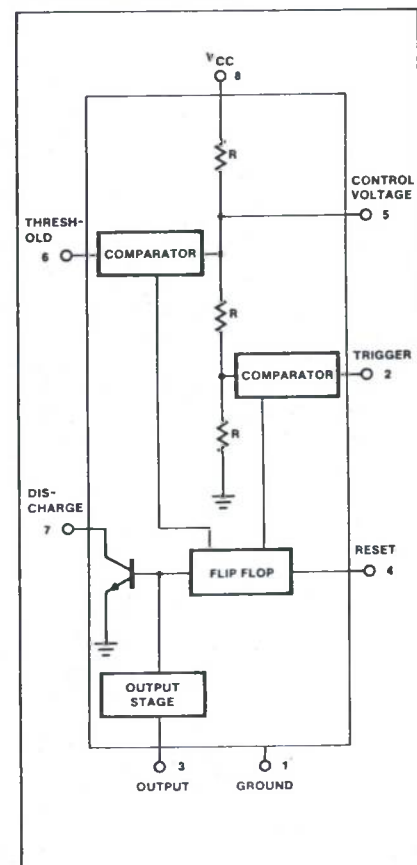
F,N-14 PACKAGE



H PACKAGE



BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = +5\text{V}$ to $+15$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE555			NE555/SE555C			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (low state) ¹	$V_{CC} = 5\text{V } R_L = \infty$ $V_{CC} = 15\text{V } R_L = \infty$		3 10	5 12		3 10	6 15	mA mA
Timing error (monostable) Initial accuracy ² Drift with temperature Drift with supply voltage	$R_A = 2\text{k}\Omega$ to $100\text{k}\Omega$ $C = 0.1\mu\text{F}$		0.5 30 0.05	2.0 100 0.2		1.0 50 0.1	3.0 — 0.5	% ppm/ $^\circ\text{C}$ %/V
Timing error (astable) Initial accuracy ² Drift with temperature Drift with supply voltage	$R_A, R_B = 1\text{k}\Omega$ to $100\text{k}\Omega$ $C = 0.1\mu\text{F}$ $V_{CC} = 15\text{V}$		1.5 90 0.15	— — —		2.25 150 0.3	— — —	% ppm/ $^\circ\text{C}$ %/V
Control voltage level	$V_{CC} = 15\text{V}$	9.6	10.0	10.4	9.0	10.0	11.0	V
Threshold voltage	$V_{CC} = 5\text{V}$	2.9	3.33	3.8	2.6	3.33	4.0	V
	$V_{CC} = 15\text{V}$	9.4	10.0	10.6	8.8	10.0	11.2	V
	$V_{CC} = 5\text{V}$	2.7	3.33	4.0	2.4	3.33	4.2	V
Threshold current ³			0.1	0.25		0.1	0.25	μA
Trigger voltage	$V_{CC} = 15\text{V}$	4.8	5.0	5.2	4.5	5.0	5.6	V
Trigger current	$V_{CC} = 5\text{V}$	1.45	1.67	1.9	1.1	1.67	2.2	V
	$V_{TRIG} = 0\text{V}$		0.5	0.9		0.5	2.0	μA
			0.7	1.0	0.4	0.7	1.0	V
Reset voltage ⁴		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset current			0.1	0.4		0.1	0.4	mA
Reset current	$V_{RESET} = 0\text{V}$		0.4	1.0		0.4	1.5	mA
Output voltage (low)	$V_{CC} = 15\text{V}$							
	$I_{SINK} = 10\text{mA}$		0.1	0.15		0.1	0.25	V
	$I_{SINK} = 50\text{mA}$		0.4	0.5		0.4	0.75	V
	$I_{SINK} = 100\text{mA}$		2.0	2.2		2.0	2.5	V
	$I_{SINK} = 200\text{mA}$		2.5	—		2.5	—	V
	$V_{CC} = 5\text{V}$							
Output voltage (high)	$I_{SINK} = 8\text{mA}$		0.1	0.25		0.3	0.4	V
	$I_{SINK} = 5\text{mA}$		0.05	0.2		0.25	0.35	V
	$V_{CC} = 15\text{V}$							
	$I_{SOURCE} = 200\text{mA}$		12.5	—		12.5	—	V
	$I_{SOURCE} = 100\text{mA}$	13.0	13.3	—	12.75	13.3	—	V
	$V_{CC} = 5\text{V}$							
Turn off time ⁵	$I_{SOURCE} = 100\text{mA}$	3.0	3.3	—	2.75	3.3	—	V
	$V_{RESET} = V_{CC}$		0.5	2.0		0.5	—	μs
Rise time of output			100	200		100	300	ns
Fall time of output			100	200		100	300	ns
Discharge leakage current			20	100		20	100	na

NOTES

1. Supply current when output high typically 1mA less.
2. Tested at $V_{CC} = 5\text{V}$ and $V_{CC} = 15\text{V}$.
3. This will determine the maximum value of $R_A + R_B$, for 15V operation, the max total $R = 10$ megohm, and for 5V operation, the max total $R = 3.4$ megohm.
4. Specified with trigger input high.
5. Time measured from a positive going input pulse from 0 to $0.8 \times V_{CC}$ into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

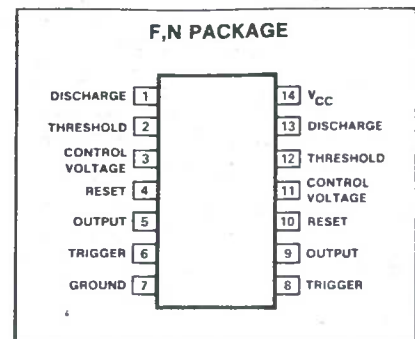
FEATURES

- Timing from microseconds to hours
- Replaces two 555 timers
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C
- SE566 MIL STD 883A, B, C available, N38510 (JAN planned, 38510 processing available).

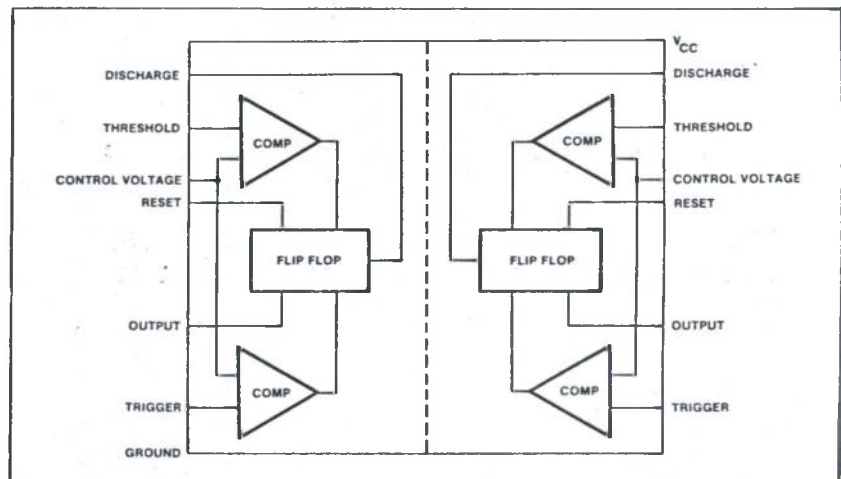
APPLICATIONS

- Precision timing
- Sequential timing
- Pulse shaping
- Pulse generator
- Missing pulse detector
- Tone burst generator
- Pulse width modulation
- Time delay generator
- Frequency division
- Industrial controls
- Pulse position modulation
- Appliance timing
- Traffic light control
- Touch tone encoder

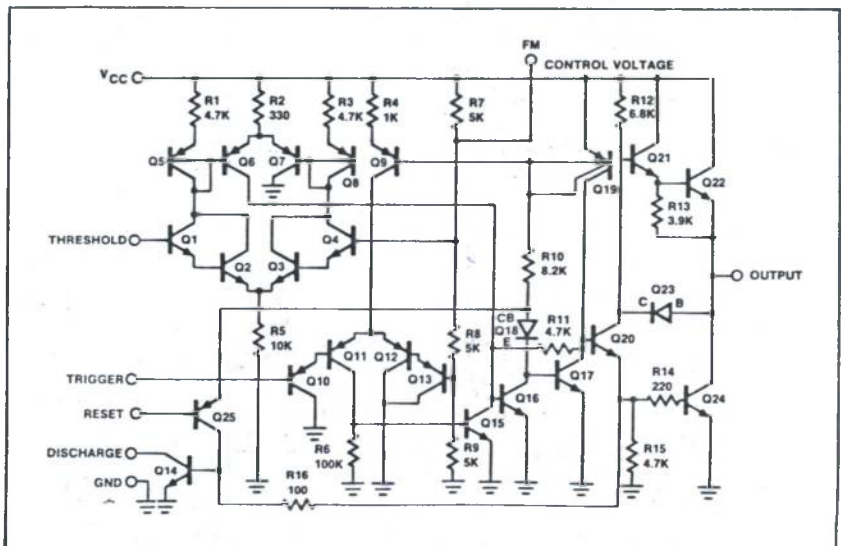
PIN CONFIGURATION



BLOCK DIAGRAM



EQUIVALENT SCHEMATIC (Shown for one circuit only)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+18	V
SE556	+16	V
NE556, SE556C,	600	mW
Power dissipation		
Operating temperature range	0 to +70	°C
NE556	-55 to +125	°C
SE556, SE556C	-65 to +150	°C
Storage temperature range	+300	°C
Lead temperature		
(Soldering, 60 sec)		

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = +5\text{V}$ to $+15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE556			NE556/SE556C			UNITS
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (low state) ¹	$V_{CC} = 5\text{V}$ $R_L = \infty$		6	10		6	12	mA
	$V_{CC} = 15\text{V}$ $R_L = \infty$		20	24		20	30	mA
Timing error (monostable)	$R_A = 2\text{k}\Omega$ to $100\text{k}\Omega$							
Initial accuracy ²	$C = 0.1\mu\text{F}$		0.5	1.5		0.75	3.0	%
Drift with temperature			30	100		50		ppm/°C
Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
Timing error (astable)	$R_A, R_B = 1\text{k}\Omega$ to $100\text{k}\Omega$							
Initial accuracy ²	$C = 0.1\mu\text{F}$		1.5			2.25		%
Drift with temperature	$V_{CC} = 15\text{V}$		90			150		ppm/°C
Drift with supply voltage			0.15			0.3		%/V
Control voltage level	$V_{CC} = 15\text{V}$	9.6	10.0	10.4	9.0	10.0	11.0	V
	$V_{CC} = 5\text{V}$	2.9	3.33	3.8	2.6	3.33	4.0	V
Threshold voltage	$V_{CC} = 15\text{V}$	9.4	10.0	10.6	8.8	10.0	11.2	V
	$V_{CC} = 5\text{V}$	2.7	3.33	4.0	2.4	3.33	4.2	V
Threshold current ³			30	250		30	250	nA
Trigger voltage	$V_{CC} = 15\text{V}$	4.8	5.0	5.2	4.5	5.0	5.6	V
	$V_{CC} = 5\text{V}$	1.45	1.67	1.9	1.1	1.67	2.2	V
Trigger current	$V_{TRIG} = 0\text{V}$		0.5	0.9		0.5	2.0	μA
Reset voltage ⁵		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset current	$V_{RESET} = 0\text{V}$		0.1	0.4		0.1	0.6	mA
			0.4	1.0		0.4	1.5	mA
Output voltage (low)	$V_{CC} = 15\text{V}$							
	$I_{SINK} = 10\text{mA}$		0.1	0.15		0.1	0.25	V
	$I_{SINK} = 50\text{mA}$		0.4	0.5		0.4	0.75	V
	$I_{SINK} = 100\text{mA}$		2.0	2.25		2.0	3.2	V
	$I_{SINK} = 200\text{mA}$		2.5			2.5		V
	$V_{CC} = 5\text{V}$							
	$I_{SINK} = 8\text{mA}$		0.1	0.2		0.25	0.3	V
	$I_{SINK} = 5\text{mA}$		0.05	0.15		0.15	0.25	V
Output voltage (high)	$V_{CC} = 15\text{V}$							
	$I_{SOURCE} = 200\text{mA}$		12.5			12.5		V
	$I_{SOURCE} = 100\text{mA}$	13.0	13.3		12.75	13.3		V
	$V_{CC} = 5\text{V}$							
	$I_{SOURCE} = 100\text{mA}$	3.0	3.3		2.75	3.3		V
Rise time of output			100	200		100	300	ns
Fall time of output			100	200		100	300	ns
Discharge leakage current			20	100		20	100	nA
Matching characteristics ⁴								
	Initial accuracy ²		0.5	1.0		1.0	2.0	%
	Drift with temperature		10			10		ppm/°C
	Drift with supply voltage		0.1	0.2		0.2	0.5	%/V

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5MΩ PIN 7

ON TRIM

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ANALOG DEVICES

DACPORT™ Low Cost Complete μP-Compatible 8-Bit DAC

AD558

- FEATURES**
- Complete 8-Bit DAC
 - Voltage Output — 2 Calibrated Ranges
 - Internal Precision Band-Gap Reference
 - Single-Supply Operation: +5V to +15V
 - Full Microprocessor Interface
 - Fast: 1μs Voltage Settling to ±1/2LSB
 - Low Power: 75mW
 - No User Trims
 - Guaranteed Monotonic Over Temperature
 - All Errors Specified T_{min} to T_{max}
 - Small 16-Pin DIP Package
 - Single Laser-Wafer-Trimmed Chip for Hybrids
 - Low Cost

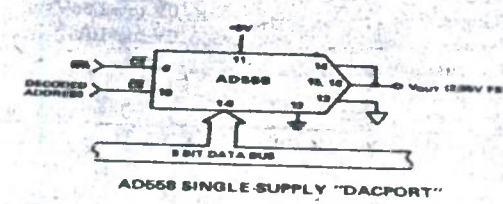
PRODUCT DESCRIPTION

The AD558 DACPORT is a complete voltage-output 8-bit digital-to-analog converter, including output amplifier, full microprocessor interface and precision voltage reference on a single monolithic chip. No external components or trims are required to interface, with full accuracy, an 8-bit data bus to an analog system.

The performance and versatility of the DACPORT is a result of several recently-developed monolithic bipolar technologies. The complete microprocessor interface and control logic is implemented with integrated injection logic (I²L), an extremely dense and low-power logic structure that is process-compatible with linear bipolar fabrication. The internal precision voltage reference is the patented low-voltage band-gap circuit* which permits full-accuracy performance on a single +5V to +15V power supply. Thin-film silicon-chromium resistors provide the stability required for guaranteed monotonic operation over the entire operating temperature range (all grades), while recent advances in laser-wafer-trimming of these thin-film resistors permit absolute calibration at the factory to within ±1LSB; thus no user-trims for gain or offset are required. A new circuit design provides voltage settling to ±1/2LSB for a full-scale step in 1μs.

The AD558 is available in four performance grades and two package types. The AD558J and K are specified for use over the 0 to +70°C temperature range and are available in either a 16-pin hermetically-sealed side-brazed ceramic DIP or a lower-cost 16-pin plastic DIP. The AD558S and T grades are specified for -55°C to +125°C operation and the hermetically-sealed ceramic package is standard. Processing to MIL-STD-883, Class B is optional on S and T grades.

*Covered by U.S. Patent No. 3,887,863.



AD558 SINGLE SUPPLY "DACPORT"



- PRODUCT HIGHLIGHTS**
1. The 8-bit I²L input register and fully microprocessor-compatible control logic allows the AD558 to be directly connected to 8- or 16-bit data buses and operated with standard control signals. The latch may be disabled for direct DAC interfacing.
 2. The laser-trimmed on-chip SiCr thin-film resistors are calibrated for absolute accuracy and linearity at the factory. Therefore, no user trims are necessary for full rated accuracy over the operating temperature range.
 3. The inclusion of a precision low-voltage band-gap reference eliminates the need to specify and apply a separate reference source.
 4. The voltage-switching structure of the AD558 DAC section along with a high-speed output amplifier and laser-trimmed resistors give the user a choice of 0V to +2.56V or 0V to +10V output ranges, selectable by pin-strapping. Circuitry is internally compensated for minimum settling time on both ranges; typically settling to ±1/2LSB for a full-scale 2.55 volt step in 700ns.
 5. The AD558 is designed and specified to operate from a single +4.5V to +16.5V power supply.
 6. Low digital input currents, 100μA max, minimize bus loading. Input thresholds are TTL/low voltage CMOS compatible over the entire operating V_{CC} range.

(continued on page 9-16)

SPECIFICATIONS

(typical @ $T_A = +25^\circ\text{C}$, $V_{CC} = +5\text{V}$ to $+15\text{V}$ unless otherwise specified)

MODEL	AD558J	AD558K	AD558S ¹	AD558T ¹
RESOLUTION	8 Bits	*	*	*
RELATIVE ACCURACY ²				
0 to $+70^\circ\text{C}$	$\pm 1/2\text{LSB}$ max	$\pm 1/4\text{LSB}$ max	*	***
-55°C to $+125^\circ\text{C}$	—	—	$\pm 3/4\text{LSB}$ max	$\pm 3/8\text{LSB}$ max
OUTPUT				
Ranges	0V to $+2.56\text{V}$ 0V to $+10\text{V}$ ³	*	*	*
Current, Source	$+5\text{mA}$	*	$+5\text{mA}$ min	***
Sink	Internal Passive Pull-Down to Ground ⁴	*	*	*
OUTPUT SETTLING TIME ⁵				
0 to 2.56 volt range	$0.8\mu\text{s}$ ($1.5\mu\text{s}$ max)	*	*	*
0 to 10 volt range ³	$2.0\mu\text{s}$ ($3.0\mu\text{s}$ max)	*	*	*
FULL SCALE ACCURACY				
@ 25°C	$\pm 1.5\text{LSB}$ ($\pm 0.6\%$) max	$\pm 0.5\text{LSB}$ ($\pm 0.2\%$) max	*	**
$T_{\min}$ to $T_{\max}$	$\pm 2.5\text{LSB}$ ($\pm 1.0\%$) max	$\pm 1\text{LSB}$ ($\pm 0.4\%$) max	*	**
ZERO ERROR				
@ 25°C	$\pm 1\text{LSB}$ max	$\pm 1/2\text{LSB}$ max	*	**
$T_{\min}$ to $T_{\max}$	$\pm 2\text{LSB}$ max	$\pm 1\text{LSB}$ max	*	**
MONOTONICITY ⁶				
$T_{\min}$ to $T_{\max}$	Guaranteed	*	*	*
DIGITAL INPUTS				
$T_{\min}$ to $T_{\max}$				
Input Current	$\pm 100\mu\text{A}$ max	*	*	*
Data Inputs, Voltage				
Bit On — Logic "1"	2.0V min	*	*	*
Bit Off — Logic "0"	0.8V max	*	*	*
Control Inputs, Voltage				
On — Logic "1"	2.0V min	*	*	*
Off — Logic "0"	0.8V max	*	*	*
TIMING ⁷				
$T_{\min}$ to $T_{\max}$				
t_W (Strobe Pulse Width)	100ns min	*	*	*
t_{DH} (Data Hold Time)	10ns max	*	*	*
t_{DS} (Data Set-Up Time)	100ns min	*	*	*
POWER SUPPLY				
Operating Voltage Range (V_{CC})				
2.56 Volt Range	$+4.5\text{V}$ to $+16.5\text{V}$	*	*	*
10 Volt Range	$+11.4\text{V}$ to $+16.5\text{V}$	*	*	*
Current (I_{CC})	15mA typ, 25mA max	*	*	*
Rejection Ratio	$0.03\%/%$ max	*	*	*
POWER DISSIPATION, $V_{CC} = 5\text{V}$	75mW (125mW max)	*	*	*
$V_{CC} = 15\text{V}$	225mW (375mW max)	*	*	*
OPERATING TEMPERATURE				
RANGE				
$T_{\min}$	0°C	*	-55°C	***
$T_{\max}$	$+70^\circ\text{C}$	*	$+125^\circ\text{C}$	***

NOTES

¹ The AD558S and AD558T are available fully processed and screened to the requirements of MIL-STD-883, Class B. A complete description is given on page 9-16 of this data sheet. Order AD558SD/883B or AD558TD/883B.

² Relative Accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

³ Operation of the 0 to 10 volt output range requires a minimum supply voltage of $+11.4$ volts.

⁴ Passive pull-down resistance is $2\text{k}\Omega$ for 2.56 volt range, $10\text{k}\Omega$ for 10 volt range.

⁵ Settling time is specified for a positive-going full-scale step. Negative-going steps to zero are slower, but can be improved with an external pull-down. See page 9-19 of this data sheet for details.

⁶ A monotonic converter has a maximum differential linearity error of $\pm 1\text{LSB}$.

⁷ See Figure 8, page 9-18.

*Specifications same as AD558J.

**Specifications same as AD558K.

***Specifications same as AD558S.

Specifications subject to change without notice.

ABSOLUTE MA

V_{CC} to Ground.
Digital Inputs (P
VOUT

Power Dissipation
Storage Tempera

N (plastic)
D (ceramic)

Lead Temperatu
Thermal Resistan

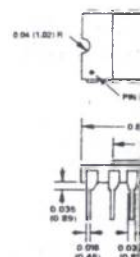
Junction to A
N (plastic)
D (ceramic)

(LSB)

(MSB)

Figure

D (C



(continued from page 9-13)

7. The single-chip, low power I²L design of the AD558 is inherently more reliable than hybrid multi-chip or conventional single-chip bipolar designs. The AD558S and T grades, which are specified over the -55°C to +125°C temperature range, are available fully processed to MIL-STD-883, Class B.
8. All AD558 grades are available in chip form with guaranteed specifications from +25°C to T_{max}. MIL-STD-883, Class B processing is standard on Analog Devices bipolar chips. Contact the factory for additional chip information.

CIRCUIT DESCRIPTION

The AD588 consists of four major functional blocks, fabricated on a single monolithic chip (see Figure 3). The main D to A converter section uses eight equally-weighted laser-trimmed current sources switched into a silicon-chromium thin-film R/2R resistor ladder network to give a direct but unbuffered 0mV to 400mV output range. The transistors that form the DAC switches are PNPs; this allows direct positive-voltage logic interface and a zero-based output range.

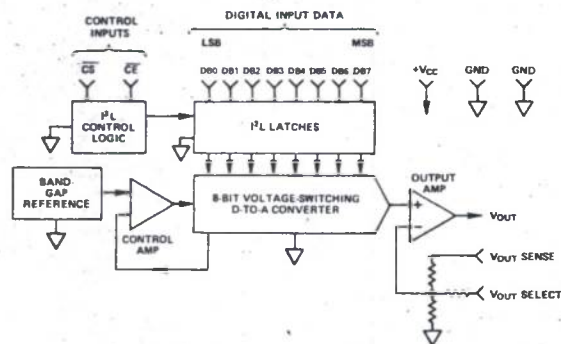


Figure 3. AD558 Functional Block Diagram

The high-speed output buffer amplifier is operated in the non-inverting mode with gain determined by the user-connections at the output range select pin. The gain-setting application resistors are thin-film laser-trimmed to match and track the DAC resistors and to assure precise initial calibration of the two output ranges, 0V to 2.56V and 0V to 10V. The amplifier output stage is an NPN transistor with passive pull-down for zero-based output capability with a single power supply.

The internal precision voltage reference is of the patented band-gap type. This design produces a reference voltage of 1.2 volts and thus, unlike 6.3 volt temperature-compensated zeners, may be operated from a single, low-voltage logic power supply.

The microprocessor interface logic consists of an 8-bit data latch and control circuitry. Low-power, small geometry and high-speed are advantages of the I²L design as applied to this section. I²L is bipolar process compatible so that the performance of the analog sections need not be compromised to provide on-chip logic capabilities. The control logic allows the latches to be operated from a decoded microprocessor address and write signal. If the application does not involve a μ P or data bus, wiring $\overline{CS}$ and $\overline{CE}$ to ground renders the latches "transparent" for direct DAC access.

MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD558, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. The available hermetically-sealed, low profile DIP package ("D" suffix) takes up a fraction of the space required by equivalent modular designs and protects the chip from hazardous environments. To further ensure reliability, military-temperature range AD558 grades S and T are available 100% screened to MIL-STD-883, Class B, method 5004. Table 1 details the test procedure.

TEST	METHOD
1) Internal Visual (Pre cap)	Method 2010, Test Condition B
2) Stabilization Bake	Method 1008, 24 hours @ +150°C
3) Temperature Cycling	Method 1010, Test Condition C, 10 Cycles, -65°C to +150°C
4) Constant Acceleration	Method 2001, Test Condition E, Y1 plane, 30kg
5) Seal, Fine and Gross	Method 1014, Test Condition A and C
6) Burn-in Test	Method 1014, Test Condition B, 160 hours @ +125°C min
7) Final Electrical Tests	Performed 100% to all min and max dc specifications on data pages.
8) External Visual	Method 2009

Table 1. MIL-STD-883, Class B Test Procedures

CONNECTING

The AD558 has reference, output internally. In a the factory ass only connection single jumper to board layout is one side of the p

Figure 4 shows The 0V to 2.56 power supply b range requires a

Because of its p tended to be op therefore no pr If a small increa accomplished by a buffer. A resisto output range.

For example if = 1LSB), a nom remembered th match and trac typically $\pm 20\%$ (0 to -100ppm) is performed. F full-scale outpu shown are nom NOTE: Decre GND will not u rents in GND. A recommended f

a.

b. U

Figur

TIMING AND CONTROL

The AD558 has data input latches that simplify interface to 8- and 16-bit data buses. These latches are controlled by Chip Enable ($\overline{CE}$) and Chip Select ($\overline{CS}$) inputs, pins 9 and 10 respectively. $\overline{CE}$ and $\overline{CS}$ are internally "NORed" so that the latches transmit input data to the DAC section when both $\overline{CE}$ and $\overline{CS}$ are at Logic "0". If the application does not involve a data bus, a "00" condition allows for direct operation of the DAC. When either $\overline{CE}$ or $\overline{CS}$ go to Logic "1", the input data is latched into the registers and held until both $\overline{CE}$ and $\overline{CS}$ return to "0". (Unused $\overline{CE}$ or $\overline{CS}$ inputs should be tied to ground.) The truth table is given in Table II. The logic function is also shown in Figure 7.

Input Data	$\overline{CE}$	$\overline{CS}$	DAC Data	Latch Condition
0	0	0	0	"transparent"
1	0	0	1	"transparent"
0	$\uparrow$	0	0	latching
1	$\uparrow$	0	1	latching
0	0	$\uparrow$	0	latching
1	0	$\uparrow$	1	latching
X	1	X	previous data	latched
X	X	1	previous data	latched

Notes: X = Does not matter
 $\uparrow$ = Logic Threshold at Positive-Going Transition

Table II. AD558 Control Logic Truth Table

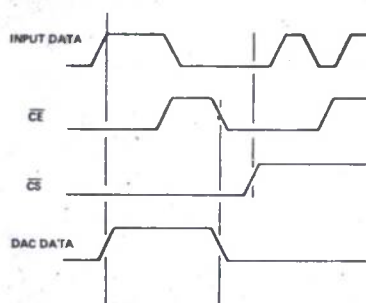


Figure 7. AD558 Control Logic Function

Figure 8 shows the timing for the data and control signals; $\overline{CE}$ and $\overline{CS}$ are identical in timing as well as in function.

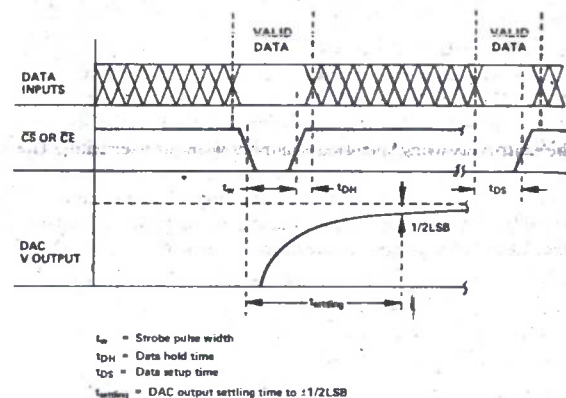
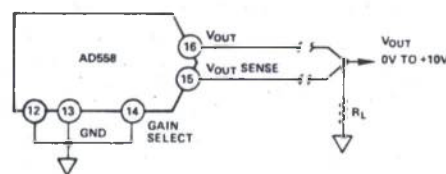


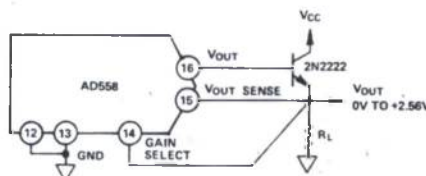
Figure 8. AD558 Timing

USE OF V_{OUT} SENSE

Separate access to the feedback resistor of the output amplifier allows additional application versatility. Figure 9a shows how $I \times R$ drops in long lines to remote loads may be cancelled by putting the drops "inside the loop". Figure 9b shows how the separate sense may be used to provide a higher output current by feeding back around a simple current booster.



a. Compensation for $I \times R$ Drops in Output Lines



b. Output Current Booster

Figure 9. Use of V_{OUT} sense

OPTIMIZING SENSE

In order to provide output voltage regulation, a "pull-down" resistor is required to bring output steps to zero. The resistor value is determined by the output step and the output capacitance. A negative-going step requires a pull-down resistor from the output to zero voltage output.

BIPOLAR OUTPUT

The AD558 has a supply and is thus capable of providing a bipolar output offsetting voltage output range is available. The 1.2 volt reference voltage output swing is available. The AD544 output swing is available. The AD544 output swing is available.

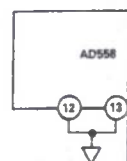


Figure 11. Bipolar Output

INTERFACING BUSES*

The AD558 is connected in memory that allows data to be read later via the RA. The AD558 is connected in memory that allows data to be read later via the RA. The AD558 is connected in memory that allows data to be read later via the RA.

DESCRIPTION

The NE564 is a versatile, high frequency Phase Locked Loop designed for operation up to 50MHz. As shown in the block diagram, the NE564 consists of a VCO, limiter, phase comparator, and post detection processor.

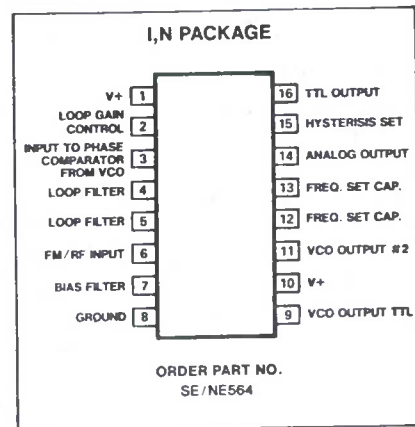
APPLICATIONS

- High speed modems
- FSK receivers and transmitters
- Frequency synthesizers
- Signal generators

FEATURES

- Operation with single 5V supply
- TTL compatible inputs and outputs
- Operation to 50MHz
- External loop gain control
- Reduced carrier feedthrough
- No elaborate filtering needed in FSK applications
- Can be used as a modulator
- Variable loop gain (Externally Controlled)

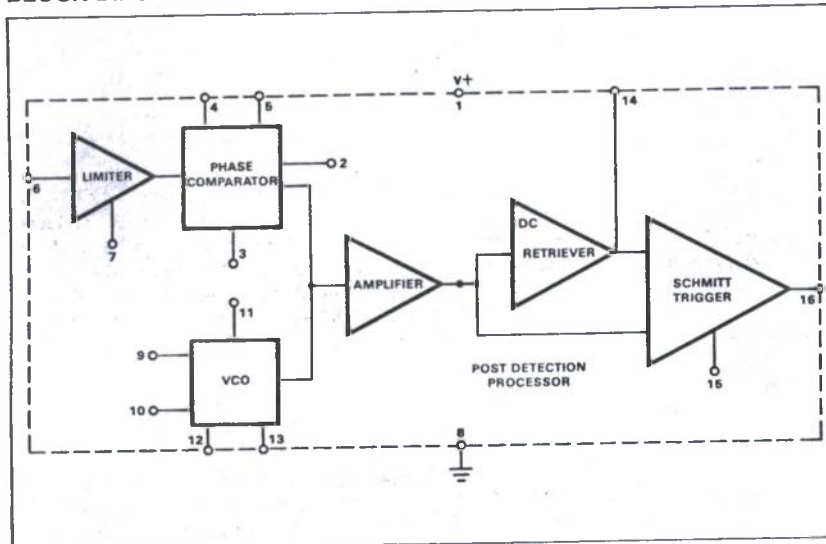
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER			RATING	UNIT
V+	Supply voltage		14	V
	Pin 1		6	
	Pin 10		400	mW
P _D	Power dissipation		0 to 70	°C
T _A	Operating temperature	NE	-55 to +125	°C
	Operating temperature	SE	-65 to 150	°C
t _{stg}	Storage temperature			°C

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The NE564 is a monolithic phase locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to greater than 50MHz. In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output voltage of the PLL can be written as shown in the following equation:

$$V_O = \frac{(f_{in} - f_o)}{K_{VCO}} \quad \text{Equation 1}$$

K_{VCO} = conversion gain of the VCO (see figure 7)
 f_{in} = frequency of the input signal
 f_o = free running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output of the PLL due to the wideband nature of the loop filter. To avoid the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of f_{in} from f_o . Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is

ELECTRICAL CHARACTERISTICS

$V_+ = 5V$, $T_A = 25^\circ C$, $f_o = 5MHz$, $I_B = -200\mu A$ unless otherwise specified.
Test Circuit: Figure 1

PARAMETER	TEST CONDITIONS	SE564			NE564			UNIT
		Min	Typ	Max	Min	Typ	Max	
Maximum VCO frequency		50	65		45	60		MHz
Lock range	Input $\geq 200\text{mVrms}$, $T_A = 25^\circ\text{C}$ $= 125^\circ\text{C}$ $= -55^\circ\text{C}$ $= 0^\circ\text{C}$ $= 70^\circ\text{C}$	60 30 120	90 50 150		60 100 50	90 120 70		% of fo
Capture range	Input $\geq 200\text{mVrms}$, $R_2 = 27\Omega$ $= 100\Omega$	25 35	35 50		25 35	35 50		% of fo
VCO frequency drift with temperature	fo = 5MHz, $T_A = -55^\circ\text{C}$ to 125°C $= 0^\circ\text{C}$ to 70°C fo = 500kHz, $T_A = -55^\circ\text{C}$ to 125°C $= 0^\circ\text{C}$ to 70°C		400 250	1000 500		400 400	1250 850	PPM / °C
VCO frequency change with supply voltage	V+ = 4.5V to 5.5V		3	6		3	6	% of fo
Demodulated output voltage	Modulation frequency: 1kHz, fo = 5MHz Input deviation: 10%, T = 25°C : 1%, T = 25°C T = 0°C = -55°C = 70°C = 125°C	120 12 9 14	140 14 12 16		120 12 11 13	140 14 13 15		mVrms mVrms mVrms mVrms mVrms
Linearity	Deviation: 1% to 8%		1 3			1 3		%
Signal to noise ratio AM rejection			40 35			40 35		dB dB
Supply current	V+ = 5V		35	50		35	50	mA
Leakage current	Pin 9		1	10		1	10	μA
Output current	Pin 9			6			6	mA
Supply voltage	Pin 1 Pin 10	4.5 4.5		12 5.5	4.5 4.5		12 5.5	V V

accomplished in the 564 by varying the voltage at pin 15 which results in a change of the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the dc levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrow band signals where the deviation in f_{in} itself may be less than the change in f_0 due to temperature. This effect can be eliminated if the dc or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the dc levels of the PLL output do not affect the FSK output.

VCO Section

Due to its inherent high frequency performance, an emitter coupled oscillator is used in the VCO. In the circuit, shown in the equi-

valent schematic, transistors Q₂₁ and Q₂₃ with current sources Q₂₅–Q₂₆ form the basic oscillator. The free running frequency of the oscillator is shown in the following equation:

$$f_o = \frac{1}{16R_C C_1}$$

Equation 2

$R_C = R_{19} = R_{20} = 100\Omega$ (INTERNAL)
 C_1 = external frequency setting capacitor

Variation of V_D (phase detector output voltage) changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative temperature coefficient due to the positive temperature coefficient of the monolithic resistor. To compensate for this, a current I_R with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

Phase Comparator Section

The phase comparator consists of a double balanced modulator with a limiter amplifier

to improve AM rejection. Schottky clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied by changing the current in Q₄ and Q₁₅ which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at pin 2.

Post Detection Processor Section

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a dc retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysteresis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the dc retriever is formed by the transductance amplifier Q₄₂-Q₄₃ together with an external capacitor which is connected at the am-

plifier output (pin 14). This forms an integrator whose output voltage is shown in the following equation:

$$V_0 = \frac{g_m}{C_2} \int V_{in} dt \quad \text{Equation 3}$$

g_m = transconductance of the amplifier
 C_2 = capacitor at the output (pin 14)
 V_{in} = signal voltage at amplifier input

With proper selection of C_2 , the integrator time constant can be varied so that the output voltage is the dc or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysteresis is made up of Q49-Q50 with positive feedback being provided by Q47-Q48. The hysteresis is varied by changing the current in Q52 with a resulting variation in the loop gain of the comparator. This method of hysteresis control, which is a dc control, provides symmetric variation around the nominal value.

Design Formula

The free running frequency of the VCO is shown by the following equation:

$$f_o = \frac{1}{16R_C C_1} \text{ in Hz} \quad \text{Equation 4}$$

$R_C = 100\Omega$
 C_1 = external cap in farads

The loop filter diagram shown is explained by the following equation:

$$F(s) = \frac{1}{1 + sRC_3} \quad \text{Equation 5}$$

$R = R_{12} = R_{13} = 1.3k\Omega$ (INTERNAL)

By adding capacitors to pins 4 and 5, two poles are added to the loop transfer function

$$\text{at } \omega = \frac{1}{RC_3}$$

FM DEMODULATOR

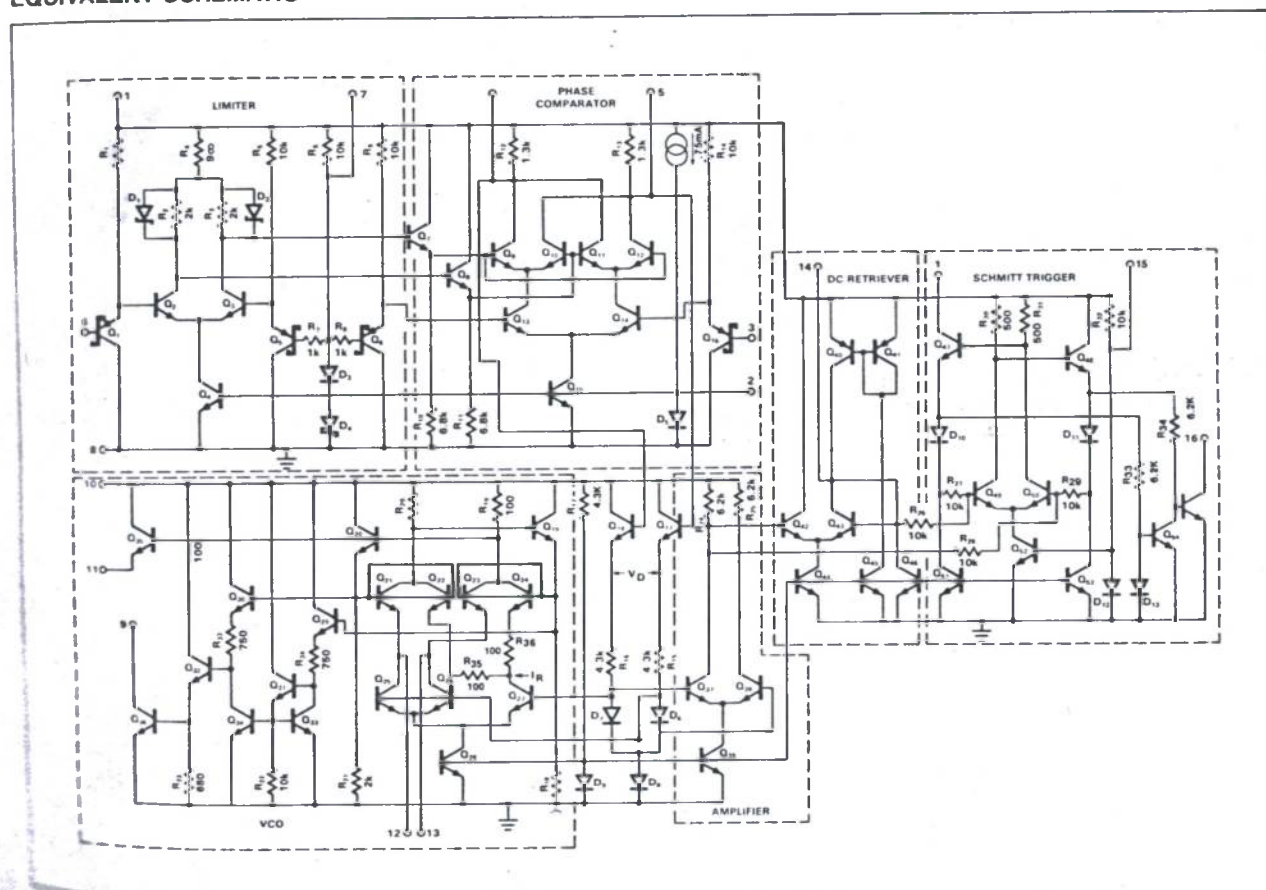
The NE564 can be used as an FM demodulator. The connections for operation

at 5V and 12V are shown in figures 2 and 3 respectively. The input signal is ac coupled with the output signal being extracted at pin 14. Loop filtering is provided by the capacitors at pins 4 and 5 with additional filtering being provided by the capacitor at pin 14. Since the conversion gain of the VCO is not very high, to obtain sufficient demodulated output signal the frequency deviation in the input signal should be fairly high (1% or higher).

MODULATION TECHNIQUES

The NE564 phase locked loop can be modulated at either the loop filter ports (pins 4 and 5) or the input port (pin 6) as shown in figure 4. The approximate modulation frequency can be determined from the frequency conversion gain curve shown in figure 5. This curve will be appropriate for signals injected into pins 4 and 5 as shown in figure 4.

EQUIVALENT SCHEMATIC



Am592

Differential Video Amplifier

PRELIMINARY DATA

Distinctive Characteristics

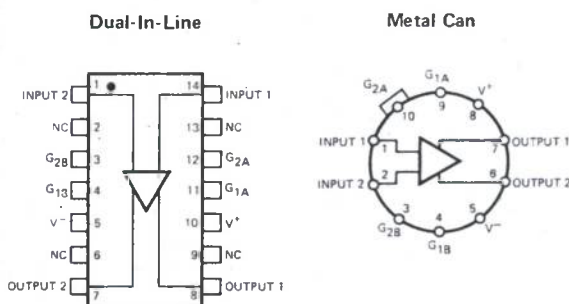
- The Am592 and Am592C differential video amplifiers are functionally, electrically and pin-for-pin equivalent to the Signetics SE592 and NE592.
- Bandwidths: 40 to 120 MHz
- Rise times: 2.5 to 10 ns
- Propagation delay: 3.6 to 10 ns
- 100% reliability assurance testing in compliance with MIL-STD-883A
- Electrically tested and optically inspected dice for hybrid manufacturers
- 120 MHz bandwidth
- Adjustable gains from 0 to 400
- Adjustable pass band
- No frequency compensation required
- Available in metal can, hermetic dual-in-line or plastic dual-in-line packages

FUNCTIONAL DESCRIPTION

The Am592/Am592C is a monolithic, two stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems.

CONNECTION DIAGRAMS

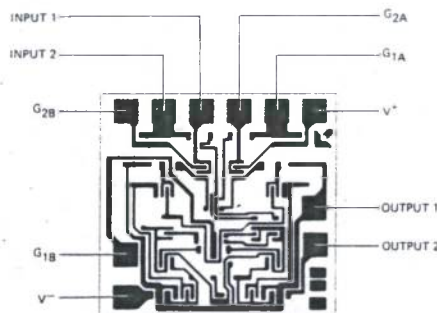
Top Views



ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am592C	TO-100	0°C to +70°C	AM592HC
	DIP	0°C to +70°C	AM592DC
	Molded DIP	0°C to +70°C	AM592PC
	Dice	0°C to +70°C	LD592C
Am592	TO-100	-55°C to +125°C	AM592HM
	DIP	-55°C to +125°C	AM592DM
	Dice	-55°C to +125°C	LD592

Metallization and Pad Layout



DIE SIZE 41 X 41 mils

Am592

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±8V
Differential Input Voltage	±5V
Common Mode Input Voltage	±6V
Output Current	10mA
Operating Temperature Range	
Am592	-55°C to +125°C
Am592C	0°C to + 70°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS Standard Conditions ($T_A = +25^\circ\text{C}$, $V_S = \pm 6\text{V}$, $V_{CM} = 0$ unless otherwise specified)

Parameter	Conditions			Am592C			Am592			Units
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Differential Voltage Gain	Gain 1	Note 1	$R_L = 2\text{k}\Omega$, $V_{OUT} = 3\text{V p-p}$	250	400	600	300	400	500	
	Gain 2	Note 2		80	100	120	90	100	110	
Bandwidth	Gain 1	Note 1			40			40		MHz
	Gain 2	Note 2			90			90		
Rise Time	Gain 1	Note 1	$V_{OUT} = 1\text{V p-p}$		11			11		ns
	Gain 2	Note 2			6.0	12		6.0	10	
Propagation Delay	Gain 1	Note 1	$V_{OUT} = 1\text{V p-p}$		7.5			7.5		ns
	Gain 2	Note 2			6.0	10		6.0	10	
Input Resistance	Gain 1	Note 1			4.0			4.0		$\text{k}\Omega$
	Gain 2	Note 2		10	30		20	30		
Input Capacitance	Gain 2	Note 2			2.0			2.0		pF
Input Offset Current					0.4	5.0		0.4	3.0	μA
Input Bias Current					9.0	30		9.0	20	μA
Input Noise Voltage			BW 1kHz to 10kHz		12			12		$\mu\text{V rms}$
Input Voltage Range						±1.0			±1.0	Volts
Common Mode Rejection Ratio	Gain 2	$V_{CM} \pm 1\text{V}$, $F < 100\text{kHz}$		60	86		60	86		dB
	Gain 2	$V_{CM} \pm 1\text{V}$, $F = 5\text{MHz}$			60			60		
Supply Voltage Rejection Ratio	Gain 2	$\Delta V_S = \pm 0.5\text{V}$		50	80		50	80		dB
Output Offset Voltage	Gain 3	Note 3 $R_L = \infty$			0.2	0.75		0.2	0.75	Volts
Output Common Mode Voltage		$R_L = \infty$		2.4	2.9	3.4	2.4	2.9	3.4	Volts
Output Voltage Swing		$R_L = 2\text{k}\Omega$, Single Ended		3.0	3.9		3.0	3.9		Volts
Output Resistance					20			20		Ω
Power Supply Current		$R_L = \infty$			16	24		16	24	mA

Recommended Operating Supply Voltage ($V_S = \pm 6.0\text{V}$)

- Notes: 1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

SY6522 Versatile Interface Adapter (VIA)

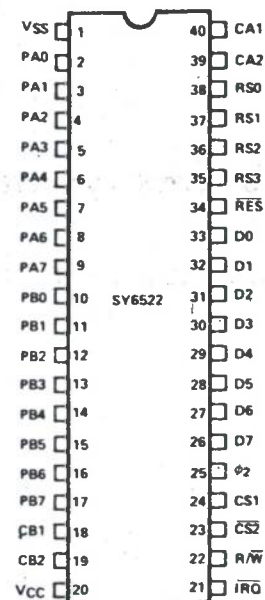
Features

- Two 8-Bit Bidirectional I/O Ports
- Two 16-Bit Programmable Timer/Counters
- Serial Data Port
- Single +5V Power Supply
- TTL Compatible
- CMOS-Compatible Peripheral Port A Lines
- Expanded "Handshake" Capability Allows Positive Control of Data Transfers Between Processor and Peripheral Devices
- Latched Output and Input Registers
- 1 MHz and 2 MHz Operation

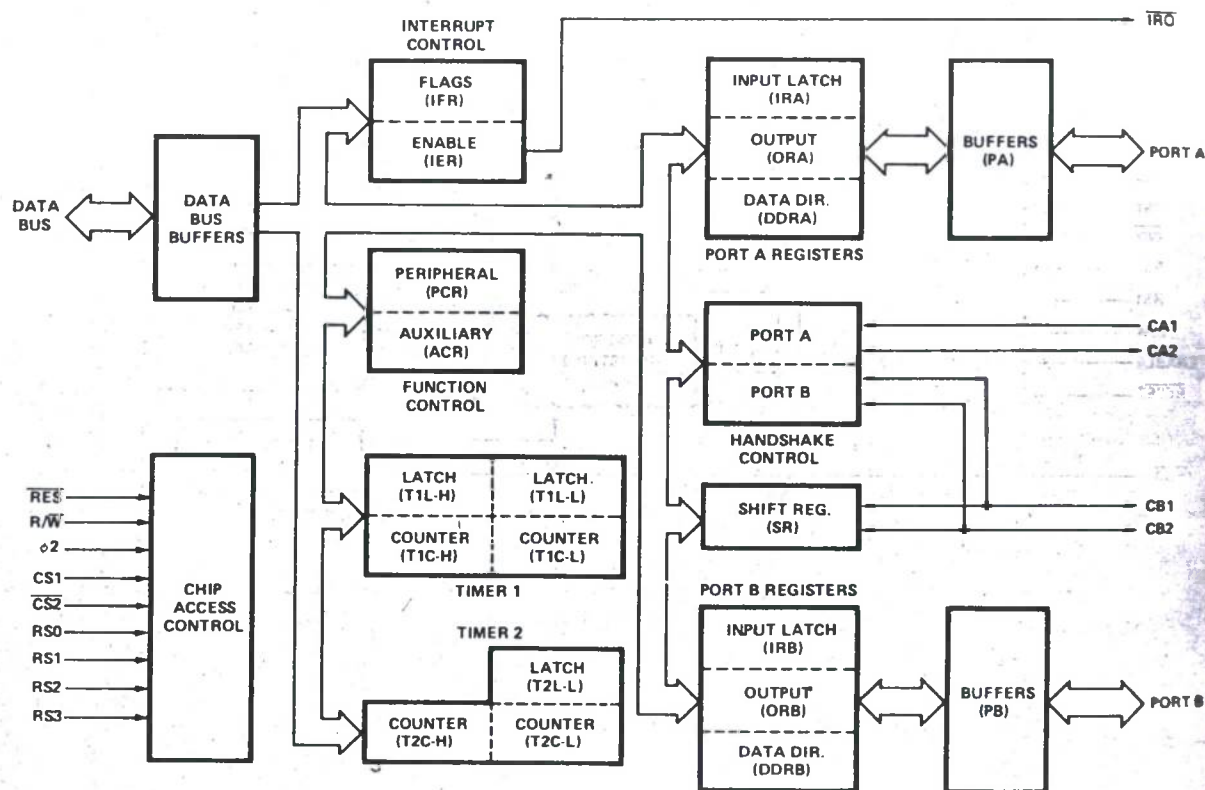
Ordering Information

Order Number	Package Type	Clock Rate
SYC 6522	Ceramic	1 MHz
SYP 6522	Plastic	1 MHz
SYC 6522A	Ceramic	2 MHz
SYP 6522A	Plastic	2 MHz

Pin Configuration



Block Diagram



Synertek

MICROPROCESSOR



SYNERTEK INC.

P.O. BOX 552 - MS/34

SANTA CLARA, CA 95052

TEL (408) 988-5600

TWX 910-333-3333

6551 Asynchronous Communication Interface Adapter

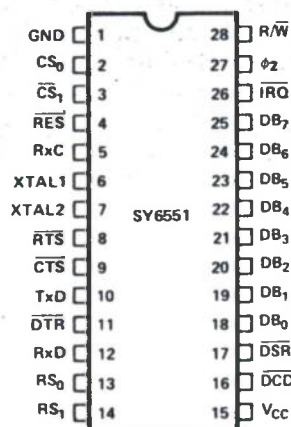
Features

- On-chip baud rate generator: 15 programmable baud rates derived from a standard 1.8432 MHz external crystal (50 to 19,200 baud).
- Programmable interrupt and status register to simplify software design.
- Single +5 volt power supply.
- Serial echo mode.
- False start bit detection.
- 8-bit bi-directional data bus for direct communication with the microprocessor.
- External 16x clock input for non-standard baud rates (up to 125 Kbaud).
- Programmable: word lengths; number of stop bits; and parity bit generation and detection.
- Data set and modem control signals provided.
- Parity: (odd, even, none, mark, space).
- Full-duplex or half-duplex operation.
- 5, 6, 7, 8 and 9 bit transmission.

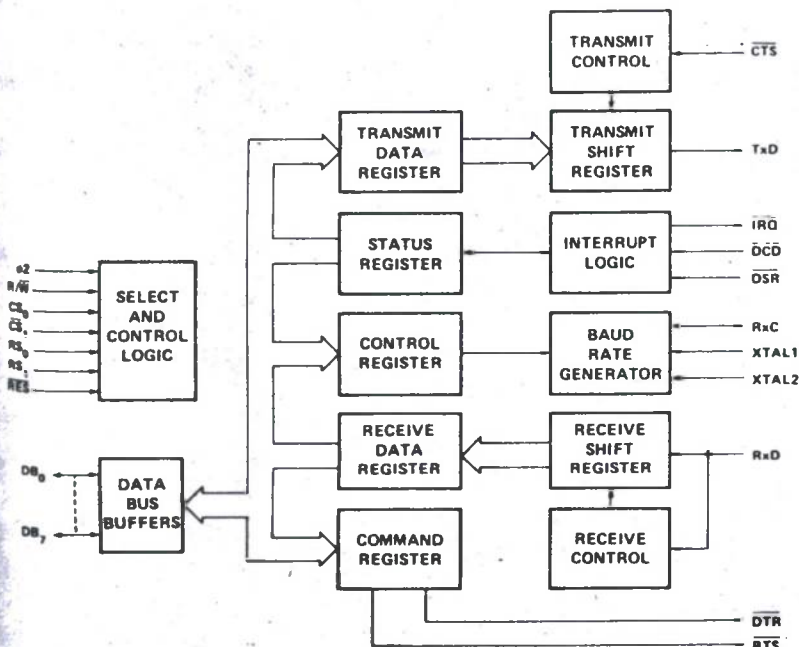
Ordering Information

Part No.	Package	Clock Rate
SYC6551	Ceramic	1 MHz
SYP6551	Plastic	1 MHz
SYC6551A	Ceramic	2 MHz
SYP6551A	Plastic	2 MHz

Pin Configuration



Block Diagram



Synertek

MICROPROCESSOR



**MOTOROLA**

SEMICONDUCTORS

3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

8-BIT MICROPROCESSING UNIT

The MC6809 is a revolutionary high-performance 8-bit microprocessor which supports modern programming techniques such as position independence, reentrancy, and modular programming.

This third-generation addition to the M6800 family has major architectural improvements which include additional registers, instructions, and addressing modes.

The basic instructions of any computer are greatly enhanced by the presence of powerful addressing modes. The MC6809 has the most complete set of addressing modes available on any 8-bit microprocessor today.

The MC6809 has hardware and software features which make it an ideal processor for higher level language execution or standard controller applications.

MC6800 COMPATIBLE

- Hardware — Interfaces with All M6800 Peripherals
- Software — Upward Source Code Compatible Instruction Set and Addressing Modes

ARCHITECTURAL FEATURES

- Two 16-bit Index Registers
- Two 16-bit Indexable Stack Pointers
- Two 8-bit Accumulators can be Concatenated to Form One 16-Bit Accumulator
- Direct Page Register Allows Direct Addressing Throughout Memory

HARDWARE FEATURES

- On-Chip Oscillator (Crystal Frequency = 4XE)
- DMA/BREQ Allows DMA Operation on Memory Refresh
- Fast Interrupt Request Input Stacks Only Condition Code Register and Program Counter
- MRDY Input Extends Data Access Times for Use with Slow Memory
- Interrupt Acknowledge Output Allows Vectoring By Devices
- SYNC Acknowledge Output Allows for Synchronization to External Event
- Single Bus-Cycle RESET
- Single 5-Volt Supply Operation
- NMI Inhibited After RESET Until After First Load of Stack Pointer
- Early Address Valid Allows Use With Slower Memories
- Early Write-Data for Dynamic Memories

SOFTWARE FEATURES

- 10 Addressing Modes
 - 6800 Upward Compatible Addressing Modes
 - Direct Addressing Anywhere in Memory Map
 - Long Relative Branches
 - Program Counter Relative
 - True Indirect Addressing
 - Expanded Indexed Addressing:
 - 0-, 5-, 8-, or 16-bit Constant Offsets
 - 8-, or 16-bit Accumulator Offsets
 - Auto-Increment/Decrement by 1 or 2
- Improved Stack Manipulation
- 1464 Instructions with Unique Addressing Modes
- 8 x 8 Unsigned Multiply
- 16-bit Arithmetic
- Transfer/Exchange All Registers
- Push/Pull Any Registers or Any Set of Registers
- Load Effective Address

MC6809

(1.0 MHz)

MC68A09

(1.5 MHz)

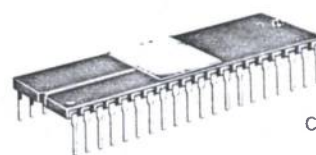
MC68B09

(2.0 MHz)

HMOS

(HIGH DENSITY N-CHANNEL, SILICON-GATE)

8-BIT MICROPROCESSING UNIT



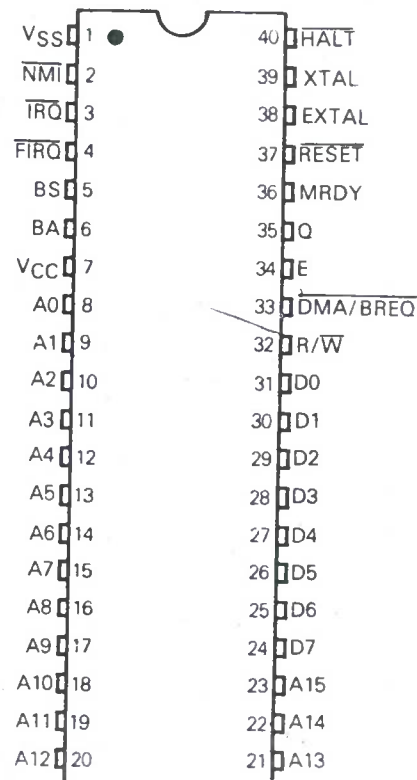
L SUFFIX
CERAMIC PACKAGE
CASE 715



P SUFFIX
PLASTIC PACKAGE
CASE 711



S SUFFIX
CERDIP PACKAGE
CASE 734

FIGURE 1 — PIN ASSIGNMENT

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.3 to +7.0	V
Input Voltage	V _{in}	-0.3 to +7.0	V
Operating Temperature Range MC6809, MC68A09, MC68B09 MC6809C, MC68A09C, MC68B09C	T _A	T _L to T _H 0 to +70 -40 to +85	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage levels (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance			
Ceramic	θ_{JA}	50	°C/W
Cerdip		60	
Plastic		100	

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D = P_{INT} + P_{PORT}

P_{INT} = I_{CC} × V_{CC}, Watts — Chip Internal Power.

P_{PORT} = Port Power Dissipation, Watts — User Determined

For most applications P_{PORT} ≤ P_{INT} and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K + (T_J + 273^\circ\text{C}) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \cdot (T_A + 273^\circ\text{C}) + \theta_{JA} \cdot P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted)

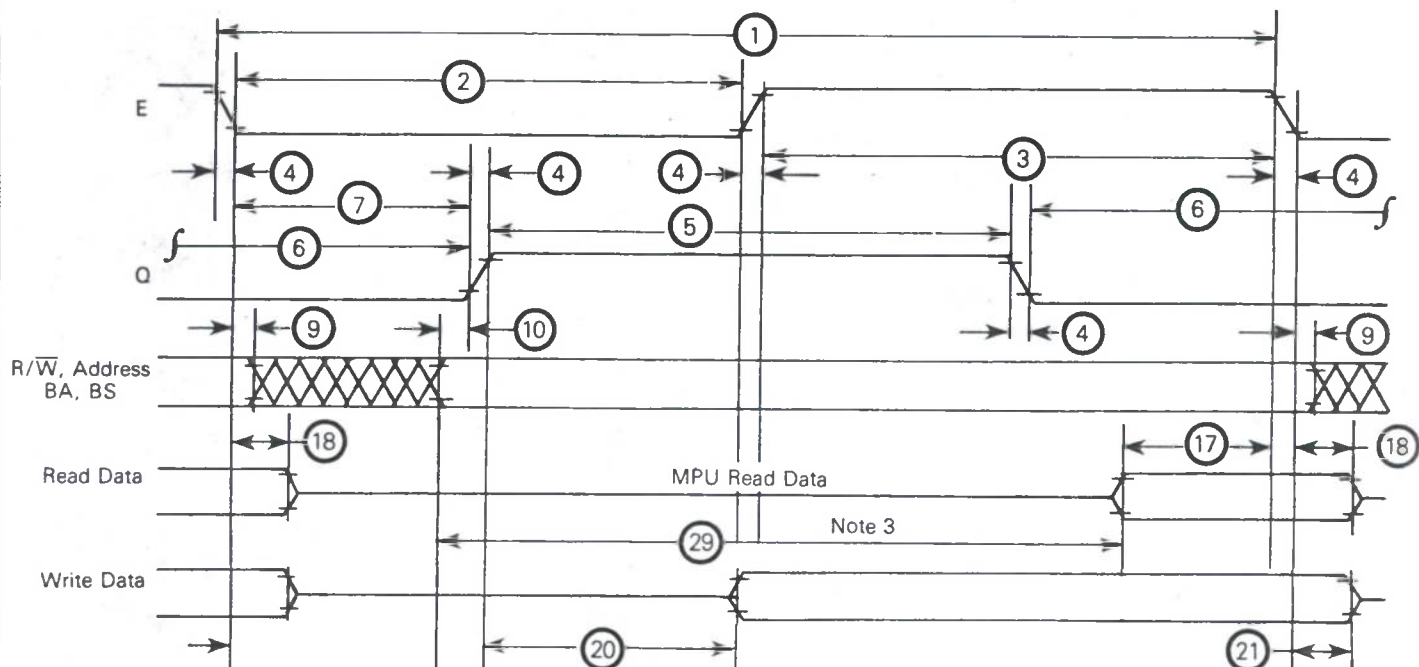
ELECTRICAL CHARACTERISTICS (V _{CC} =5.0 V ±5%, V _{SS} =0, T _A =0 to 70°C unless otherwise noted)		Symbol	Min	Typ	Max	Unit
Characteristic						
Input High Voltage	Logic, EXTERNAL	V _{IH}	V _{SS} +2.0	—	V _{CC}	V
	RESET	V _{IHR}	V _{SS} +4.0	—	V _{CC}	
Input Low Voltage	Logic, EXTERNAL, RESET	V _{IL}	V _{SS} -0.3	—	V _{SS} +0.8	V
Input Leakage Current (V _{in} =0 to 5.25 V, V _{CC} =max)	Logic	I _{in}	—	—	2.5	μA
DC Output High Voltage (I _{Load} =-205 μA, V _{CC} =min) (I _{Load} =-145 μA, V _{CC} =min) (I _{Load} =-100 μA, V _{CC} =min)	D0-D7	V _{OH}	V _{SS} +2.4	—	—	V
	A0-A15, R/W, Q, E		V _{SS} +2.4	—	—	
	BA, BS		V _{SS} +2.4	—	—	
DC Output Low Voltage (I _{Load} =2.0 mA, V _{CC} =min)		V _{OL}	—	—	V _{SS} +0.5	V
Internal Power Dissipation (measured at T _A =0°C in steady state operation)		P _{INT}	—	—	1.0	W
Capacitance # (V _{in} =0, T _A =25°C, f=1.0 MHz)	D0-D7, RESET	C _{in}	—	10	15	pF
	Logic Inputs, EXTERNAL, XTAL		—	10	15	
	A0-A15, R/W, BA, BS	C _{out}	—	—	15	pF
Frequency of Operation (Crystal or External Input)	MC6809	f _{XTAL}	0.4	—	4	MHz
	MC68A09		0.4	—	6	
	MC68B09		0.4	—	8	
Three-State (Off State) Input Current (V _{in} =0.4 to 2.4 V, V _{CC} =max)	D0-D7 A0-A15, R/W	I _{TSI}	— —	2.0 —	10 100	μA

capacitances are periodically tested rather than 100% tested.



MOTOROLA Semiconductor Products Inc.

FIGURE 2 — BUS TIMING



BUS TIMING CHARACTERISTICS (See Notes 1 and 2)

Ident. Number	Characteristics	Symbol	MC6809		MC68A09		MC68B09		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time (See Note 5)	t_{cyc}	1.0	10	0.667	10	0.5	10	μs
2	Pulse Width, E Low	PW_{EL}	430	5000	280	5000	210	5000	ns
3	Pulse Width, E High	PW_{EH}	450	15500	280	15700	220	15700	ns
4	Clock Rise and Fall Time	t_r, t_f	—	25	—	25	—	20	ns
5	Pulse Width, Q High	PW_{QH}	430	5000	280	5000	210	5000	ns
6	Pulse Width, Q Low	PW_{QL}	450	15500	280	15700	220	15700	ns
7	Delay Time, E to Q Rise	t_{AVS}	200	250	130	165	80	125	ns
9	Address Hold Time* (See Note 4)	t_{AH}	20	—	20	—	20	—	ns
10	BA, BS, R/W, and Address Valid Time to Q Rise	t_{AQ}	50	—	25	—	15	—	ns
17	Read Data Setup Time	t_{DSR}	80	—	60	—	40	—	ns
18	Read Data Hold Time*	t_{DHR}	10	—	10	—	10	—	ns
20	Data Delay Time from Q	t_{DDQ}	—	200	—	140	—	110	ns
21	Write Data Hold Time*	t_{DHW}	30	—	30	—	30	—	ns
29	Usable Access Time (See Note 3)	t_{ACC}	695	—	440	—	330	—	ns
	Processor Control Setup Time (MRDY, Interrupts, $\overline{DMA/BREQ}$, HALT, RESET) (Figures 7, 9, 10, 11, 13, and 14)	t_{PCS}	200	—	140	—	110	—	ns
	Crystal Oscillator Start Time (Figures 7 and 8)	t_{RC}	—	100	—	100	—	100	ms
	Processor Control Rise and Fall Time (Figures 7 and 9)	t_{PCr}, t_{PCf}	—	100	—	100	—	100	ns

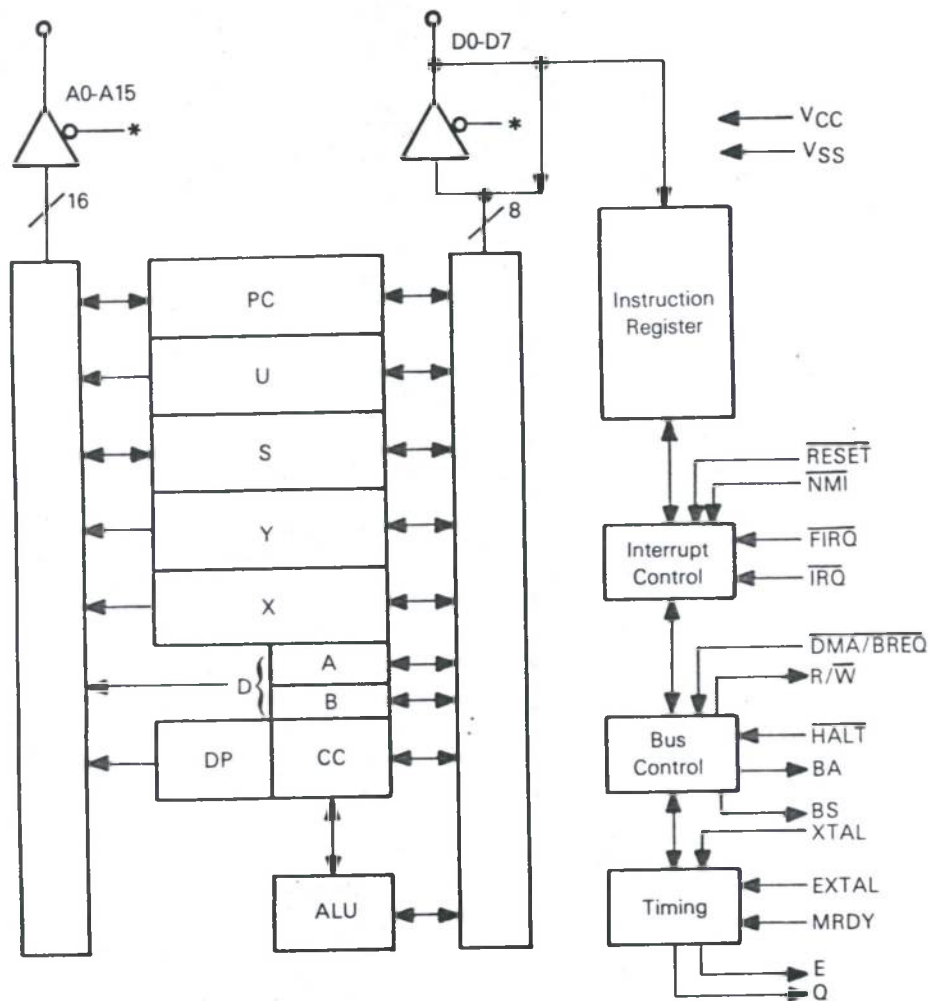
* Address and data hold times are periodically tested rather than 100% tested.

NOTES:

1. Voltage levels shown are $V_L \leq 0.4 V$, $V_H \geq 2.4 V$, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.
3. Usable access time is computed by: $1 - 4 - 7 \text{ max} + 10 - 17$.
4. Hold time (9) for BA and BS is not specified.
5. Maximum t_{cyc} during MRDY or $\overline{DMA/BREQ}$ is 16 μs .

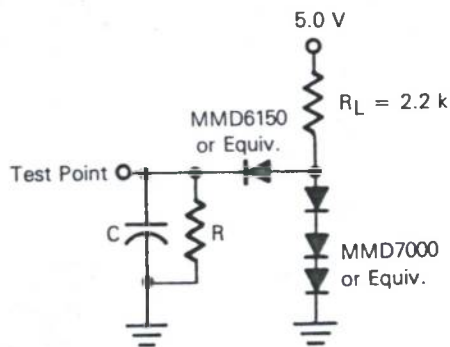


FIGURE 3 — MC6809 EXPANDED BLOCK DIAGRAM



* Internal Three-State Control

FIGURE 4 — BUS TIMING TEST LOAD



C = 30 pF for BA, BS
 130 pF for D0-D7, E, Q
 90 pF for A0-A15, R/W

R = 11.7 kΩ for D0-D7
 16.5 kΩ for A0-A15, E, Q, R/W
 24 kΩ for BA, BS

PROGRAMMING MODEL

As shown in Figure 5, the MC6809 adds three registers to the set available in the MC6800. The added registers include a Direct Page Register, the User Stack pointer and a second Index Register.

ACCUMULATORS (A, B, D)

The A and B registers are general purpose accumulators which are used for arithmetic calculations and manipulation of data.

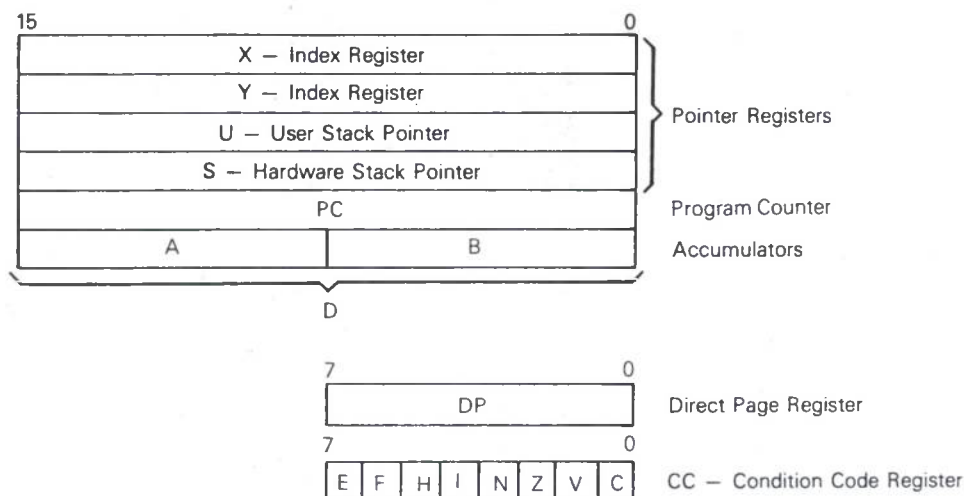
Certain instructions concatenate the A and B registers to form a single 16-bit accumulator. This is referred to as the D Register, and is formed with the A Register as the most significant byte.

DIRECT PAGE REGISTER (DP)

The Direct Page Register of the MC6809 serves to enhance the Direct Addressing Mode. The content of this register appears at the higher address outputs (A8-A15) during direct Addressing Instruction execution. This allows the direct mode to be used at any place in memory, under program control. To ensure 6800 compatibility, all bits of this register are cleared during Processor Reset.



FIGURE 5 — PROGRAMMING MODEL OF THE MICROPROCESSING UNIT



INDEX REGISTERS (X, Y)

The Index Registers are used in indexed mode of addressing. The 16-bit address in this register takes part in the calculation of effective addresses. This address may be used to point to data directly or may be modified by an optional constant or register offset. During some indexed modes, the contents of the index register are incremented or decremented to point to the next item of tabular type data. All four pointer registers (X, Y, U, S) may be used as index registers.

STACK POINTER (U, S)

The Hardware Stack Pointer (S) is used automatically by the processor during subroutine calls and interrupts. The stack pointers of the MC6809 point to the top of the stack, in contrast to the MC6800 stack pointer, which pointed to the next free location on the stack. The User Stack Pointer (U) is controlled exclusively by the programmer thus allowing arguments to be passed to and from subroutines with ease. Both Stack Pointers have the same indexed mode addressing capabilities as the X and Y registers, but also support **Push** and **Pull** instructions. This allows the MC6809 to be used efficiently as a stack processor, greatly enhancing its ability to support higher level languages and modular programming.

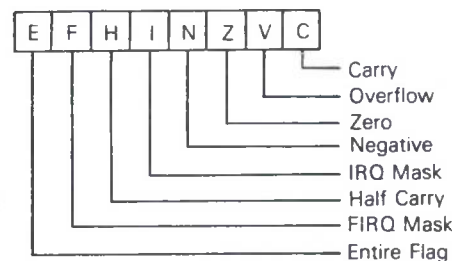
PROGRAM COUNTER

The Program Counter is used by the processor to point to the address of the next instruction to be executed by the processor. Relative Addressing is provided allowing the Program Counter to be used like an index register in some situations.

CONDITION CODE REGISTER

The Condition Code Register defines the State of the Processor at any given time. See Figure 6.

FIGURE 6 — CONDITION CODE REGISTER FORMAT



CONDITION CODE REGISTER DESCRIPTION

BIT 0 (C)

Bit 0 is the carry flag, and is usually the carry from the binary ALU. C is also used to represent a 'borrow' from subtract like instructions (CMP, NEG, SUB, SBC) and is the complement of the carry from the binary ALU.

BIT 1 (V)

Bit 1 is the overflow flag, and is set to a one by an operation which causes a signed two's complement arithmetic overflow. This overflow is detected in an operation in which the carry from the MSB in the ALU does not match the carry from the MSB-1.

BIT 2 (Z)

Bit 2 is the zero flag, and is set to a one if the result of the previous operation was identically zero.



BIT 3 (N)

Bit 3 is the negative flag, which contains exactly the value of the MSB of the result of the preceding operation. Thus, a negative two's-complement result will leave N set to a one.

BIT 4 (I)

Bit 4 is the $\overline{\text{IRQ}}$ mask bit. The processor will not recognize interrupts from the $\overline{\text{IRQ}}$ line if this bit is set to a one. $\overline{\text{NMI}}$, $\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$, $\overline{\text{RESET}}$, and SWI are set I to a one; SWI2 and SWI3 do not affect I.

BIT 5 (H)

Bit 5 is the half-carry bit, and is used to indicate a carry from bit 3 in the ALU as a result of an 8-bit addition only (ADC or ADD). This bit is used by the DAA instruction to perform a BCD decimal add adjust operation. The state of this flag is undefined in all subtract-like instructions.

BIT 6 (F)

Bit 6 is the $\overline{\text{FIRQ}}$ mask bit. The processor will not recognize interrupts from the $\overline{\text{FIRQ}}$ line if this bit is a one. $\overline{\text{NMI}}$, $\overline{\text{FIRQ}}$, SWI, and $\overline{\text{RESET}}$ all set F to a one. $\overline{\text{IRQ}}$, SWI2 and SWI3 do not affect F.

BIT 7 (E)

Bit 7 is the entire flag, and when set to a one indicates that the complete machine state (all the registers) was stacked, as opposed to the subset state (PC and CC). The E bit of the stacked CC is used on a return from interrupt (RTI) to determine the extent of the unstacking. Therefore, the current E left in the Condition Code Register represents past action.

PIN DESCRIPTIONS**POWER (V_{SS}, V_{CC})**

Two pins are used to supply power to the part: V_{SS} is ground or 0 volts, while V_{CC} is +5.0 V $\pm$ 5%.

ADDRESS BUS (A0-A15)

Sixteen pins are used to output address information from the MPU onto the Address Bus. When the processor does not require the bus for a data transfer, it will output address FFFF₁₆, $\overline{\text{R/W}} = 1$, and $\text{BS} = 0$; this is a "dummy access" or VMA cycle. Addresses are valid on the rising edge of Q (see Figure 2). All address bus drivers are made high-impedance when output Bus Available (BA) is high. Each pin will drive one Schottky TTL load or four LS TTL loads, and 90 pF.

DATA BUS (D0-D7)

These eight pins provide communication with the system bi-directional data bus. Each pin will drive one Schottky TTL load or four LS TTL loads, and 130 pF.

READ/WRITE (R/ $\overline{\text{W}}$)

This signal indicates the direction of data transfer on the data bus. A low indicates that the MPU is writing data onto the data bus. R/ $\overline{\text{W}}$ is made high impedance when BA is high. R/ $\overline{\text{W}}$ is valid on the rising edge of Q.

 $\overline{\text{RESET}}$

A low level on this Schmitt-trigger input for greater than one bus cycle will reset the MPU, as shown in Figure 7. The Reset vectors are fetched from locations FFFE₁₆ and FFFF₁₆ (Table 1) when Interrupt Acknowledge is true, ($\overline{\text{BA}} \bullet \text{BS} = 1$). During initial power-on, the $\overline{\text{RESET}}$ line should be held low until the clock oscillator is fully operational. See Figure 8.

Because the MC6809 $\overline{\text{RESET}}$ pin has a Schmitt-trigger input with a threshold voltage higher than that of standard peripherals, a simple R/C network may be used to reset the entire system. This higher threshold voltage ensures that all peripherals are out of the reset state before the Processor.

 $\overline{\text{HALT}}$

A low level on this input pin will cause the MPU to stop running at the end of the present instruction and remain halted indefinitely without loss of data. When halted, the BA output is driven high indicating the buses are high impedance. BS is also high which indicates the processor is in the Halt or Bus Grant state. While halted, the MPU will not respond to external real-time requests ($\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$) although $\overline{\text{DMA/BREQ}}$ will always be accepted, and $\overline{\text{NMI}}$ or $\overline{\text{RESET}}$ will be latched for later response. During the Halt state Q and E continue to run normally. If the MPU is not running ($\overline{\text{RESET}}$, $\overline{\text{DMA/BREQ}}$), a halted state ($\overline{\text{BA}} \bullet \text{BS} = 1$) can be achieved by pulling $\overline{\text{HALT}}$ low while $\overline{\text{RESET}}$ is still low. If $\overline{\text{DMA/BREQ}}$ and $\overline{\text{HALT}}$ are both pulled low, the processor will reach the last cycle of the instruction (by reverse cycle stealing) where the machine will then become halted. See Figure 9.

BUS AVAILABLE, BUS STATUS (BA, BS)

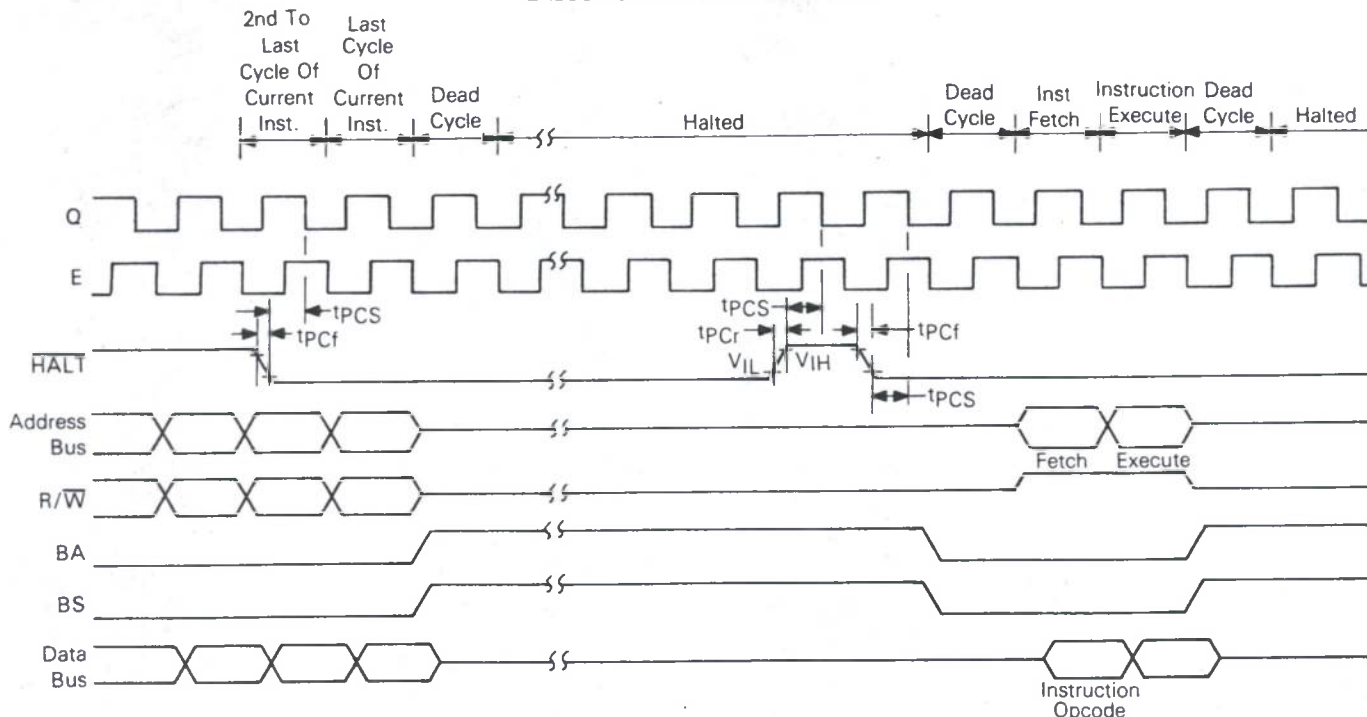
The Bus Available output is an indication of an internal control signal which makes the MOS buses of the MPU high impedance. This signal does not imply that the bus will be available for more than one cycle. When BA goes low, a dead cycle will elapse before the MPU acquires the bus.

The Bus Status output signal, when decoded with BA, represents the MPU state (valid with leading edge of Q).

MPU State		MPU State Definition
BA	BS	
0	0	Normal (Running)
0	1	Interrupt or Reset Acknowledge
1	0	Sync Acknowledge
1	1	Halt or Bus Grant Acknowledge



FIGURE 9 — HALT AND SINGLE INSTRUCTION EXECUTION FOR SYSTEM DEBUG



NOTE: Waveform measurements for all inputs and outputs are specified at logic high 2.0 V and logic low 0.8 V unless otherwise specified.

Interrupt Acknowledge is indicated during both cycles of a hardware-vector-fetch (RESET, NMI, $\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$, SWI, SWI2, SWI3). This signal, plus decoding of the lower four address lines, can provide the user with an indication of which interrupt level is being serviced and allow vectoring by device. See Table 1.

Sync Acknowledge is indicated while the MPU is waiting for external synchronization on an interrupt line.

Halt/Bus Grant is true when the MC6809 is in a Halt or Bus Grant condition.

interrupt cannot be inhibited by the program, and also has a higher priority than $\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$ or software interrupts. During recognition of an NMI, the entire machine state is saved on the hardware stack. After reset, an NMI will not be recognized until the first program load of the Hardware Stack Pointer (S). The pulse width of NMI low must be at least one E cycle. If the NMI input does not meet the minimum set up with respect to Q, the interrupt will not be recognized until the next cycle. See Figure 10.

TABLE 1: MEMORY MAP FOR INTERRUPT VECTORS

Memory Map For Vector Locations		Interrupt Vector Description
MS	LS	
FFFE	FFFF	RESET
FFFC	FFFD	NMI
FFFA	FFFB	SWI
FFF8	FFF9	$\overline{\text{IRQ}}$
FFF6	FFF7	$\overline{\text{FIRQ}}$
FFF4	FFF5	SWI2
FFF2	FFF3	SWI3
FFF0	FFF1	Reserved

NON MASKABLE INTERRUPT (NMI)*

A negative transition on this input requests that a non-maskable interrupt sequence be generated. A non-maskable

FAST-INTERRUPT REQUEST ($\overline{\text{FIRQ}}$)*

A low level on this input pin will initiate a fast interrupt sequence, provided its mask bit (F) in the CC is clear. This sequence has priority over the standard Interrupt Request ($\overline{\text{IRQ}}$), and is fast in the sense that it stacks only the contents of the condition code register and the program counter. The interrupt service routine should clear the source of the interrupt before doing an RTI. See Figure 11.

INTERRUPT REQUEST ($\overline{\text{IRQ}}$)*

A low level input on this pin will initiate an Interrupt Request sequence provided the mask bit (I) in the CC is clear. Since $\overline{\text{IRQ}}$ stacks the entire machine state it provides a slower response to interrupts than $\overline{\text{FIRQ}}$. $\overline{\text{IRQ}}$ also has a lower priority than $\overline{\text{FIRQ}}$. Again, the interrupt service routine should clear the source of the interrupt before doing an RTI. See Figure 10.

*NMI, $\overline{\text{FIRQ}}$, and $\overline{\text{IRQ}}$ requests are sampled on the falling edge of Q. One cycle is required for synchronization before these interrupts are recognized. The pending interrupt(s) will not be serviced until completion of the current instruction unless a SYNC or CWA1 condition is present. If $\overline{\text{IRQ}}$ and $\overline{\text{FIRQ}}$ do not remain low until completion of the current instruction they may not be recognized. However, NMI is latched and need only remain low for one cycle. No interrupts are recognized or latched between the falling edge of RESET and the rising edge of BS indicating RESET acknowledge.



XTAL, EXTAL

These inputs are used to connect the on-chip oscillator to an external parallel-resonant crystal. Alternately, the pin EXTAL may be used as a TTL level input for external timing by grounding XTAL. The crystal or external frequency is four times the bus frequency. See Figure 8. Proper RF layout techniques should be observed in the layout of printed circuit boards.

E, Q

E is similar to the MC6800 bus timing signal $\phi 2$; Q is a quadrature clock signal which leads E. Q has no parallel on the MC6800. Addresses from the MPU will be valid with the leading edge of Q. Data is latched on the falling edge of E. Timing for E and Q is shown in Figure 12.

MRDY*

This input control signal allows stretching of E and Q to extend data-access time. E and Q operate normally while MRDY is high. When MRDY is low, E and Q may be stretched in integral multiples of quarter ($\frac{1}{4}$) bus cycles, thus allowing interface to slow memories, as shown in Figure 13(A). During non-valid memory access ($\overline{VMA}$ cycles) MRDY has no effect on stretching E and Q; this inhibits slowing the processor during "don't care" bus accesses. MRDY may also be used to stretch clocks (for slow memory) when bus control has been transferred to an external device (through the use of $\overline{HALT}$ and $\overline{DMA/BREQ}$).

NOTE: Four of the early production mask sets (G7F, T5A, P6F, T6M) require synchronization of the MRDY input with the $4f$ clock. The synchronization necessitates an external oscillator as shown in Figure 13(B). The negative transition of the MRDY signal, normally derived from the chip select decoding, must meet the tPCS timing. With these four mask sets, MRDY's positive transition must occur with the rising edge of $4f$.

In addition, on these same mask sets, MRDY will not stretch the E and Q signals if the machine is executing either a TFR or EXG instruction during the $\overline{HALT}$ high-to-low transition. If the MPU executes a CWAI instruction, the machine pushes the internal registers onto the stack and then awaits an interrupt. During this waiting period, it is possible to place

the MPU into a Halt mode to three-state the machine, but MRDY will not stretch the clocks.

The mask set for a particular part may be determined by examining the markings on top of the part. Below the part number is a string of characters. The first two characters are the last two characters of the mask set code. If there are only four digits the part is the G7F mask set. The last four digits, the date code, show when the part was manufactured. These four digits represent year and week. For example a ceramic part marked:



is a T5A mask set made the twelfth week of 1980.

$\overline{DMA/BREQ}$ *

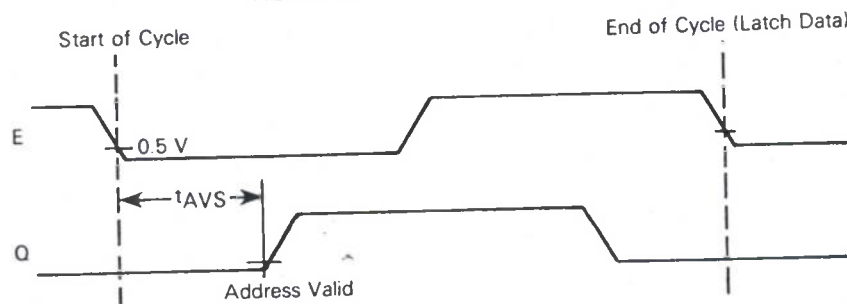
The $\overline{DMA/BREQ}$ input provides a method of suspending execution and acquiring the MPU bus for another use, as shown in Figure 14. Typical uses include DMA and dynamic memory refresh.

Transitions of $\overline{DMA/BREQ}$ should occur during Q. A low level on this pin will stop instruction execution at the end of the current cycle unless pre-empted by self-refresh. The MPU will acknowledge $\overline{DMA/BREQ}$ by setting BA and BS to a one. The requesting device will now have up to 15 bus cycles before the MPU retrieves the bus for self-refresh. Self-refresh requires one bus cycle with a leading and trailing dead cycle. See Figure 15. The self-refresh counter is only cleared if $\overline{DMA/BREQ}$ is inactive for two or more MPU cycles.

Typically, the DMA controller will request to use the bus by asserting $\overline{DMA/BREQ}$ pin low on the leading edge of E. When the MPU replies by setting BA and BS to a one, that cycle will be a dead cycle used to transfer bus mastership to the DMA controller.

False memory accesses may be prevented during any dead cycles by developing a system $\overline{DMAVMA}$ signal which is LOW in any cycle when BA has changed.

FIGURE 12 — E/Q RELATIONSHIP



NOTE: Waveform measurements for all inputs and outputs are specified at logic high 2.0 V and logic low 0.8 V unless otherwise specified.

*The on-board clock generator furnishes E and Q to both the system and the MPU. When MRDY is pulled low, both the system clocks and the internal MPU clocks are stretched. Assertion of $\overline{DMA/BREQ}$ input stops the internal MPU clocks while allowing the external system clocks to RUN (i.e., release the bus to a DMA controller). The internal MPU clocks resume operation after $\overline{DMA/BREQ}$ is released or after 16 bus cycles (14 DMA, 2 dead), whichever occurs first. While $\overline{DMA/BREQ}$ is asserted it is sometimes necessary to pull MRDY low to allow DMA to/from slow memory/peripherals. As both MRDY and $\overline{DMA/BREQ}$ control the internal MPU clocks, care must be exercised not to violate the maximum t_{cyc} specification for MRDY or $\overline{DMA/BREQ}$. (See Note 5 in Bus Timing.)



**MOTOROLA****SEMICONDUCTORS**

3501 ED BLUESTEIN BLVD. AUSTIN, TEXAS 78721

8-BIT MICROPROCESSING UNIT

The MC6809E is a revolutionary high performance 8-bit microprocessor which supports modern programming techniques such as position independence, reentrancy, and modular programming.

This third-generation addition to the M6800 family has major architectural improvements which include additional registers, instructions and addressing modes.

The basic instructions of any computer are greatly enhanced by the presence of powerful addressing modes. The MC6809E has the most complete set of addressing modes available on any 8-bit microprocessor today.

The MC6809E has hardware and software features which make it an ideal processor for higher level language execution or standard controller applications. External clock inputs are provided to allow synchronization with peripherals, systems or other MPUs.

MC6800 COMPATIBLE

- Hardware — Interfaces with All M6800 Peripherals
- Software — Upward Source Code Compatible Instruction Set and Addressing Modes

ARCHITECTURAL FEATURES

- Two 16-bit Index Registers
- Two 16-bit Indexable Stack Pointers
- Two 8-bit Accumulators can be Concatenated to Form One 16-Bit Accumulator
- Direct Page Register Allows Direct Addressing Throughout Memory

HARDWARE FEATURES

- External Clock Inputs, E and Q, Allow Synchronization
- TSC Input Controls Internal Bus Buffers
- LIC Indicates Opcode Fetch
- AVMA Allows Efficient Use of Common Resources in A Multiprocessor System
- BUSY is a Status Line for Multiprocessing
- Fast Interrupt Request Input Stacks Only Condition Code Register and Program Counter
- Interrupt Acknowledge Output Allows Vectoring By Devices
- SYNC Acknowledge Output Allows for Synchronization to External Event
- Single Bus-Cycle $\overline{\text{RESET}}$
- Single 5-Volt Supply Operation
- NMI Inhibited After $\overline{\text{RESET}}$ Until After First Load of Stack Pointer
- Early Address Valid Allows Use With Slower Memories
- Early Write-Data for Dynamic Memories

SOFTWARE FEATURES

- 10 Addressing Modes
 - M6800 Upward Compatible Addressing Modes
 - Direct Addressing Anywhere in Memory Map
 - Long Relative Branches
 - Program Counter Relative
 - True Indirect Addressing
 - Expanded Indexed Addressing:
 - 0, 5, 8, or 16-bit Constant Offsets
 - 8, or 16-bit Accumulator Offsets
 - Auto-Increment/Decrement by 1 or 2
- Improved Stack Manipulation
- 1464 Instruction with Unique Addressing Modes
- 8×8 Unsigned Multiply
- 16-bit Arithmetic
- Transfer/Exchange All Registers
- Push/Pull Any Registers or Any Set of Registers
- Load Effective Address

MC6809E

(1.0 MHz)

MC68A09E

(1.5 MHz)

MC68B09E

(2.0 MHz)

HMOS

(HIGH-DENSITY N-CHANNEL, SILICON-GATE)

**8-BIT
MICROPROCESSING
UNIT**

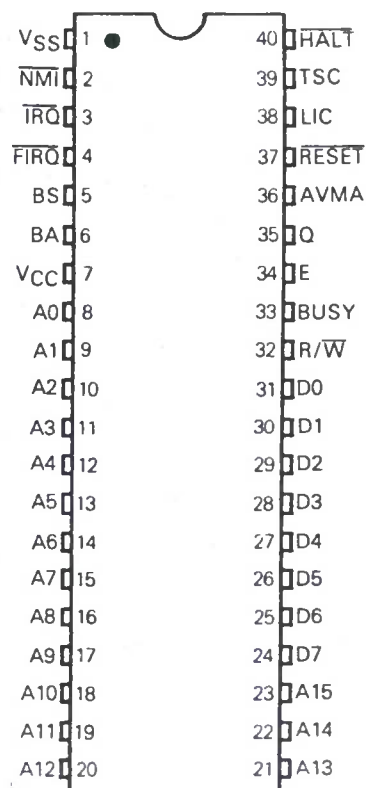
L SUFFIX
CERAMIC PACKAGE
CASE 715



P SUFFIX
PLASTIC PACKAGE
CASE 711



S SUFFIX
CERDIP PACKAGE
CASE 734

FIGURE 1 — PIN ASSIGNMENT

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.3 to +7.0	V
Input Voltage	V _{in}	-0.3 to +7.0	V
Operating Temperature Range MC6809E, MC68A09E, MC68B09E	T _A	T _L to T _H 0 to +70	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance			
Ceramic	θ_{JA}	50	°C/W
Cerdip		60	
Plastic		100	

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D = P_{INT} + P_{PORT}

P_{INT} = I_{CC} × V_{CC}, Watts — Chip Internal Power

P_{PORT} = Port Power Dissipation, Watts — User Determined

For most applications P_{PORT} < P_{INT} and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K + (T_J + 273^\circ\text{C}) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \cdot (T_A + 273^\circ\text{C}) + \theta_{JA} \cdot P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_A = T_L to T_H unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	Logic, Q, RESET V _{IH} V _{IHR} V _{IHC}	V _{SS} + 2.0 V _{SS} + 4.0 V _{CC} - 0.75	— — —	V _{CC} V _{CC} V _{CC} + 0.3	V
Input Low Voltage	Logic, Q, RESET V _{IL} V _{ILC}	V _{SS} - 0.3 V _{SS} - 0.3	— —	V _{SS} + 0.8 V _{SS} + 0.4	V
Input Leakage Current (V _{in} = 0 to 5.25 V, V _{CC} = max)	Logic, Q, RESET I _{in} E	— —	— —	2.5 100	μA
DC Output High Voltage (I _{Load} = -205 μA, V _{CC} = min) (I _{Load} = -145 μA, V _{CC} = min) (I _{Load} = -100 μA, V _{CC} = min)	D0-D7 A0-A15, R/W BA, BS, LIC, AVMA, BUSY	V _{OH} V _{OH} V _{OH}	— — —	— — —	V
DC Output Low Voltage (I _{Load} = 2.0 mA, V _{CC} = min)	V _{OL}	—	—	V _{SS} + 0.5	V
Internal Power Dissipation (Measured at T _A = T _L in Steady State Operation)	P _{INT}	—	—	1.0	W
Capacitance* (V _{in} = 0, T _A = 25°C, f = 1.0 MHz)	C _{in}	— —	10 30	15 50	pF
	C _{out}	—	10	15	pF
Frequency of Operation (E and Q Inputs)	MC6809E MC68A09E MC68B09E	0.1 0.1 0.1	— — —	1.0 1.5 2.0	MHz
Three-State (Off State) Input Current (V _{in} = 0.4 to 2.4 V, V _{CC} = max)	D0-D7 A0-A15, R/W	— —	2.0 —	10 100	μA

*Capacitances are periodically tested rather than 100% tested.

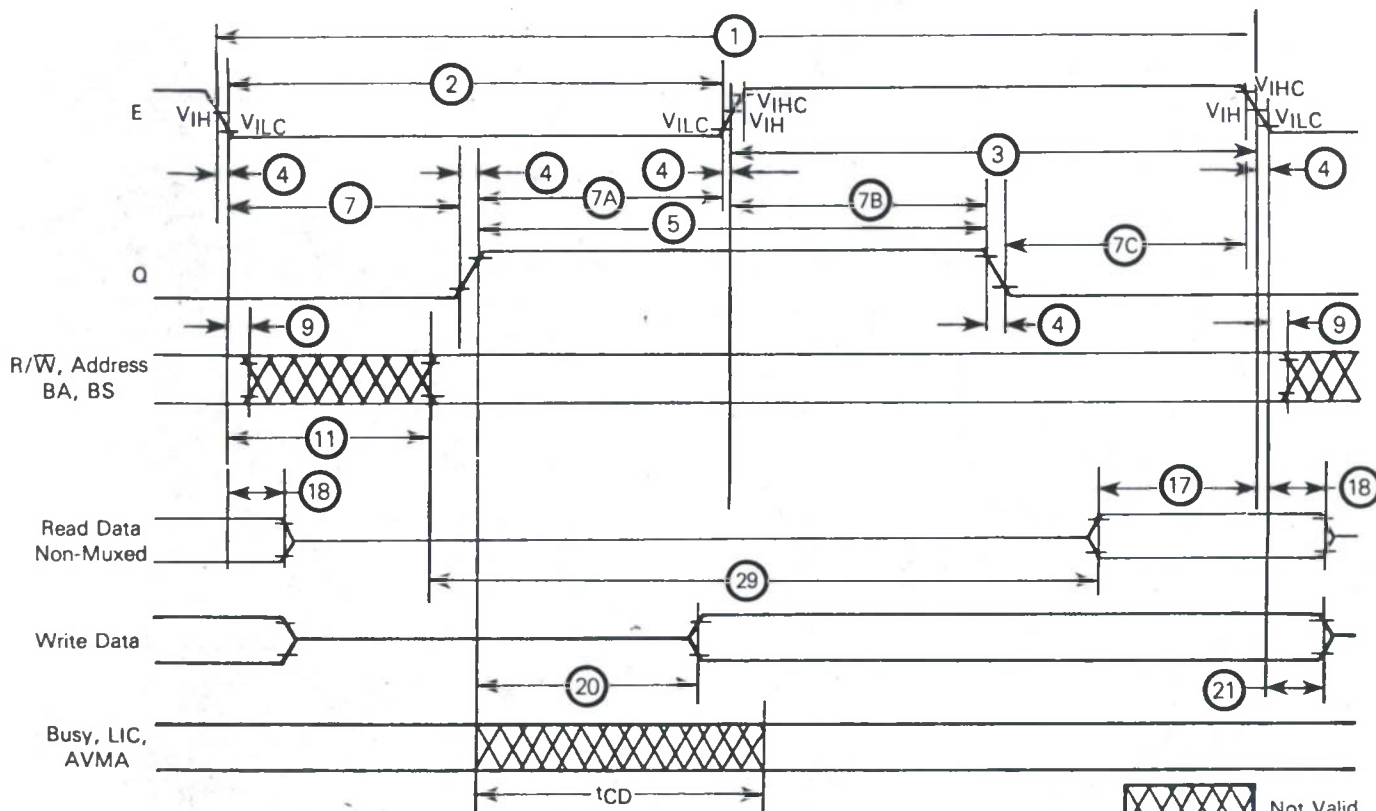


MOTOROLA Semiconductor Products Inc.

BUS TIMING CHARACTERISTICS (See Notes 1, 2, 3, and 4)

Ident. Number	Characteristics	Symbol	MC6809E		MC68A09E		MC68B09E		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1.0	10	0.667	10	0.5	10	μs
2	Pulse Width, E Low	PW_{EL}	450	9500	295	9500	210	9500	ns
3	Pulse Width, E High	PW_{EH}	450	9500	280	9500	220	9500	ns
4	Clock Rise and Fall Time	t_r, t_f	—	25	—	25	—	20	ns
5	Pulse Width, Q High	PW_{QH}	450	9500	280	9500	220	9500	ns
7	Delay Time, E to Q Rise	t_{EQ1}	200	—	130	—	100	—	ns
7A	Delay Time, Q High to E Rise	t_{EQ2}	200	—	130	—	100	—	ns
7B	Delay Time, E High to Q Fall	t_{EQ3}	200	—	130	—	100	—	ns
7C	Delay Time, Q High to E Fall	t_{EQ4}	200	—	130	—	100	—	ns
9	Address Hold Time	t_{AH}	20	—	20	—	20	—	ns
11	Address Delay Time from E Low (BA, BS, R/W)	t_{AD}	—	200	—	140	—	110	ns
17	Read Data Setup Time	t_{DSR}	80	—	60	—	40	—	ns
18	Read Data Hold Time	t_{DHR}	10	—	10	—	10	—	ns
20	Data Delay Time from Q	t_{DDQ}	—	200	—	140	—	110	ns
21	Write Data Hold Time	t_{DHW}	30	—	30	—	30	—	ns
29	Usable Access Time	t_{ACC}	695	—	440	—	330	—	ns
	Control Delay Time (Figure 2)	t_{CD}	—	300	—	250	—	200	ns
	Interrupts, $\overline{HALT}$, $\overline{RESET}$, and TSC Setup Time (Figures 7, 8, 9, 10, 13, and 14)	t_{PCS}	200	—	140	—	110	—	ns
	TSC Drive to Valid Logic Level (Figure 14)	t_{TSV}	—	210	—	150	—	120	ns
	TSC Release MOS Buffers to High Impedance (Figure 14)	t_{TSR}	—	200	—	140	—	110	ns
	TSC Three-State Delay Time (Figure 14)	t_{TSC}	—	120	—	85	—	80	ns
	Processor Control Rise and Fall Time (Figure 8)	t_{PCr}, t_{PCf}	—	100	—	100	—	100	ns

FIGURE 2 — READ/WRITE DATA TO MEMORY OR PERIPHERALS



NOTES:

1. Voltage levels shown are $V_L \leq 0.4 V$, $V_{IH} \geq 2.4 V$, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.
3. Hold time (⑨) for BA and BS is not specified.
4. Usable access time is computed by: 1 - 4 - 11 max - 17.



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FIGURE 3 — MC6809E EXPANDED BLOCK DIAGRAM

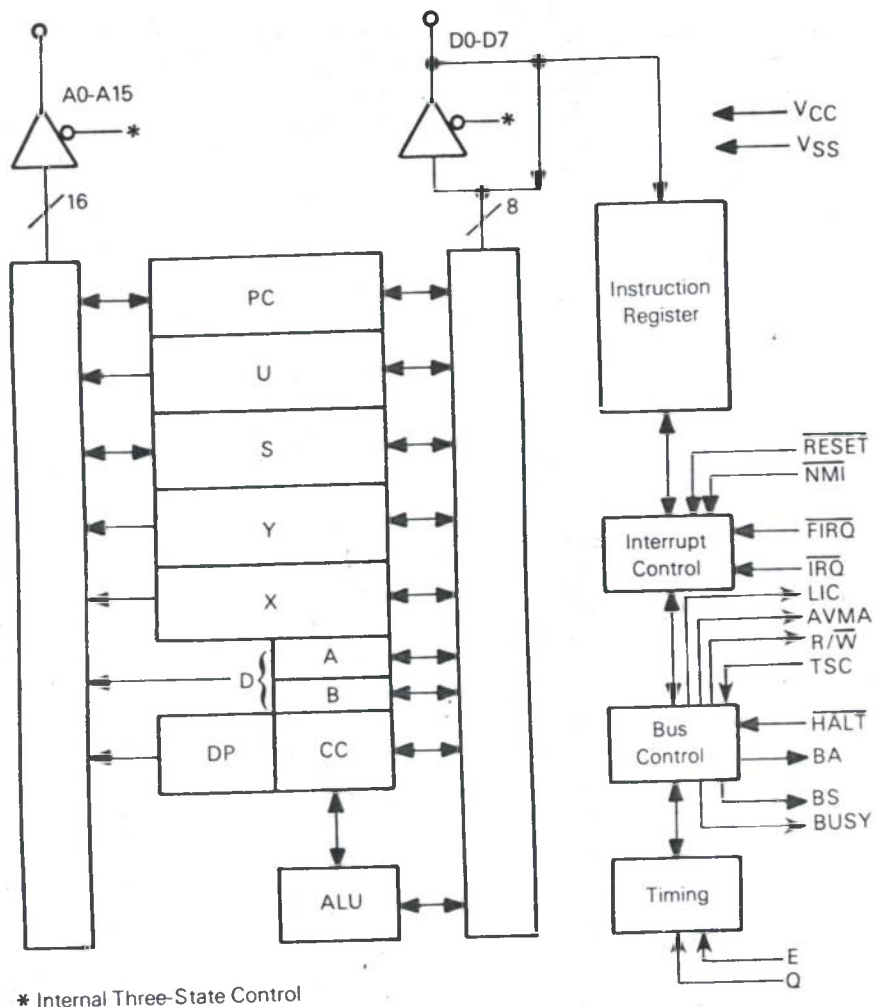
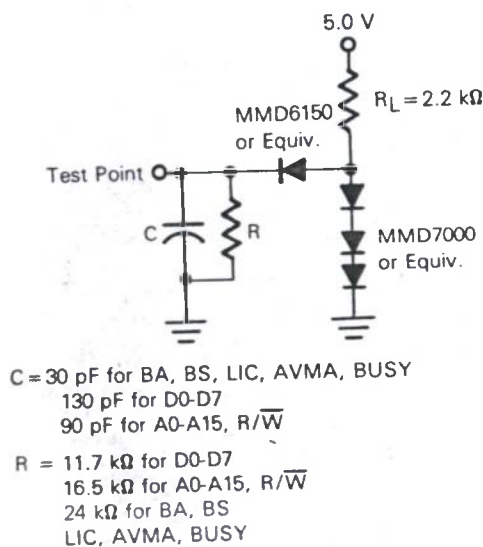


FIGURE 4 — BUS TIMING TEST LOAD



PROGRAMMING MODEL

As shown in Figure 5, the MC6809E adds three registers to the set available in the MC6800. The added registers include a Direct Page Register, the User Stack pointer and a second Index Register.

ACCUMULATORS (A, B, D)

The A and B registers are general purpose accumulators which are used for arithmetic calculations and manipulation of data.

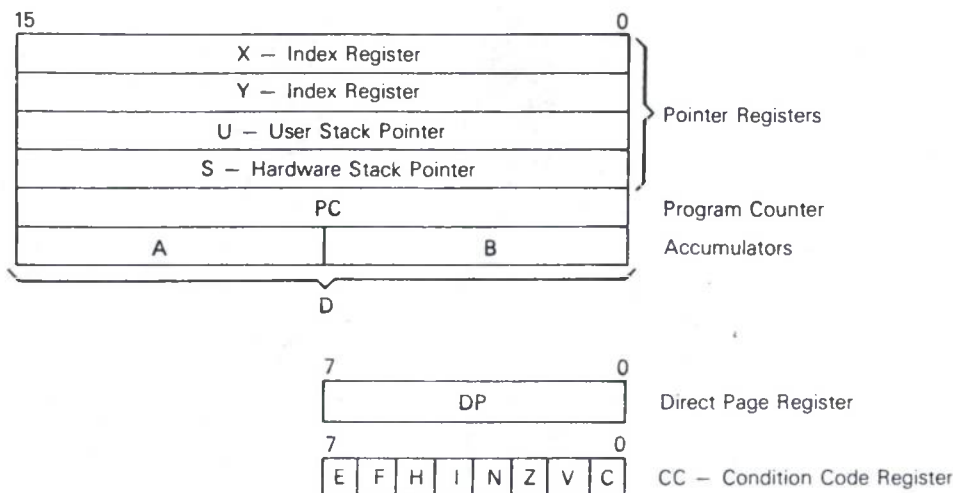
Certain instructions concatenate the A and B registers to form a single 16-bit accumulator. This is referred to as the D Register, and is formed with the A Register as the most significant byte.

DIRECT PAGE REGISTER (DP)

The Direct Page Register of the MC6809E serves to enhance the Direct Addressing Mode. The content of this register appears at the higher address outputs (A8-A15) during direct addressing instruction execution. This allows the direct mode to be used at any place in memory, under program control. To ensure M6800 compatibility, all bits of this register are cleared during Processor Reset.



FIGURE 5 — PROGRAMMING MODEL OF THE MICROPROCESSING UNIT



INDEX REGISTERS (X, Y)

The Index Registers are used in indexed mode of addressing. The 16-bit address in this register takes part in the calculation of effective addresses. This address may be used to point to data directly or may be modified by an optional constant or register offset. During some indexed modes, the contents of the index register are incremented and decremented to point to the next item of tabular type data. All four pointer registers (X, Y, U, S) may be used as index registers.

STACK POINTER (U, S)

The Hardware Stack Pointer (S) is used automatically by the processor during subroutine calls and interrupts. The User Stack Pointer (U) is controlled exclusively by the programmer thus allowing arguments to be passed to and from subroutines with ease. The U-register is frequently used as a stack marker. Both Stack Pointers have the same indexed mode addressing capabilities as the X and Y registers, but also support **Push** and **Pull** instructions. This allows the MC6809E to be used efficiently as a stack processor, greatly enhancing its ability to support higher level languages and modular programming.

NOTE

The stack pointers of the MC6809E point to the top of the stack, in contrast to the MC6800 stack pointer, which pointed to the next free location on stack.

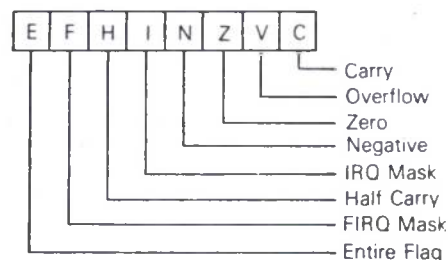
PROGRAM COUNTER

The Program Counter is used by the processor to point to the address of the next instruction to be executed by the processor. Relative Addressing is provided allowing the Program Counter to be used like an index register in some situations.

CONDITION CODE REGISTER

The Condition Code Register defines the state of the processor at any given time. See Figure 6.

FIGURE 6 — CONDITION CODE REGISTER FORMAT



CONDITION CODE REGISTER DESCRIPTION

BIT 0 (C)

Bit 0 is the carry flag, and is usually the carry from the binary ALU. C is also used to represent a 'borrow' from subtract like instructions (CMP, NEG, SUB, SBC) and is the complement of the carry from the binary ALU.

BIT 1 (V)

Bit 1 is the overflow flag, and is set to a one by an operation which causes a signed two's complement arithmetic overflow. This overflow is detected in an operation in which the carry from the MSB in the ALU does not match the carry from the MSB-1.

BIT 2 (Z)

Bit 2 is the zero flag, and is set to a one if the result of the previous operation was identically zero.



BIT 3 (N)

Bit 3 is the negative flag, which contains exactly the value of the MSB of the result of the preceding operation. Thus, a negative two's-complement result will leave N set to a one.

BIT 4 (I)

Bit 4 is the $\overline{\text{IRQ}}$ mask bit. The processor will not recognize interrupts from the $\overline{\text{IRQ}}$ line if this bit is set to a one. $\overline{\text{NMI}}$, $\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$, $\overline{\text{RESET}}$, and $\overline{\text{SWI}}$ all set I to a one; $\overline{\text{SWI2}}$ and $\overline{\text{SWI3}}$ do not affect I.

BIT 5 (H)

Bit 5 is the half-carry bit, and is used to indicate a carry from bit 3 in the ALU as a result of an 8-bit addition only (ADC or ADD). This bit is used by the DAA instruction to perform a BCD decimal add adjust operation. The state of this flag is undefined in all subtract-like instructions.

BIT 6 (F)

Bit 6 is the $\overline{\text{FIRQ}}$ mask bit. The processor will not recognize interrupts from the $\overline{\text{FIRQ}}$ line if this bit is a one. $\overline{\text{NMI}}$, $\overline{\text{FIRQ}}$, $\overline{\text{SWI}}$, and $\overline{\text{RESET}}$ all set F to a one. $\overline{\text{IRQ}}$, $\overline{\text{SWI2}}$ and $\overline{\text{SWI3}}$ do not affect F.

BIT 7 (E)

Bit 7 is the entire flag, and when set to a one indicates that the complete machine state (all the registers) was stacked, as opposed to the subset state (PC and CC). The E bit of the stacked CC is used on a return from interrupt (RTI) to determine the extent of the unstacking. Therefore, the current E left in the Condition Code Register represents past action.

PIN DESCRIPTIONS**POWER (V_{SS}, V_{CC})**

Two pins are used to supply power to the part: V_{SS} is ground or 0 volts, while V_{CC} is +5.0 V $\pm$ 5%.

ADDRESS BUS (A0-A15)

Sixteen pins are used to output address information from the MPU onto the Address Bus. When the processor does not require the bus for a data transfer, it will output address FFFF₁₆, R/ $\overline{\text{W}}$ = 1, and BS = 0; this is a "dummy access" or VMA cycle. All address bus drivers are made high-impedance when output Bus Available (BA) is high or when TSC is asserted. Each pin will drive one Schottky TTL load or four LS TTL loads, and 90 pF. Refer to Figures 1 and 2.

DATA BUS (D0-D7)

These eight pins provide communication with the system bi-directional data bus. Each pin will drive one Schottky TTL load or four LS TTL loads, and 130 pF.

READ/WRITE (R/ $\overline{\text{W}}$)

This signal indicates the direction of data transfer on the data bus. A low indicates that the MPU is writing data onto the data bus. R/ $\overline{\text{W}}$ is made high impedance when BA is high or when TSC is asserted. Refer to Figures 1 and 2.

RESET

A low level on this Schmitt-trigger input for greater than one bus cycle will reset the MPU, as shown in Figure 7. The

Reset vectors are fetched from locations FFFE₁₆ and FFFF₁₆ (Table 1) when Interrupt Acknowledge is true, ($\overline{\text{BA}} \bullet \text{BS} = 1$). During initial power-on, the Reset line should be held low until the clock input signals are fully operational.

Because the MC6809E Reset pin has a Schmitt-trigger input with a threshold voltage higher than that of standard peripherals, a simple R/C network may be used to reset the entire system. This higher threshold voltage ensures that all peripherals are out of the reset state before the Processor.

HALT

A low level on this input pin will cause the MPU to stop running at the end of the present instruction and remain halted indefinitely without loss of data. When halted, the BA output is driven high indicating the buses are high impedance. BS is also high which indicates the processor is in the Halt state. While halted, the MPU will not respond to external real-time requests ($\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$) although $\overline{\text{NMI}}$ or $\overline{\text{RESET}}$ will be latched for later response. During the Halt state Q and E should continue to run normally. A halted state ($\overline{\text{BA}} \bullet \text{BS} = 1$) can be achieved by pulling HALT low while $\overline{\text{RESET}}$ is still low. See Figure 8.

BUS AVAILABLE, BUS STATUS (BA, BS)

The Bus Available output is an indication of an internal control signal which makes the MOS buses of the MPU high impedance. When BA goes low, a dead cycle will elapse before the MPU acquires the bus. BA will not be asserted when TSC is active, thus allowing dead cycle consistency.

The Bus Status output signal, when decoded with BA, represents the MPU state (valid with leading edge of Q).

MPU State		MPU State Definition
BA	BS	
0	0	Normal (Running)
0	1	Interrupt or RESET Acknowledge
1	0	SYNC Acknowledge
1	1	HALT Acknowledge

Interrupt Acknowledge is indicated during both cycles of a hardware-vector-fetch ($\overline{\text{RESET}}$, $\overline{\text{NMI}}$, $\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$, $\overline{\text{SWI}}$, $\overline{\text{SWI2}}$, $\overline{\text{SWI3}}$). This signal, plus decoding of the lower four address lines, can provide the user with an indication of which interrupt level is being serviced and allow vectoring by device. See Table 1.

TABLE 1 — MEMORY MAP FOR INTERRUPT VECTORS

Memory Map For Vector Locations		Interrupt Vector Description
MS	LS	
FFFE	FFFF	$\overline{\text{RESET}}$
FFFC	FFFD	$\overline{\text{NMI}}$
FFFA	FFFB	$\overline{\text{SWI}}$
FFF8	FFF9	$\overline{\text{IRQ}}$
FFF6	FFF7	$\overline{\text{FIRQ}}$
FFF4	FFF5	$\overline{\text{SWI2}}$
FFF2	FFF3	$\overline{\text{SWI3}}$
FFF0	FFF1	Reserved



Sync Acknowledge is indicated while the MPU is waiting for external synchronization on an interrupt line.

Halt/Acknowledge is indicated when the MC6809E is in a Halt condition.

NON MASKABLE INTERRUPT (NMI)*

A negative transition on this input requests that a non-maskable interrupt sequence be generated. A non-maskable interrupt cannot be inhibited by the program, and also has a higher priority than $\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$ or software interrupts. During recognition of an NMI, the entire machine state is saved on the hardware stack. After reset, an NMI will not be recognized until the first program load of the Hardware Stack Pointer (S). The pulse width of $\overline{\text{NMI}}$ low must be at least one E cycle. If the $\overline{\text{NMI}}$ input does not meet the minimum set up with respect to Q, the interrupt will not be recognized until the next cycle. See Figure 9.

FAST-INTERRUPT REQUEST ($\overline{\text{FIRQ}}$)*

A low level on this input pin will initiate a fast interrupt sequence, provided its mask bit (F) in the CC is clear. This sequence has priority over the standard Interrupt Request ($\overline{\text{IRQ}}$), and is fast in the sense that it stacks only the contents of the condition code register and the program counter. The interrupt service routine should clear the source of the interrupt before doing an RTI. See Figure 10.

INTERRUPT REQUEST ($\overline{\text{IRQ}}$)*

A low level input on this pin will initiate an Interrupt Request sequence provided the mask bit (I) in the CC is clear. Since $\overline{\text{IRQ}}$ stacks the entire machine state it provides a slower response to interrupts than $\overline{\text{FIRQ}}$. $\overline{\text{IRQ}}$ also has a lower priority than $\overline{\text{FIRQ}}$. Again, the interrupt service routine should clear the source of the interrupt before doing an RTI. See Figure 9.

CLOCK INPUTS E, Q

E and Q are the clock signals required by the MC6809E. Q must lead E; that is, a transition on Q must be followed by a similar transition on E after a minimum delay. Addresses will be valid from the MPU, t_{AD} after the falling edge of E, and data will be latched from the bus by the falling edge of E. While the Q input is fully TTL compatible, the E input directly drives internal MOS circuitry and, thus, requires a high level above normal TTL levels. This approach minimizes clock skew inherent with an internal buffer. Timing and waveforms for E and Q are shown in Figure 2 while Figure 11 shows a simple clock generator for the MC6809E.

BUSY

Busy will be high for the read and modify cycles of a read-modify-write instruction and during the access of the first byte of a double-byte operation (e.g., LDX, STD, ADDD). Busy is also high during the first byte of any indirect or other vector fetch (e.g., jump extended, SWI indirect etc.).

In a multi-processor system, busy indicates the need to

defer the re-arbitration of the next bus cycle to insure the integrity of the above operations. This difference provides the indivisible memory access required for a "test-and-set" primitive, using any one of several read-modify-write instructions.

Busy does not become active during PSH or PUL operations. A typical read-modify-write instruction (ASL) is shown in Figure 12. Timing information is given in Figure 13. Busy is valid t_{CD} after the rising edge of Q.

AVMA

AVMA is the Advanced VMA signal and indicates that the MPU will use the bus in the following bus cycle. The predictive nature of the AVMA signal allows efficient shared-bus multiprocessor systems. AVMA is LOW when the MPU is in either a HALT or SYNC state. AVMA is valid t_{CD} after the rising edge of Q.

LIC

LIC (Last Instruction Cycle) is HIGH during the last cycle of every instruction, and its transition from HIGH to LOW will indicate that the first byte of an opcode will be latched at the end of the present bus cycle. LIC will be HIGH when the MPU is Halted at the end of an instruction, (i.e., not in CWA1 or RESET) in SYNC state or while stacking during interrupts. LIC is valid t_{CD} after the rising edge of Q.

TSC

TSC (Three-State Control) will cause MOS address, data, and R/W buffers to assume a high-impedance state. The control signals (BA, BS, BUSY, AVMA and LIC) will not go to the high-impedance state. TSC is intended to allow a single bus to be shared with other bus masters (processors or DMA controllers).

While E is low, TSC controls the address buffers and $R/\overline{W}$ directly. The data bus buffers during a write operation are in a high-impedance state until Q rises at which time, if TSC is true, they will remain in a high-impedance state. If TSC is held beyond the rising edge of E, then it will be internally latched, keeping the bus drivers in a high-impedance state for the remainder of the bus cycle. See Figure 14.

MPU OPERATION

During normal operation, the MPU fetches an instruction from memory and then executes the requested function. This sequence begins after $\overline{\text{RESET}}$ and is repeated indefinitely unless altered by a special instruction or hardware occurrence. Software instructions that alter normal MPU operation are: SWI, SWI2, SWI3, CWA1, RTI and SYNC. An interrupt or HALT input can also alter the normal execution of instructions. Figure 15 is the flow chart for the MC6809E.

*NMI, $\overline{\text{FIRQ}}$, and $\overline{\text{IRQ}}$ requests are sampled on the falling edge of Q. One cycle is required for synchronization before these interrupts are recognized. The pending interrupt(s) will not be serviced until completion of the current instruction unless a SYNC or CWA1 condition is present. If $\overline{\text{IRQ}}$ and $\overline{\text{FIRQ}}$ do not remain low until completion of the current instruction they may not be recognized. However, NMI is latched and need only remain low for one cycle. No interrupts are recognized or latched between the falling edge of $\overline{\text{RESET}}$ and the rising edge of BS indicating $\overline{\text{RESET}}$ acknowledge. See $\overline{\text{RESET}}$ sequence in the MPU flowchart in Figure 15.





MOTOROLA

PERIPHERAL INTERFACE ADAPTER (PIA)

The MC6821 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the M6800 family of microprocessors. This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines; Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance Three-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Drive Capability on Side A Peripheral Lines
- Two TTL Drive Capability on All A and B Side Buffers
- TTL-Compatible
- Static Operation

MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.3 to +7.0	V
Input Voltage	V _{in}	-0.3 to +7.0	V
Operating Temperature Range MC6821, MC68A21, MC68B21 MC6821C, MC68A21C, MC68B21C	T _A	T _L to T _H 0 to 70 -40 to +85	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance			
Ceramic	θ _{JA}	50	°C/W
Plastic		100	
Cerdip		60	

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage (i.e., either V_{SS} or V_{CC}).

MC6821

(1.0 MHz)

MC68A21

(1.5 MHz)

MC68B21

(2.0 MHz)

MOS

(N-CHANNEL, SILICON-GATE,
DEPLETION LOAD)

PERIPHERAL INTERFACE ADAPTER



L SUFFIX
CERAMIC PACKAGE
CASE 715



S SUFFIX
CERDIP PACKAGE
CASE 734



P SUFFIX
PLASTIC PACKAGE
CASE 711

PIN ASSIGNMENT

V _{SS}	1	40	CA1
PA0	2	39	CA2
PA1	3	38	IRQA
PA2	4	37	IRQB
PA3	5	36	RS0
PA4	6	35	RS1
PA5	7	34	RESET
PA6	8	33	D0
PA7	9	32	D1
PB0	10	31	D2
PB1	11	30	D3
PB2	12	29	D4
PB3	13	28	D5
PB4	14	27	D6
PB5	15	26	D7
PB6	16	25	E
PB7	17	24	CS1
CB1	18	23	CS2
CB2	19	22	CS0
V _{CC}	20	21	R/W

POWER CONSIDERATIONS

The average chip-junction temperature, T_J , in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

P_{PORT} = Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K + (T_J + 273^\circ\text{C}) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \cdot (T_A + 273^\circ\text{C}) + \theta_{JA} \cdot P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A .

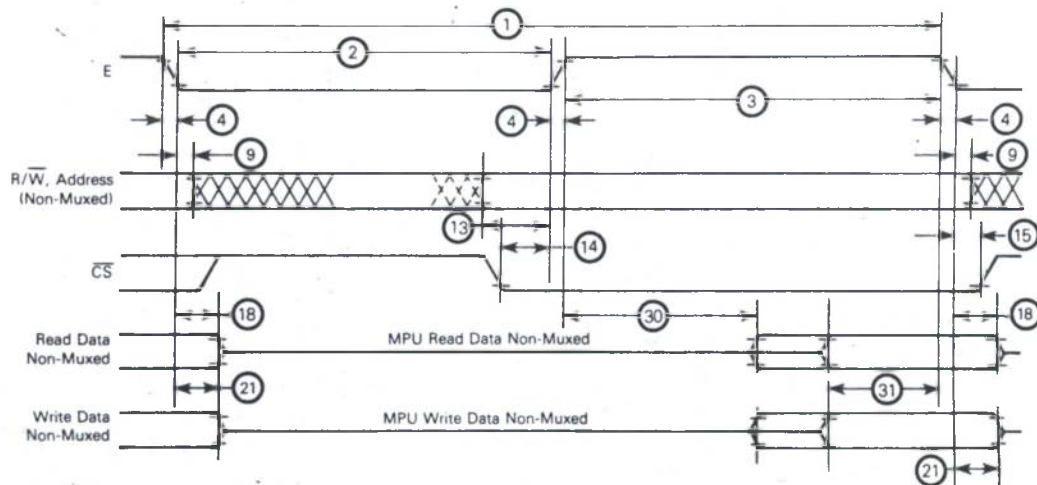
DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ Vdc} \pm 5\%$, $V_{SS} = 0$, $T_A = T_L$ to T_H unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit	
BUS CONTROL INPUTS (R/W, Enable, RESET, RS0, RS1, CS0, CS1, CS2)						
Input High Voltage	V_{IH}	$V_{SS} + 2.0$	—	V_{CC}	V	
Input Low Voltage	V_{IL}	$V_{SS} - 0.3$	—	$V_{SS} + 0.8$	V	
Input Leakage Current ($V_{in} = 0$ to 5.25 V)	I_{in}	—	1.0	2.5	μA	
Capacitance ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)	C_{in}	—	—	7.5	pF	
INTERRUPT OUTPUTS (IRQA, IRQB)						
Output Low Voltage ($I_{Load} = 3.2\text{ mA}$)	V_{OL}	—	—	$V_{SS} + 0.4$	V	
Three-State Output Leakage Current	I_{OZ}	—	1.0	10	μA	
Capacitance ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)	C_{out}	—	—	5.0	pF	
DATA BUS (D0-D7)						
Input High Voltage	V_{IH}	$V_{SS} + 2.0$	—	V_{CC}	V	
Input Low Voltage	V_{IL}	$V_{SS} - 0.3$	—	$V_{SS} + 0.8$	V	
Three-State Input Leakage Current ($V_{in} = 0.4$ to 2.4 V)	I_{IZ}	—	2.0	10	μA	
Output High Voltage ($I_{Load} = -205\text{ }\mu\text{A}$)	V_{OH}	$V_{SS} + 2.4$	—	—	V	
Output Low Voltage ($I_{Load} = 1.6\text{ mA}$)	V_{OL}	—	—	$V_{SS} + 0.4$	V	
Capacitance ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)	C_{in}	—	—	12.5	pF	
PERIPHERAL BUS (PA0-PA7, PB0-PB7, CA1, CA2, CB1, CB2)						
Input Leakage Current ($V_{in} = 0$ to 5.25 V)	R/W, RESET, RS0, RS1, CS0, CS1, CS2, CA1, CB1, Enable	I_{in}	—	1.0	2.5	μA
Three-State Input Leakage Current ($V_{in} = 0.4$ to 2.4 V)	PB0-PB7, CB2	I_{IZ}	—	2.0	10	μA
Input High Current ($V_{IH} = 2.4\text{ V}$)	PA0-PA7, CA2	I_{IH}	-200	-400	—	μA
Darlington Drive Current ($V_O = 1.5\text{ V}$)	PR0-PB7, CB2	I_{OH}	-1.0	—	-10	mA
Input Low Current ($V_{IL} = 0.4\text{ V}$)	PA0-PA7, CA2	I_{IL}	—	-1.3	-2.4	mA
Output High Voltage ($I_{Load} = -200\text{ }\mu\text{A}$) ($I_{Load} = -10\text{ }\mu\text{A}$)	PA0-PA7, PB0-PB7, CA2, CB2 PA0-PA7, CA2	V_{OH}	$V_{SS} + 2.4$ $V_{CC} - 1.0$	— —	— —	V
Output Low Voltage ($I_{Load} = 3.2\text{ mA}$)		V_{OL}	—	—	$V_{SS} + 0.4$	V
Capacitance ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)		C_{in}	—	—	10	pF
POWER REQUIREMENTS						
Internal Power Dissipation (Measured at $T_A = T_L$)	P_{INT}	—	—	550	mW	

BUS TIMING CHARACTERISTICS (See Notes 1 and 2)

Ident. Number	Characteristic	Symbol	MC6821		MC68A21		MC68B21		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1.0	10	0.67	10	0.5	10	μs
2	Pulse Width, E Low	PW_{EL}	430	—	280	—	210	—	ns
3	Pulse Width, E High	PW_{EH}	450	—	280	—	220	—	ns
4	Clock Rise and Fall Time	t_r, t_f	—	25	—	25	—	20	ns
9	Address Hold Time	t_{AH}	10	—	10	—	10	—	ns
13	Address Setup Time Before E	t_{AS}	80	—	60	—	40	—	ns
14	Chip Select Setup Time Before E	t_{CS}	80	—	60	—	40	—	ns
15	Chip Select Hold Time	t_{CH}	10	—	10	—	10	—	ns
18	Read Data Hold Time	t_{DHR}	20	100	20	100	20	100	ns
21	Write Data Hold Time	t_{DHW}	10	—	10	—	10	—	ms
30	Output Data Delay Time	t_{DDR}	—	290	—	180	—	150	ns
31	Input Data Setup Time	t_{DSW}	165	—	80	—	60	—	ns

FIGURE 1 — BUS TIMING



Notes:

1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

PERIPHERAL TIMING CHARACTERISTICS ($V_{CC}=5.0\text{ V} \pm 5\%$, $V_{SS}=0\text{ V}$, $T_A=T_L$ to T_H unless otherwise specified)

Characteristic	Symbol	MC6821		MC68A21		MC68B21		Unit	Reference Fig. No.
		Min	Max	Min	Max	Min	Max		
Data Setup Time	t_{PDS}	200	—	135	—	100	—	ns	6
Data Hold Time	t_{PDH}	0	—	0	—	0	—	ns	6
Delay Time, Enable Negative Transition to CA2 Negative Transition	t_{CA2}	—	1.0	—	0.670	—	0.500	μs	3, 7, 8
Delay Time, Enable Negative Transition to CA2 Positive Transition	t_{RS1}	—	1.0	—	0.670	—	0.500	μs	3, 7
Rise and Fall Times for CA1 and CA2 Input Signals	t_r, t_f	—	1.0	—	1.0	—	1.0	μs	8
Delay Time from CA1 Active Transition to CA2 Positive Transition	t_{RS2}	—	2.0	—	1.35	—	1.0	μs	3, 8
Delay Time, Enable Negative Transition to Data Valid	t_{PDW}	—	1.0	—	0.670	—	0.5	μs	3, 9, 10
Delay Time, Enable Negative Transition to CMOS Data Valid PA0-PA7, CA2	t_{CMOS}	—	2.0	—	1.35	—	1.0	μs	4, 9
Delay Time, Enable Positive Transition to CB2 Negative Transition	t_{CB2}	—	1.0	—	0.670	—	0.5	μs	3, 11, 12
Delay Time, Data Valid to CB2 Negative Transition	t_{DC}	20	—	20	—	20	—	ns	3, 10
Delay Time, Enable Positive Transition to CB2 Positive Transition	t_{RS1}	—	1.0	—	0.670	—	0.5	μs	3, 11
Control Output Pulse Width, CA2/CB2	PW_{CT}	500	—	375	—	250	—	ns	3, 11
Rise and Fall Time for CB1 and CB2 Input Signals	t_r, t_f	—	1.0	—	1.0	—	1.0	μs	12
Delay Time, CB1 Active Transition to CB2 Positive Transition	t_{RS2}	—	2.0	—	1.35	—	1.0	μs	3, 12
Interrupt Release Time, $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$	t_{IR}	—	1.60	—	1.10	—	0.85	μs	5, 14
Interrupt Response Time	t_{RS3}	—	1.0	—	1.0	—	1.0	μs	5, 13
Interrupt Input Pulse Time	PW_I	500	—	500	—	500	—	ns	13
RESET Low Time*	t_{RL}	1.0	—	0.66	—	0.5	—	μs	15

*The RESET line must be high a minimum of 1.0 μs before addressing the PIA.

FIGURE 2 — BUS TIMING TEST LOADS

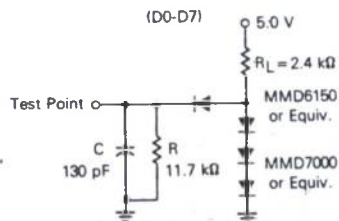


FIGURE 4 — CMOS EQUIVALENT TEST LOAD

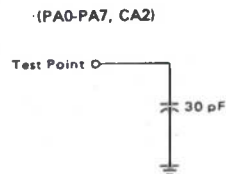


FIGURE 3 — TTL EQUIVALENT TEST LOAD

(PA0-PA7, PB0-PB7, CA2, CB2)

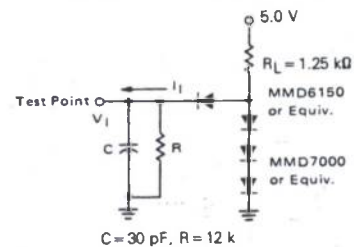


FIGURE 5 — NMOS EQUIVALENT TEST LOAD

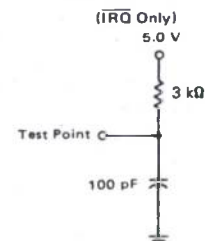
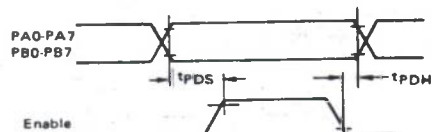
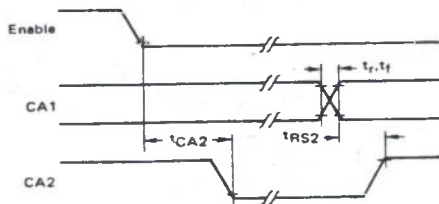
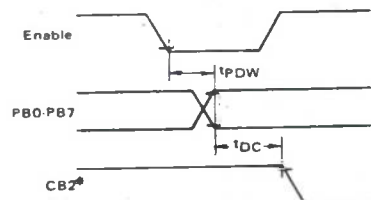
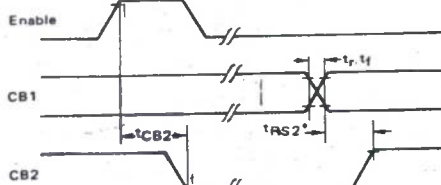
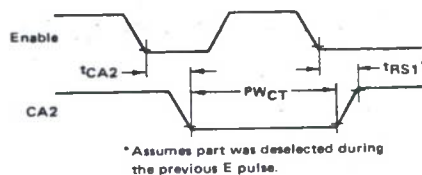


FIGURE 6 — PERIPHERAL DATA SETUP AND HOLD TIMES
(Read Mode)FIGURE 8 — CA2 DELAY TIME
(Read Mode; CRA-5 = 1, CRA-3 = CRA-4 = 0)FIGURE 10 — PERIPHERAL DATA AND CB2 DELAY TIMES
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)

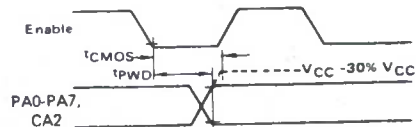
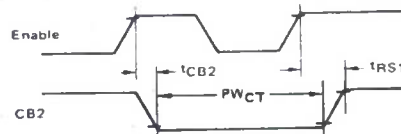
* CB2 goes low as a result of the positive transition of Enable.

FIGURE 12 — CB2 DELAY TIME
(Write Mode; CRB-5 = 1, CRB-3 = CRB-4 = 0)

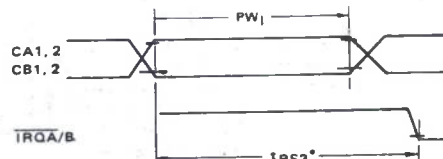
* Assumes part was deselected during any previous E pulse.

FIGURE 7 — CA2 DELAY TIME
(Read Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)

* Assumes part was deselected during the previous E pulse.

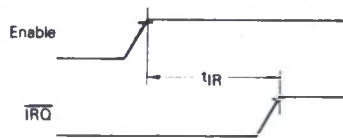
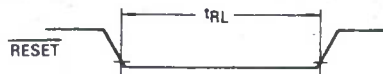
FIGURE 9 — PERIPHERAL CMOS DATA DELAY TIMES
(Write Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)FIGURE 11 — CB2 DELAY TIME
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)

* Assumes part was deselected during the previous E pulse.

FIGURE 13 — INTERRUPT PULSE WIDTH AND $\overline{IRQ}/B$ RESPONSE

* Assumes Interrupt Enable Bits are set.

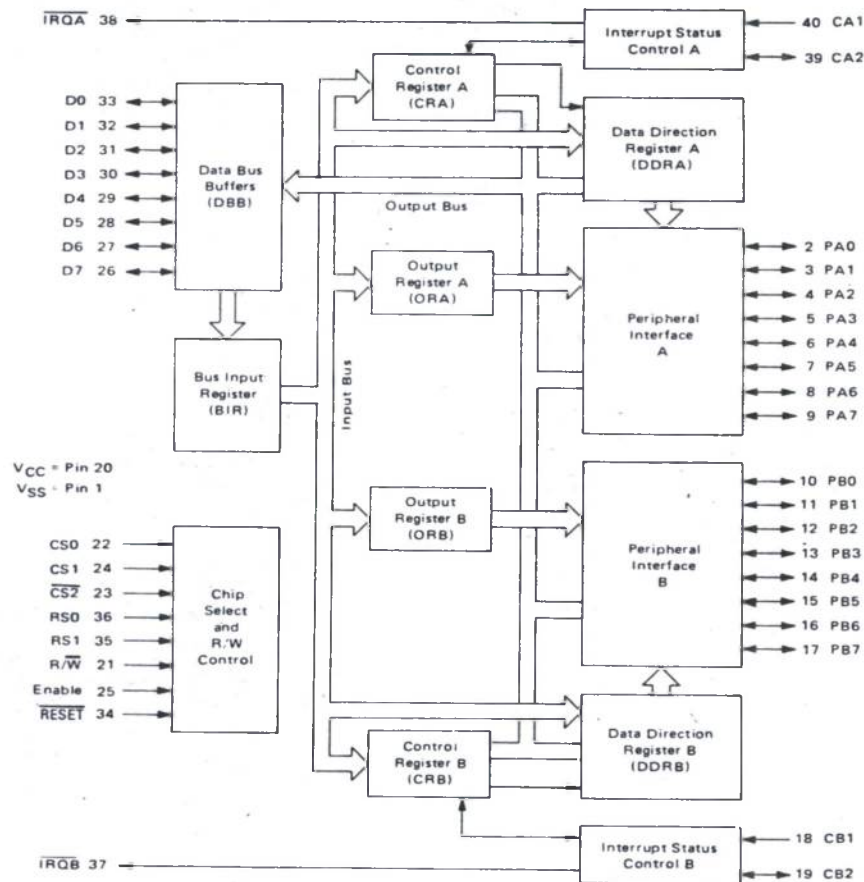
Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 14 — $\overline{\text{IRQ}}$ RELEASE TIMEFIGURE 15 — $\overline{\text{RESET}}$ LOW TIME

*The $\overline{\text{RESET}}$ line must be a V_{IH} for a minimum of $1.0 \mu\text{s}$ before addressing the PIA.

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 16 — EXPANDED BLOCK DIAGRAM



PIA INTERFACE SIGNALS FOR MPU

The PIA interfaces to the M6800 bus with an 8-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, a read/write line, an enable line and a reset line. To ensure proper operation with the MC6800, MC6802, or MC6808 microprocessors, VMA should be used as an active part of the address decoding.

Bidirectional Data (D0-D7) — The bidirectional data lines (D0-D7) allow the transfer of data between the MPU and the PIA. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs a PIA read operation. The read/write line is in the read (high) state when the PIA is selected for a read operation.

Enable (E) — The enable pulse, E, is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse.

Read/Write (R/W) — This signal is generated by the MPU to control the direction of data transfers on the data bus. A low state on the PIA read/write line enables the input buffers and data is transferred from the MPU to the PIA on the E signal if the device has been selected. A high on the read/write line sets up the PIA for a transfer of data to the bus. The PIA output buffers are enabled when the proper address and the enable pulse E are present.

RESET — The active low **RESET** line is used to reset all register bits in the PIA to a logical zero (low). This line can be used as a power-on reset and as a master reset during system operation.

Chip Selects (CS0, CS1, and CS2) — These three input signals are used to select the PIA. CS0 and CS1 must be high and CS2 must be low for selection of the device. Data transfers are then performed under the control of the enable and read/write signals. The chip select lines must be stable

for the duration of the E pulse. The device is deselected when any of the chip selects are in the inactive state.

Register Selects (RS0 and RS1) — The two register select lines are used to select the various registers inside the PIA. These two lines are used in conjunction with internal Control Registers to select a particular register that is to be written or read.

The register and chip select lines should be stable for the duration of the E pulse while in the read or write cycle.

Interrupt Request (IRQA and IRQB) — The active low Interrupt Request lines (IRQA and IRQB) act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are "open drain" (no load device on the chip). This permits all interrupt request lines to be tied together in a wire-OR configuration.

Each Interrupt Request line has two internal interrupt flag bits that can cause the Interrupt Request line to go low. Each flag bit is associated with a particular peripheral interrupt line. Also, four interrupt enable bits are provided in the PIA which may be used to inhibit a particular interrupt from a peripheral device.

Servicing an interrupt by the MPU may be accomplished by a software routine that, on a prioritized basis, sequentially reads and tests the two control registers in each PIA for interrupt flag bits that are set.

The interrupt flags are cleared (zeroed) as a result of an MPU Read Peripheral Data Operation of the corresponding data register. After being cleared, the interrupt flag bit cannot be enabled to be set until the PIA is deselected during an E pulse. The E pulse is used to condition the interrupt control lines (CA1, CA2, CB1, CB2). When these lines are used as interrupt inputs, at least one E pulse must occur from the inactive edge to the active edge of the interrupt input signal to condition the edge sense network. If the interrupt flag has been enabled and the edge sense circuit has been properly conditioned, the interrupt flag will be set on the next active transition of the interrupt input pin.

PIA PERIPHERAL INTERFACE LINES

The PIA provides two 8-bit bidirectional data buses and four interrupt/control lines for interfacing to peripheral devices.

Section A Peripheral Data (PA0-PA7) — Each of the peripheral data lines can be programmed to act as an input or output. This is accomplished by setting a "1" in the corresponding Data Direction Register bit for those lines which are to be outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral data line to act as an input. During an MPU Read Peripheral Data Operation, the data on peripheral lines programmed to act as inputs appears directly on the corresponding MPU Data Bus lines. In the input mode, the internal pullup resistor on these lines represents a maximum of 1.5 standard TTL loads.

The data in Output Register A will appear on the data lines that are programmed to be outputs. A logical "1" written into the register will cause a "high" on the corresponding data

line while a "0" results in a "low." Data in Output Register A may be read by an MPU "Read Peripheral Data A" operation when the corresponding lines are programmed as outputs. This data will be read properly if the voltage on the peripheral data lines is greater than 2.0 volts for a logic "1" output and less than 0.8 volt for a logic "0" output. Loading the output lines such that the voltage on these lines does not reach full voltage causes the data transferred into the MPU on a Read operation to differ from that contained in the respective bit of Output Register A.

Section B Peripheral Data (PB0-PB7) — The peripheral data lines in the B Section of the PIA can be programmed to act as either inputs or outputs in a similar manner to PA0-PA7. They have three-state capability, allowing them to enter a high-impedance state when the peripheral data line is used as an input. In addition, data on the peripheral data lines

PB0-PB7 will be read properly from those lines programmed as outputs even if the voltages are below 2.0 volts for a "high" or above 0.8 V for a "low". As outputs, these lines are compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch.

Interrupt Input (CA1 and CB1) — Peripheral input lines CA1 and CB1 are input only lines that set the interrupt flags of the control registers. The active transition for these signals is also programmed by the two control registers.

Peripheral Control (CA2) — The peripheral control line CA2 can be programmed to act as an interrupt input or as a

peripheral control output. As an output, this line is compatible with standard TTL; as an input the internal pullup resistor on this line represents 1.5 standard TTL loads. The function of this signal line is programmed with Control Register A.

Peripheral Control (CB2) — Peripheral Control line CB2 may also be programmed to act as an interrupt input or peripheral control output. As an input, this line has high input impedance and is compatible with standard TTL. As an output it is compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch. This line is programmed by Control Register B.

INTERNAL CONTROLS

INITIALIZATION

A RESET has the effect of zeroing all PIA registers. This will set PA0-PA7, PB0-PB7, CA2 and CB2 as inputs, and all interrupts disabled. The PIA must be configured during the restart program which follows the reset.

There are six locations within the PIA accessible to the MPU data bus: two Peripheral Registers, two Data Direction Registers, and two Control Registers. Selection of these locations is controlled by the RS0 and RS1 inputs together with bit 2 in the Control Register, as shown in Table 1.

Details of possible configurations of the Data Direction and Control Register are as follows:

TABLE 1 — INTERNAL ADDRESSING

RS1	RS0	Control Register Bit		Location Selected
		CRA-2	CRB-2	
0	0	1	X	Peripheral Register A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

X = Don't Care

PORT A-B HARDWARE CHARACTERISTICS

As shown in Figure 17, the MC6821 has a pair of I/O ports whose characteristics differ greatly. The A side is designed to drive CMOS logic to normal 30% to 70% levels, and incorporates an internal pullup device that remains connected even in the input mode. Because of this, the A side requires more drive current in the input mode than Port B. In contrast, the B side uses a normal three-state NMOS buffer which cannot pullup to CMOS levels without external resistors. The B side can drive extra loads such as Darlington transistors without problem. When the PIA comes out of reset, the A port represents inputs with pullup resistors, whereas the B side (input mode also) will float high or low, depending upon the load connected to it.

Notice the differences between a Port A and Port B read operation when in the output mode. When reading Port A, the actual pin is read, whereas the B side read comes from an output latch, ahead of the actual pin.

CONTROL REGISTERS (CRA and CRB)

The two Control Registers (CRA and CRB) allow the MPU to control the operation of the four peripheral control lines CA1, CA2, CB1, and CB2. In addition they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers may be written or read by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read only and are modified by external interrupts occurring on control lines CA1, CA2, CB1, or CB2. The format of the control words is shown in Figure 18.

DATA DIRECTION ACCESS CONTROL BIT (CRA-2 and CRB-2)

Bit 2, in each Control Register (CRA and CRB), determines selection of either a Peripheral Output Register or the corresponding Data Direction Register when the proper register select signals are applied to RS0 and RS1. A "1" in bit 2 allows access of the Peripheral Interface Register, while a "0" causes the Data Direction Register to be addressed.

Interrupt Flags (CRA-6, CRA-7, CRB-6, and CRB-7) — The four interrupt flag bits are set by active transitions of signals on the four Interrupt and Peripheral Control lines when those lines are programmed to be inputs. These bits cannot be set directly from the MPU Data Bus and are reset indirectly by a Read Peripheral Data Operation on the appropriate section.

Control of CA2 and CB2 Peripheral Control Lines (CRA-3, CRA-4, CRA-5, CRB-3, CRB-4, and CRB-5) — Bits 3, 4, and 5 of the two control registers are used to control the CA2 and CB2 Peripheral Control lines. These bits determine if the control lines will be an interrupt input or an output control signal. If bit CRA-5 (CRB-5) is low, CA2 (CB2) is an interrupt input line similar to CA1 (CB1). When CRA-5 (CRB-5) is high, CA2 (CB2) becomes an output signal that may be used to control peripheral data transfers. When in the output mode, CA2 and CB2 have slightly different loading characteristics.

Control of CA1 and CB1 Interrupt Input Lines (CRA-0, CRB-1, CRA-1, and CRB-1) — The two lowest-order bits of the control registers are used to control the interrupt input lines CA1 and CB1. Bits CRA-0 and CRB-0 are used to

enable the MPU interrupt signals $\overline{IRQA}$ and $\overline{IRQB}$, respectively. Bits CRA-1 and CRB-1 determine the active transition of the interrupt input signals CA1 and CB1.

FIGURE 17 — PORT A AND PORT B EQUIVALENT CIRCUITS

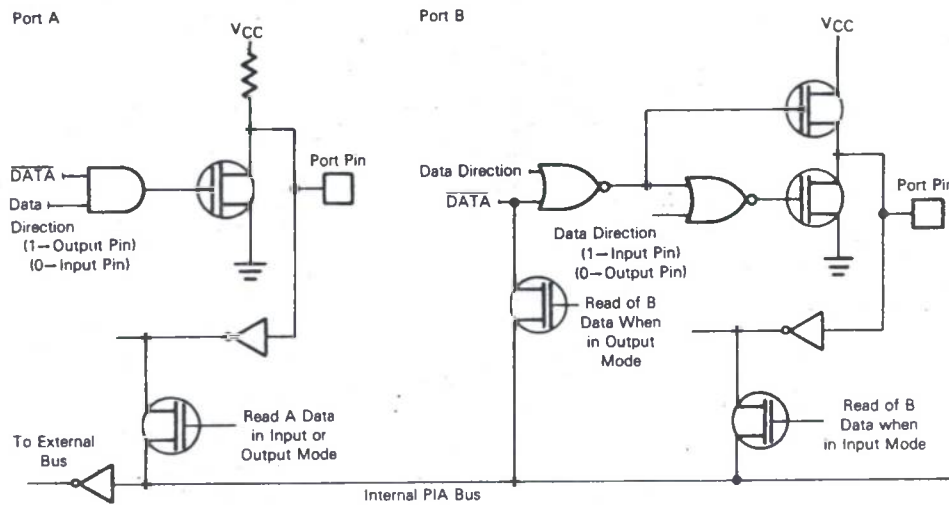
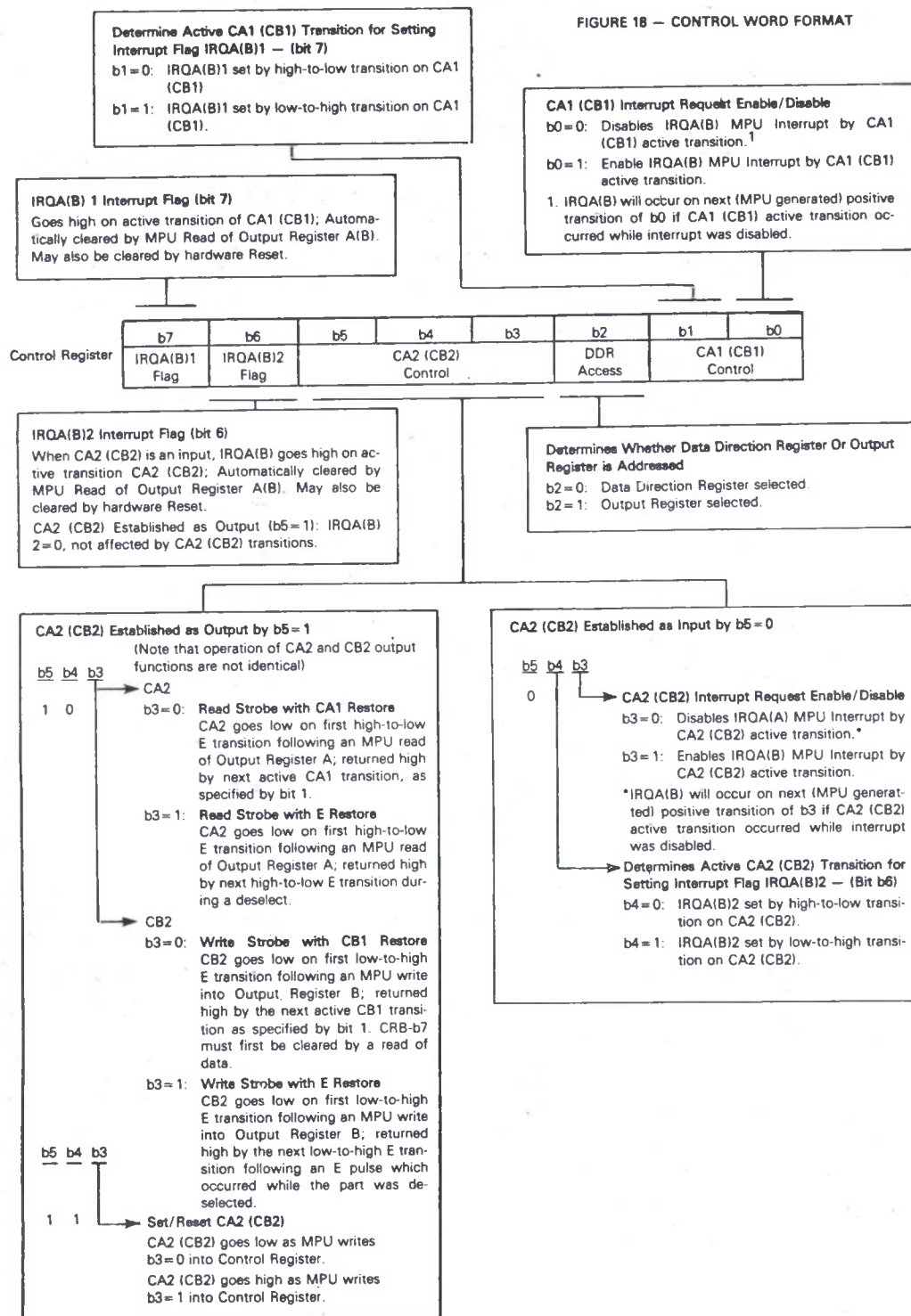


FIGURE 18 — CONTROL WORD FORMAT





MOTOROLA

PROGRAMMABLE TIMER MODULE (PTM)

The MC6840 is a programmable subsystem component of the M6800 family designed to provide variable system time intervals.

The MC6840 has three 16-bit binary counters, three corresponding control registers, and a status register. These counters are under software control and may be used to cause system interrupts and/or generate output signals. The MC6840 may be utilized for such tasks as frequency measurements, event counting, interval measuring, and similar tasks. The device may be used for square wave generation, gated delay signals, single pulses of controlled duration, and pulse width modulation as well as system interrupts.

- Operates from a Single 5 Volt Power Supply
- Fully TTL Compatible
- Single System Clock Required (Enable)
- Selectable Prescaler on Timer 3 Capable of 4 MHz for the MC6840, 6 MHz for the MC68A40 and 8 MHz for the MC68B40
- Programmable Interrupts (IRQ) Output to MPU
- Readable Down Counter Indicates Counts to Go Until Time-Out
- Selectable Gating for Frequency or Pulse-Width Comparison
- RESET Input
- Three Asynchronous External Clock and Gate/Trigger Inputs Internally Synchronized
- Three Maskable Outputs

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.3 to +7.0	V
Input Voltage	V _{in}	-0.3 to +7.0	V
Operating Temperature Range — T _L to T _H MC6840, MC68A40, MC68B40 MC6840C, MC68A40C	T _A	0 to +70 -40 to +85	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance			
Cerdip	θ _{JA}	65	°C/W
Plastic		115	
Ceramic		60	

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

MC6840
(1.0 MHz)

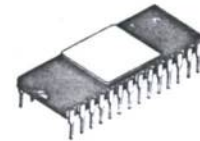
MC68A40
(1.5 MHz)

MC68B40
(2.0 MHz)

MOS

(N-CHANNEL, SILICON-GATE
DEPLETION LOAD)

PROGRAMMABLE TIMER



L SUFFIX
CERAMIC PACKAGE
CASE 719



P SUFFIX
PLASTIC PACKAGE
CASE 710



S SUFFIX
CERDIP PACKAGE
CASE 733

FIGURE 1 — PIN ASSIGNMENT

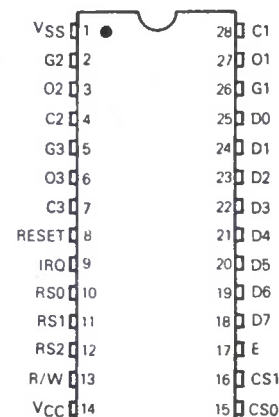
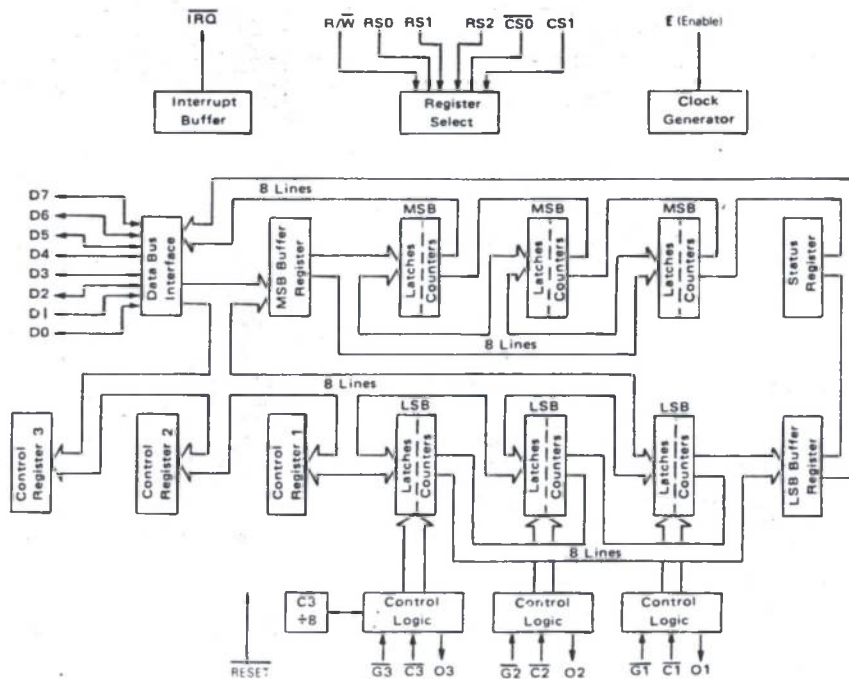


FIGURE 2 — BLOCK DIAGRAM



POWER CONSIDERATIONS

The average chip-junction temperature, T_J , in $^{\circ}\text{C}$ can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA})$$

(1)

Where:

T_A = Ambient Temperature, $^{\circ}\text{C}$

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, $^{\circ}\text{C}/\text{W}$

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

P_{PORT} = Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K + (T_J + 273^{\circ}\text{C})$$

(2)

Solving equations 1 and 2 for K gives:

$$K = P_D \cdot (T_A + 273^{\circ}\text{C}) + \theta_{JA} \cdot P_D^2$$

(3)

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A .

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0\text{ Vdc} \pm 5\%$, $V_{SS}=0$, $T_A=T_L$ to T_H unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	$V_{SS} + 2.0$	—	V_{CC}	V
Input Low Voltage	V_{IL}	$V_{SS} - 0.3$	—	$V_{SS} + 0.8$	V
Input Leakage Current ($V_{in} = 0$ to 5.25 V)	I_{in}	—	1.0	2.5	μA
Three-State (Off State) Input Current ($V_{in} = 0.5$ to 2.4 V)	D0-D7 I_{TSI}	—	2.0	10	μA
Output High Voltage ($I_{Load} = -205\text{ }\mu\text{A}$) ($I_{Load} = -200\text{ }\mu\text{A}$)	D0-D7 Other Outputs V_{OH}	$V_{SS} + 2.4$ $V_{SS} + 2.4$	— —	— —	V
Output Low Voltage ($I_{Load} = 1.6\text{ mA}$) ($I_{Load} = 3.2\text{ mA}$)	D0-D7 O1-O3, $\overline{IRQ}$ V_{OL}	— —	— —	$V_{SS} + 0.4$ $V_{SS} + 0.4$	V
Output Leakage Current (Off State) ($V_{OH} = 2.4\text{ V}$)	$\overline{IRQ}$ I_{LOH}	—	1.0	10	μA
Internal Power Dissipation (Measured at $T_A = T_L$)	P_{INT}	—	470	700	mW
Input Capacitance ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)	D0-D7 All Others C_{in}	— —	— —	12.5 7.5	pF
Output Capacitance ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)	$\overline{IRQ}$ O1, O2, O3 C_{out}	— —	— —	5.0 10	pF

AC OPERATING CHARACTERISTICS (See Figures 4-9)

Characteristic	Symbol	MC6840		MC68A40		MC68B40		Unit
		Min	Max	Min	Max	Min	Max	
Input Rise and Fall Times (Figures 4 and 5) $\overline{C}$, $\overline{G}$ and $\overline{RESET}$	t_r, t_f	—	1.0*	—	0.666*	—	0.500*	μs
Input Pulse Width Low (Figure 4) (Asynchronous Input) $\overline{C}$, $\overline{G}$ and $\overline{RESET}$	PW_L	$t_{cycE} + t_{su} + t_{hd}$	—	$t_{cycE} + t_{su} + t_{hd}$	—	$t_{cycE} + t_{su} + t_{hd}$	—	ns
Input Pulse Width High (Figure 5) (Asynchronous Input) $\overline{C}$, $\overline{G}$	PW_H	$t_{cycE} + t_{su} + t_{hd}$	—	$t_{cycE} + t_{su} + t_{hd}$	—	$t_{cycE} + t_{su} + t_{hd}$	—	ns
Input Setup Time (Figure 6) (Synchronous Input) $\overline{C}$, $\overline{G}$ and $\overline{RESET}$	t_{su}	200	—	120	—	75	—	ns
Input Hold Time (Figure 6) (Synchronous Input) $\overline{C}$, $\overline{G}$ and $\overline{RESET}$	t_{hd}	50	—	50	—	50	—	ns
Input Synchronization Time (Figure 9) $\overline{C3}$ (+8 Prescaler Mode Only)	t_{sync}	250	—	200	—	175	—	ns
Input Pulse Width $\overline{C3}$ (+8 Prescaler Mode Only)	PW_L, PW_H	120	—	80	—	60	—	ns
Output Delay, O1-O3 (Figure 7) ($V_{OH} = 2.4\text{ V}$, Load B)	TTL t_{co}	—	700	—	460	—	340	ns
($V_{OH} = 2.4\text{ V}$, Load D)	MOS t_{cm}	—	450	—	450	—	340	ns
($V_{OH} = 0.7 V_{DD}$, Load D)	CMOS t_{cmos}	—	2.0	—	1.35	—	1.0	μs
Interrupt Release Time	t_{IR}	—	1.2	—	0.9	—	0.7	μs

* t_r and $t_f \leq t_{cycE}$

BUS TIMING CHARACTERISTICS (See Notes 1, 2, and 3)

Ident. Number	Characteristic	Symbol	MC6840		MC68A40		MC68B40		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1.0	10	0.67	10	0.5	10	μs
2	Pulse Width, E Low	PW_{EL}	430	9500	280	9500	210	9500	ns
3	Pulse Width, E High	PW_{EH}	450	9500	280	9500	220	9500	ns
4	Clock Rise and Fall Time	t_r, t_f	—	25	—	25	—	20	ns
9	Address Hold Time	t_{AH}	10	—	10	—	10	—	ns
13	Address Setup Time Before E	t_{AS}	80	—	60	—	40	—	ns
14	Chip Select Setup Time Before E	t_{CS}	80	—	60	—	40	—	ns
15	Chip Select Hold Time	t_{CH}	10	—	10	—	10	—	ns
18	Read Data Hold Time	t_{DHR}	20	50*	20	50*	20	50*	ns
21	Write Data Hold Time	t_{DHW}	10	—	10	—	10	—	ns
30	Peripheral Output Data Delay Time	t_{DDR}	—	290	—	180	—	150	ns
31	Peripheral Input Data Setup Time	t_{DSW}	165	—	80	—	60	—	ns

*The data bus output buffers are no longer sourcing or sinking current by t_{DHR} max (High Impedance).

FIGURE 3 — BUS TIMING

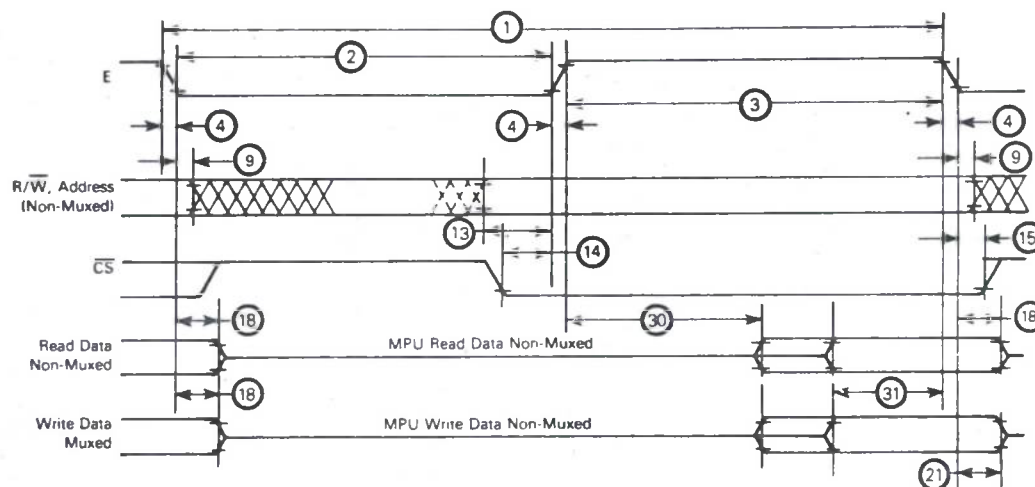


FIGURE 4 — INPUT PULSE WIDTH LOW

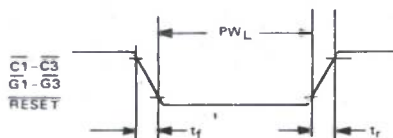
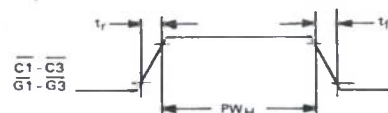


FIGURE 5 — INPUT PULSE WIDTH HIGH



NOTES:

1. Not all signals are applicable to every part.
2. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
3. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

FIGURE 6 — INPUT SETUP AND HOLD TIMES

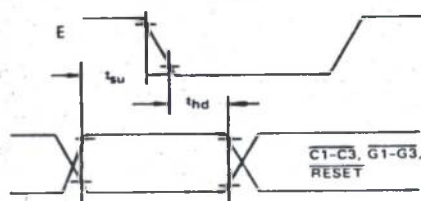


FIGURE 7 — OUTPUT DELAY

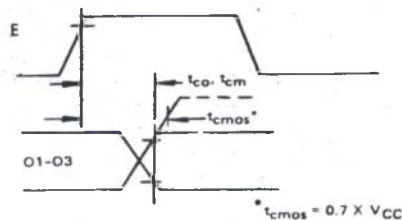
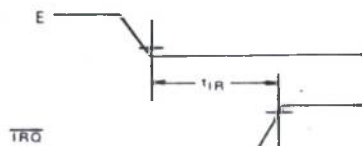
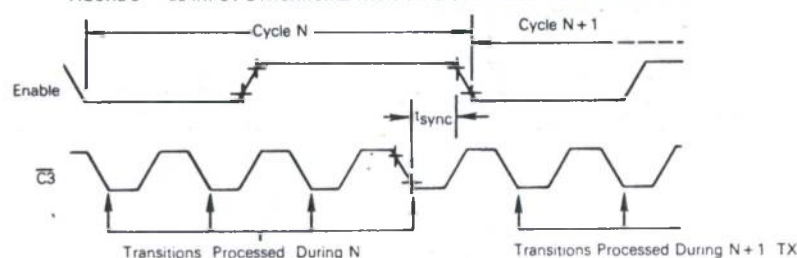
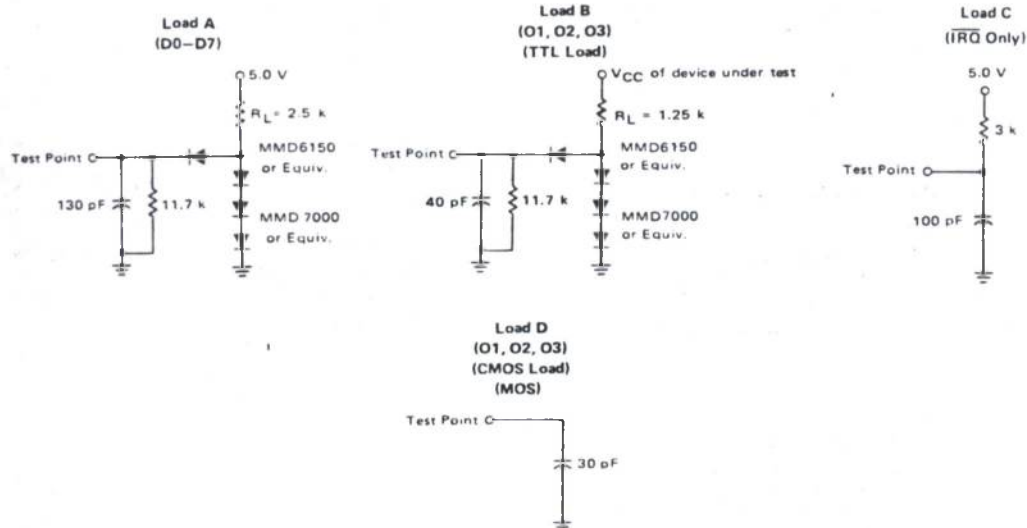
FIGURE 8 — $\overline{\text{IRQ}}$ RELEASE TIMEFIGURE 9 — $\overline{\text{C3}}$ INPUT SYNCHRONIZATION TIME (+8 PRESCALER MODE ONLY)

FIGURE 10 — BUS TIMING TEST LOADS



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

DEVICE OPERATION

The MC6840 is part of the M6800 microprocessor family and is fully bus compatible with M6800 systems. The three timers in the MC6840 operate independently and in several distinct modes to fit a wide variety of measurement and synthesis applications.

The MC6840 is an integrated set of three distinct counter/timers (Figure 1). It consists of three 16-bit data latches, three 16-bit counters (clocked independently), and the comparison and enable circuitry necessary to implement various measurement and synthesis functions. In addition, it contains interrupt drivers to alert the processor that a particular function has been completed.

In a typical application, a timer will be loaded by first storing two bytes of data into an associated Counter Latch. This data is then transferred into the counter via a Counter Initialization cycle. If the counter is enabled, the counter decrements on each subsequent clock period which may be an external clock, or Enable (E) until one of several predetermined conditions causes it to halt or recycle. The timers are thus programmable, cyclic in nature, controllable by external inputs or the MPU program, and accessible by the MPU at any time.

BUS INTERFACE

The Programmable Timer Module (PTM) interfaces to the M6800 Bus with an 8-bit bidirectional data bus, two Chip Select lines, a Read/Write line, a clock (Enable) line, and Interrupt Request line, an external Reset line, and three Register select lines. VMA should be utilized in conjunction with an MPU address line into a Chip Select of the PTM when using the MC6800/6802/6808.

BIDIRECTIONAL DATA (D0-D7) — The bidirectional data lines (D0-D7) allow the transfer of data between the MPU and PTM. The data bus output drivers are three-state devices which remain in the high-impedance (off) state except when the MPU performs a PTM read operation (Read/Write and Enable lines high and PTM Chip Selects activated).

CHIP SELECT ($\overline{CS0}$, $\overline{CS1}$) — These two signals are used to activate the Data Bus interface and allow transfer of data from the PTM. With $\overline{CS0}=0$ and $\overline{CS1}=1$, the device is selected and data transfer will occur.

READ/WRITE ($\overline{R/\overline{W}}$) — This signal is generated by the MPU to control the direction of data transfer on the Data Bus. With the PTM selected, a low state on the PTM $\overline{R/\overline{W}}$ line enables the input buffers and data is transferred from the MPU to the PTM on the trailing edge of the E (Enable) clock. Alternately, (under the same conditions) $\overline{R/\overline{W}}=1$ and Enable high allows data in the PTM to be read by the MPU.

ENABLE (E CLOCK) — The E clock signal synchronizes data transfer between the MPU and the PTM. It also performs an equivalent synchronization function on the external clock, reset, and gate inputs of the PTM.

INTERRUPT REQUEST ($\overline{IRQ}$) — The active low Interrupt Request signal is normally tied directly (or through priority interrupt circuitry) to the $\overline{IRQ}$ input of the MPU. This is an

"open drain" output (no load device on the chip) which permits other similar interrupt request lines to be tied together in a wire-OR configuration.

The $\overline{IRQ}$ line is activated if, and only if, the Composite Interrupt Flag (Bit 7 of the Internal Status Register) is asserted. The conditions under which the $\overline{IRQ}$ line is activated are discussed in conjunction with the Status Register.

RESET — A low level at this input is clocked into the PTM by the E (Enable) input. Two Enable pulses are required to synchronize and process the signal. The PTM then recognizes the active "low" or inactive "high" on the third Enable pulse. If the RESET signal is asynchronous, an additional Enable period is required if setup times are not met. The RESET input must be stable High/Low for the minimum time stated in the AC Operating Characteristics.

Recognition of a low level at this input by the PTM causes the following action to occur:

- All counter latches are preset to their maximum count values.
- All Control Register bits are cleared with the exception of CR10 (internal reset bit) which is set.
- All counters are preset to the contents of the latches.
- All counter outputs are reset and all counter clocks are disabled.
- All Status Register bits (interrupt flags) are cleared.

REGISTER SELECT LINES (RS0, RS1, RS2) — These inputs are used in conjunction with the R/W line to select the internal registers, counters and latches as shown in Table 1.

NOTE:

The PTM is accessed via MPU Load and Store operations in much the same manner as a memory device. The instructions available with the M6800 family of MPUs which perform read-modify-write operations on memory should not be used when the PTM is accessed. These instructions actually fetch a byte from memory, perform an operation, then restore it to the same address location. Since the PTM uses the R/W line as an additional register select input, the modified data will not be restored to the same register if these instructions are used.

CONTROL REGISTER

Each timer in the MC6840 has a corresponding write-only Control Register. Control Register #2 has a unique address space (RS0=1, RS=0, RS2=0) and therefore may be written into at any time. The remaining Control Registers (#1 and #3) share the Address Space selected by a logic zero on all Register Select inputs.

CR20 — The least-significant bit of Control Register #2 (CR20) is used as an additional addressing bit for Control Registers #1 and #3. Thus, with all Register selects and R/W inputs at logic zero, Control Register #1 will be written into if CR20 is a logic one. Under the same conditions, Control Register #3 can also be written into after a RESET low condition has occurred, since all control register bits (except CR10) are cleared. Therefore, one may write in the sequence CR3, CR2, CR1.

TABLE 1 – REGISTER SELECTION

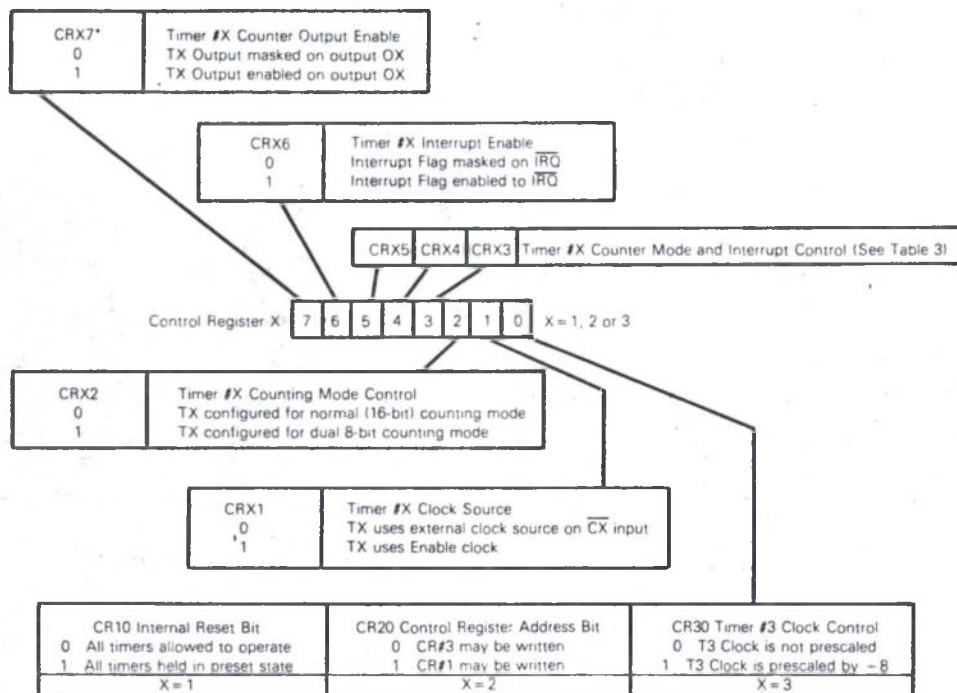
Register Select Inputs			Operations	
RS2	RS1	RS0	$R/\overline{W} = 0$	$R/\overline{W} = 1$
0	0	0	CR20 = 0 Write Control Register #3 CR20 = 1 Write Control Register #1	No Operation
0	0	1	Write Control Register #2	Read Status Register
0	1	0	Write MSB Buffer Register	Read Timer #1 Counter
0	1	1	Write Timer #1 Latches	Read LSB Buffer Register
1	0	0	Write MSB Buffer Register	Read Timer #2 Counter
1	0	1	Write Timer #2 Latches	Read LSB Buffer Register
1	1	0	Write MSB Buffer Register	Read Timer #3 Counter
1	1	1	Write Timer #3 Latches	Read LSB Buffer Register

CR10 — The least-significant bit of Control Register #1 is used as an Internal Reset bit. When this bit is a logic zero, all timers are allowed to operate in the modes prescribed by the remaining bits of the control registers. Writing a “one” into CR10 causes all counters to be preset with the contents of the corresponding counter latches, all counter clocks to be disabled, and the timer outputs and interrupt flags (Status Register) to be reset. Counter Latches and Control Registers are undisturbed by an Internal Reset and may be written into regardless of the state of CR10.

The least-significant bit of Control Register #3 is used as a selector for a $\div 8$ prescaler which is available with Timer #3 only. The prescaler, if selected, is effectively placed between the clock input circuitry and the input to Counter #3. It can therefore be used with either the internal clock (Enable) or an external clock source.

CR30 — The functions depicted in the foregoing discussions are tabulated in Table 2 for ease of reference.

TABLE 2 — CONTROL REGISTER BITS



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Timer #2.
function o
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CRX2 — information frequently loaded into 16-bit word. Mode (CRX2 + 1) enables 16-bit number. Similar Timing clock period and MSB.

CRX3-C
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STATUS REGISTER
The MC68000 contains a 16-bit status register (read-only). Each bit of the register is set or cleared by the processor. The bits are: Interrupt Flag (IF), Equal Flag (ZF), Register File Error Flag (RFE), and the Com-

INT:
whe

Control Register Bits CR10, CR20, and CR30 are unique in that each selects a different function. The remaining bits (1 through 7) of each Control Register select common functions, with a particular Control Register affecting only its corresponding timer.

CRX1 — Bit 1 of Control Register #1 (CR11) selects whether an internal or external clock source is to be used with Timer #1. Similarly, CR21 selects the clock source for Timer #2, and CR31 performs this function for Timer #3. The function of each bit of Control Register "X" can therefore be defined as shown in the remaining section of Table 2.

CRX2 — Control Register Bit 2 selects whether the binary information contained in the Counter Latches (and subsequently loaded into the counter) is to be treated as a single 16-bit word or two 8-bit bytes. In the single 16-bit Counter Mode (CRX2=0) the counter will decrement to zero after $N+1$ enabled ($G=0$) clock periods, where N is defined as the 16-bit number in the Counter Latches. With CRX2=1, a similar Time Out will occur after $(L+1) \cdot (M+1)$ enabled clock periods, where L and M , respectively, refer to the LSB and MSB bytes in the Counter Latches.

CRX3-CRX7 — Control Register Bits 3, 4, and 5 are explained in detail in the Timer Operating Mode section. Bit 6 is an interrupt mask bit which will be explained more fully in conjunction with the Status Register, and bit 7 is used to enable the corresponding Timer Output. A summary of the control register programming modes is shown in Table 3.

STATUS REGISTER/INTERRUPT FLAGS

The MC6840 has an internal Read-Only Status Register which contains four Interrupt Flags. (The remaining four bits of the register are not used, and defaults to zeros when being read.) Bits 0, 1, and 2 are assigned to Timers 1, 2, and 3, respectively, as individual flag bits, while Bit 7 is a Composite Interrupt Flag. This flag bit will be asserted if any of the individual flag bits is set while Bit 6 of the corresponding Control Register is at a logic one. The conditions for asserting the composite Interrupt Flag bit can therefore be expressed as:

$$INT = I1 \cdot CR16 + I2 \cdot CR26 + I3 \cdot CR36$$

where INT = Composite Interrupt Flag (Bit 7)

I1 = Timer #1 Interrupt Flag (Bit 0)

I2 = Timer #2 Interrupt Flag (Bit 1)

I3 = Timer #3 Interrupt Flag (Bit 2)

An interrupt flag is cleared by a Timer Reset condition, i.e., External RESET=0 or Internal Reset Bit (CR10)=1. It will also be cleared by a Read Timer Counter Command provided that the Status Register has previously been read while the interrupt flag was set. This condition on the Read Status Register-Read Timer Counter (RS-RT) sequence is designed to prevent missing interrupts which might occur after the status register is read, but prior to reading the Timer Counter.

An Individual Interrupt Flag is also cleared by a Write Timer Latches (W) command or a Counter Initialization (CI) sequence, provided that W or CI affects the Timer corresponding to the individual Interrupt Flag.

COUNTER LATCH INITIALIZATION

Each of the three independent timers consists of a 16-bit addressable counter and a 16-bit addressable latch. The counters are preset to the binary numbers stored in the latches. Counter initialization results in the transfer of the latch contents to the counter. See notes in Table 4 regarding the binary number N , L , or M placed into the Latches and their relationship to the output waveforms and counter Time-Outs.

Since the PTM data bus is 8-bits wide and the counters are 16-bits wide, a temporary register (MSB Buffer Register) is provided. This "write only" register is for the Most-Significant Byte of the desired latch data. Three addresses are provided for the MSB Buffer Register (as indicated in Table 1), but they all lead to the same Buffer. Data from the MSB Buffer will automatically be transferred into the Most-Significant Byte of Timer #X when a Write Timer #X Latches Command is performed. So it can be seen that the MC6840 has been designed to allow transfer of two bytes of data into the counter latches provided that the MSB is transferred first. The storage order must be observed to ensure proper latch operation.

In many applications, the source of the data will be an M6800 Family MPU. It should be noted that the 16-bit store operations of the M6800 family microprocessors (STS and STX) transfer data in the order required by the PTM. A Store Index Register Instruction, for example, results in the MSB of the X register being transferred to the selected address, then the LSB of the X register being written into the next higher location. Thus, either the index register or stack pointer may be transferred directly into a selected counter latch with a single instruction.

A logic zero at the RESET input also initializes the counter latches. In this case, all latches will assume a maximum count of 65,535₁₀. It is important to note that an Internal

TABLE 3 — PTM OPERATING MODE SELECTION

CRX3	CRX4	CRX5	
0	0	0	Continuous Operating Mode: Gate 1 or Write to Latches or Reset Causes Counter Initialization
0	0	1	Frequency Comparison Mode: Interrupt If Gate $\uparrow$ is < Counter Time Out
0	1	0	Continuous Operating Mode: Gate 1 or Reset Causes Counter Initialization
0	1	1	Pulse Width Comparison Mode: Interrupt If Gate $\uparrow$ is < Counter Time Out
1	0	0	Single Shot Mode: Gate 1 or Write to Latches or Reset Causes Counter Initialization
1	0	1	Frequency Comparison Mode: Interrupt If Gate $\uparrow$ is > Counter Time Out
1	1	0	Single Shot Mode: Gate 1 or Reset Causes Counter Initialization
1	1	1	Pulse Width Comparison Mode: Interrupt If Gate $\uparrow$ is > Counter Time Out

Reset (Bit zero of Control Register 1 Set) has no effect on the counter latches.

COUNTER INITIALIZATION

Counter Initialization is defined as the transfer of data from the latches to the counter with subsequent clearing of the Individual Interrupt Flag associated with the counter. Counter Initialization always occurs when a reset condition ($\overline{\text{RESET}}=0$ or $\text{CR10}=1$) is recognized. It can also occur — depending on Timer Mode — with a Write Timer Latches command or recognition of a negative transition of the Gate input.

Counter recycling or re-initialization occurs when a negative transition of the clock input is recognized after the counter has reached an all-zero state. In this case, data is transferred from the Latches to the Counter.

ASYNCHRONOUS INPUT/OUTPUT LINES

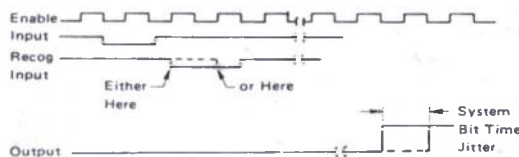
Each of the three timers within the PTM has external clock and gate inputs as well as a counter output line. The inputs are high-impedance, TTL-compatible lines and outputs are capable of driving two standard TTL loads.

CLOCK INPUTS ($\overline{\text{C1}}$, $\overline{\text{C2}}$, and $\overline{\text{C3}}$) — Input pins $\overline{\text{C1}}$, $\overline{\text{C2}}$, and $\overline{\text{C3}}$ will accept asynchronous TTL voltage level signals to decrement Timers 1, 2, and 3, respectively. The high and low levels of the external clocks must each be stable for at least one system clock period plus the sum of the setup and hold times for the clock inputs. The asynchronous clock rate can vary from dc to the limit imposed by the Enable Clock Setup, and Hold times.

The external clock inputs are clocked in by Enable pulses. Three Enable periods are used to synchronize and process the external clock. The fourth Enable pulse decrements the internal counter. This does not affect the input frequency, it merely creates a delay between a clock input transition and internal recognition of that transition by the PTM. All references to C inputs in this document relate to internal recognition of the input transition. Note that a clock high or low level which does not meet setup and hold time specifications may require an additional Enable pulse for recognition. When observing recurring events, a lack of synchronization will result in "jitter" being observed on the output of the PTM when using asynchronous clocks and gate input signals. There are two types of jitter. "System jitter" is the result of the input signals being out of synchronization with Enable, permitting signals with marginal setup and hold time to be recognized by either the bit time nearest the input transition or the subsequent bit time.

"Input jitter" can be as great as the time between input signal negative going transitions plus the system jitter, if the first transition is recognized during one system cycle, and not recognized the next cycle, or vice versa. See Figure 11.

FIGURE 11 — INPUT JITTER



CLOCK INPUT $\overline{\text{C3}}$ (+8 PRESCALER MODE) — External clock input $\overline{\text{C3}}$ represents a special case when Timer #3 is programmed to utilize its optional +8 prescaler mode.

The divide-by-8 prescaler contains an asynchronous ripple counter; thus, input setup (t_{SU}) and hold times (t_{HD}) do not apply. As long as minimum input pulse widths are maintained, the counter will recognize and process all input clock ($\overline{\text{C3}}$) transitions. However, in order to guarantee that a clock transition is processed during the current E cycle, a certain amount of synchronization time (t_{sync}) is required between the $\overline{\text{C3}}$ transition and the falling edge of Enable (see Figure 9). If the synchronization time requirement is not met, it is possible that the $\overline{\text{C3}}$ transition will not be processed until the following E cycle.

The maximum input frequency and allowable duty cycles for the +8 prescaler mode are specified under the AC Operating Characteristics. Internally, the +8 prescaler output is treated in the same manner as the previously discussed clock inputs.

GATE INPUTS ($\overline{\text{G1}}$, $\overline{\text{G2}}$, $\overline{\text{G3}}$) — Input pins $\overline{\text{G1}}$, $\overline{\text{G2}}$, and $\overline{\text{G3}}$ accept asynchronous TTL-compatible signals which are used as triggers or clock gating functions to Timers 1, 2, and 3, respectively. The gating inputs are clocked into the PTM by the E (enable) clock in the same manner as the previously discussed clock inputs. That is, a Gate transition is recognized by the PTM on the fourth Enable pulse (provided setup and hold time requirements are met), and the high or low levels of the Gate input must be stable for at least one system clock period plus the sum of setup and hold times. All references to G transition in this document relate to internal recognition of the input transition.

The Gate inputs of all timers directly affect the internal 16-bit counter. The operation of $\overline{\text{G3}}$ is therefore independent of the +8 prescaler selection.

TIMER OUTPUTS (O1 , O2 , O3) — Timer outputs O1 , O2 , and O3 are capable of driving up to two TTL loads and produce a defined output waveform for either Continuous or Single-Shot Timer modes. Output waveform definition is accomplished by selecting either Single 16-bit or Dual 8-bit operating modes. The Single 16-bit mode will produce a square-wave output in the continuous mode and a single pulse in the single-shot mode. The Dual 8-bit mode will produce a variable duty cycle pulse in both the continuous and single-shot timer modes. One bit of each Control Register (CRX7) is used to enable the corresponding output. If this bit is cleared, the output will remain low (V_{OL}) regardless of the operating mode. If it is cleared while the output is high the output will go low during the first enable cycle following a write to the Control Register.

The Continuous and Single-Shot Timer Modes are the only ones for which output response is defined in this data sheet. Refer to the Programmable Timer Fundamentals and Applications manual for a discussion of the output signals in other modes. Signals appear at the outputs (unless $\text{CRX7}=0$) during Frequency and Pulse Width comparison modes, but the actual waveform is not predictable in typical applications.

TIMER OPERATING MODES

The MC6840 has been designed to operate effectively in a wide variety of applications. This is accomplished by using three bits of each control register (CRX3, CRX4, and CRX5) to define different operating modes of the Timers. These modes are divided into WAVE SYNTHESIS and WAVE MEASUREMENT modes, and are outlined in Table 4.

TABLE 4 — OPERATING MODES

Control Register			Timer Operating Mode	
CRX3	CRX4	CRX5		
0	*	0	Continuous	Synthesizer
0	*	1	Single-Shot	
1	0	*	Frequency Comparison	Measurement
1	1	*	Pulse Width Comparison	

* Defines Additional Timer Function Selection.

One of the WAVE SYNTHESIS modes is the Continuous Operating mode, which is useful for cyclic wave generation. Either symmetrical or variable duty-cycle waves can be generated in this mode. The other wave synthesis mode, the Single-Shot mode, is similar in use to the Continuous operating mode, however, a single pulse is generated, with a programmable preset width.

The WAVE MEASUREMENT modes include the Frequency Comparison and Pulse Width Comparison modes which are used to measure cyclic and singular pulse widths, respectively.

In addition to the four timer modes in Table 4, the remaining control register bit is used to modify counter initialization and enabling or interrupt conditions.

WAVE SYNTHESIS MODES

CONTINUOUS OPERATING MODE (TABLE 5) — The continuous mode will synthesize a continuous wave with a period proportional to the preset number in the particular timer latches. Any of the timers in the PTM may be programmed to operate in a continuous mode by writing zeroes into bits 3 and 5 of the corresponding control register. Assuming

that the timer output is enabled (CRX7 = 1), either a square wave or a variable duty cycle waveform will be generated at the Timer Output, OX. The type of output is selected via Control Register Bit 2.

Either a Timer Reset (CR10 = 1 or External Reset = 0) condition or internal recognition of a negative transition of the Gate input results in Counter Initialization. A Write Timer latches command can be selected as a Counter Initialization signal by clearing CRX4.

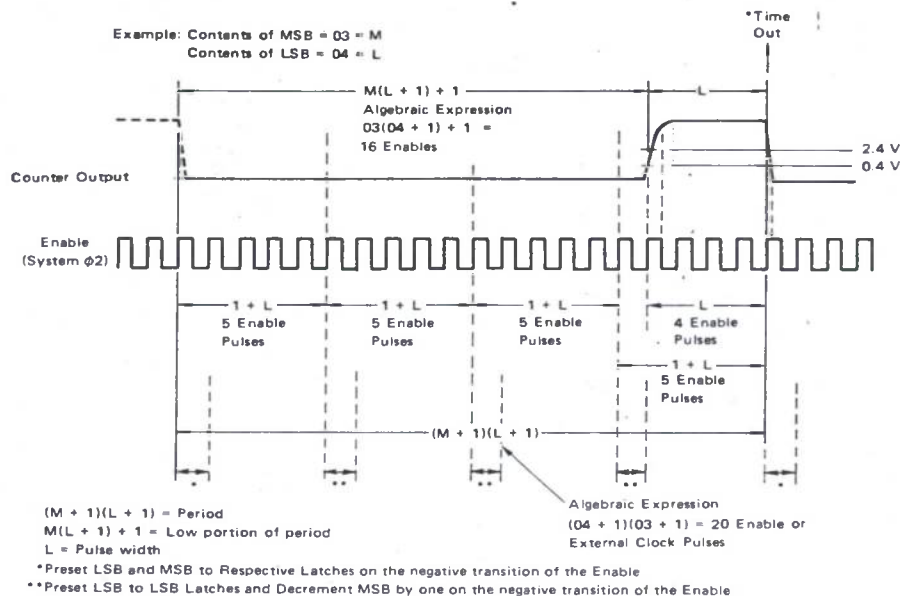
The counter is enabled by an absence of a Timer Reset condition and a logic zero at the Gate input. In the 16-bit mode, the counter will decrement on the first clock cycle during or after the counter initialization cycle. It continues to decrement on each clock signal so long as G remains low and no reset condition exists. A Counter Time Out (the first clock after all counter bits = 0) results in the Individual Interrupt Flag being set and reinitialization of the counter.

In the Dual 8-bit mode (CRX2 = 1) (refer to the example in Figure 12 and Tables 5 and 6) the MSB decrements once for every full countdown of the LSB + 1. When the LSB = 0, the MSB is unchanged; on the next clock pulse the LSB is reset to the count in the LSB Latches, and the MSB is decremented by 1 (one). The output, if enabled, remains low during and after initialization and will remain low until the counter MSB is all zeroes. The output will go high at the beginning of the next clock pulse. The output remains high until both the LSB and MSB of the counter are all zeroes. At the beginning of the next clock pulse the defined Time Out (TO) will occur and the output will go low. In the Dual 8-bit mode the period of the output of the example in Figure 12 would span 20 clock pulses as opposed to 1546 clock pulses using the normal 16-bit mode.

A special time-out condition exists for the dual 8-bit mode (CRX2 = 1) if L = 0. In this case, the counter will revert to a mode similar to the single 16-bit mode, except Time Out occurs after M + 1* clock pulses. The output, if enabled, goes low during the Counter Initialization cycle and reverses state at each Time Out. The counter remains cyclical (is reinitialized at each Time Out) and the Individual Interrupt Flag is set when Time Out occurs. If M = L = 0, the internal counters do not change, but the output toggles at a rate of 1/2 the clock frequency.

TABLE 5 — CONTINUOUS OPERATING MODES

Synthesis Modes		CONTINUOUS MODE (CRX3 = 0, CRX5 = 0)	
Control Register		Initialization/Output Waveforms	
CRX2	CRX4	Counter Initialization	*Timer Output (OX) (CRX7 = 1)
0	0	$\overline{G} \downarrow + W + R$	
0	1	$\overline{G} \downarrow + R$	
1	0	$\overline{G} \downarrow + W + R$	
1	1	$\overline{G} \downarrow + R$	

FIGURE 12 — TIMER OUTPUT WAVEFORM EXAMPLE
(Continuous Dual 8-Bit Mode Using Internal Enable)

The discussion of the Continuous Mode has assumed that the application requires an output signal. It should be noted that the Timer operates in the same manner with the output disabled (CRX7=0). A Read Timer Counter command is valid regardless of the state of CRX7.

SINGLE-SHOT TIMER MODE — This mode is identical to the Continuous Mode with three exceptions. The first of these is obvious from the name — the output returns to a low level after the initial Time Out and remains low until another Counter Initialization cycle occurs.

As indicated in Table 6, the internal counting mechanism remains cyclical in the Single-Shot Mode. Each Time Out of

the counter results in the setting of an Individual Interrupt Flag and re-initialization of the counter.

The second major difference between the Single-Shot and Continuous modes is that the internal counter enable is not dependent on the Gate input level remaining in the low state for the Single-Shot mode.

Another special condition is introduced in the Single-Shot mode. If $L=M=0$ (Dual 8-bit) or $N=0$ (Single 16-bit), the output goes low on the first clock received during or after Counter Initialization. The output remains low until the Operating Mode is changed or nonzero data is written into the Counter Latches. Time Outs continue to occur at the end of each clock period.

TABLE 6 — SINGLE-SHOT OPERATING MODES

Synthesis Modes		SINGLE-SHOT MODE (CRX3 = 0, CRX7 = 1, CRX5 = 1)	
Control Register		Initialization/Output Waveforms	
CRX2	CRX4	Counter Initialization	Timer Output (OX)
0	0	$\bar{G}_i + W + R$	
0*	1	$\bar{G}_i + R$	
1	0	$\bar{G}_i + W + R$	
1	1	$\bar{G}_i + R$	

Symbols are as defined in Table 5.

The three differences between Single-Shot and Continuous Timer Mode can be summarized as attributes of the Single-Shot mode:

1. Output is enabled for only one pulse until it is reinitialized.
2. Counter Enable is independent of Gate.
3. $L = M = 0$ or $N = 0$ disables output.

Aside from these differences, the two modes are identical.

WAVE MEASUREMENT MODES

TIME INTERVAL MODES — The Time Interval Modes are the Frequency (period) Measurement and Pulse Width Comparison Modes, and are provided for those applications which require more flexibility of interrupt generation and Counter Initialization. Individual Interrupt Flags are set in these modes as a function of both Counter Time Out and transitions of the Gate input. Counter Initialization is also affected by Interrupt Flag status.

A timer's output is normally not used in a Wave Measurement mode, but it is defined. If the output is enabled, it will operate as follows. During the period between reinitialization of the timer and the first Time Out, the output will be a logical zero. If the first Time Out is completed (regardless of its method of generation), the output will go high. If further TO's occur, the output will change state at each completion of a Time-Out.

The counter does operate in either Single 16-bit or Dual 8-bit modes as programmed by CRX2. Other features of the Wave Measurement Modes are outlined in Table 7.

Frequency Comparison Or Period Measurement Mode (CRX3=1, CRX4=0) — The Frequency Comparison Mode with CRX5=1 is straightforward. If Time Out occurs prior to the first negative transition of the Gate input after a Counter Initialization cycle, and Individual Interrupt Flag is set. The counter is disabled, and a Counter Initialization cycle cannot begin until the interrupt flag is cleared and a negative transition on $\bar{G}$ is detected.

If CRX5=0, as shown in Tables 7 and 8, an interrupt is generated if Gate input returns low prior to a Time Out. If a Counter Time Out occurs first, the counter is recycled and continues to decrement. A bit is set within the timer on the initial Time Out which precludes further individual interrupt

generation until a new Counter Initialization cycle has been completed. When this internal bit is set, a negative transition of the Gate input starts a new Counter Initialization cycle. (The condition of $\bar{G} \cdot \bar{T} \cdot TO$ is satisfied, since a Time Out has occurred and no individual Interrupt has been generated.)

Any of the timers within the PTM may be programmed to compare the period of a pulse (giving the frequency after calculations) at the Gate input with the time period requested for Counter Time Out. A negative transition of the Gate Input enables the counter and starts a Counter Initialization cycle — provided that other conditions, as noted in Table 8, are satisfied. The counter decrements on each clock signal recognized during or after Counter Initialization until an Interrupt is generated, a Write.Timer Latches command is issued, or a Timer Reset condition occurs. It can be seen from Table 8 that an interrupt condition will be generated if CRX5=0 and the period of the pulse (single pulse or measured separately repetitive pulses) at the Gate input is less than the Counter Time Out period. If CRX5=1, an interrupt is generated if the reverse is true.

Assume now with CRX5=1 that a Counter Initialization has occurred and that the Gate input has returned low prior to Counter Time Out. Since there is no Individual Interrupt Flag generated, this automatically starts a new Counter Initialization Cycle. The process will continue with frequency comparison being performed on each Gate input cycle until the mode is changed, or a cycle is determined to be above the predetermined limit.

Pulse Width Comparison Mode (CRX3=1, CRX4=1) — This mode is similar to the Frequency Comparison Mode except for a positive, rather than negative, transition of the Gate input terminates the count. With CRX5=0, an Individual Interrupt Flag will be generated if the zero level pulse applied to the Gate input is less than the time period required for Counter Time Out. With CRX5=1, the interrupt is generated when the reverse condition is true.

As can be seen in Table 8, a positive transition of the Gate input disables the counter. With CRX5=0, it is therefore possible to directly obtain the width of any pulse causing an interrupt. Similar data for other Time Interval Modes and conditions can be obtained, if two sections of the PTM are dedicated to the purpose.

FIGURE 7 — OUTPUT DELAY

CRX3 = 1			
CRX4	CRX5	Application	Condition for Setting Individual Interrupt Flag
0	0	Frequency Comparison	Interrupt Generated if Gate Input Period (1/F) is less than Counter Time Out (TO)
0	1	Frequency Comparison	Interrupt Generated if Gate Input Period (1/F) is greater than Counter Time Out (TO)
1	0	Pulse Width Comparison	Interrupt Generated if Gate Input "Down Time" is less than Counter Time Out (TO)
1	1	Pulse Width Comparison	Interrupt Generated if Gate Input "Down Time" is greater than Counter Time Out (TO)

TABLE 8 — FREQUENCY COMPARISON MODE

Mode	Bit 3	Bit 4	Control Reg. Bit 5	Counter Initialization	Counter Enable Flip-Flop Set (CE)	Counter Enable Flip-Flop Reset (CE)	Interrupt Flag Set (I)
Frequency	1	0	0	$\overline{GI} \cdot \overline{I} + (CE + TO) + R$	$\overline{GI} \cdot W \cdot R \cdot \overline{I}$	$W + R + I$	$\overline{GI}$ Before TO
Comparison	1	0	1	$\overline{GI} \cdot \overline{I} + R$	$\overline{GI} \cdot W \cdot R \cdot \overline{I}$	$W + R + I$	TO Before $\overline{GI}$
Pulse Width	1	1	0	$\overline{GI} \cdot \overline{I} + R$	$\overline{GI} W \cdot R \cdot \overline{I}$	$W + R + I + G$	$\overline{GI}$ Before TO
Comperison	1	1	1	$\overline{GI} \cdot \overline{I} + R$	$\overline{GI} \cdot W \cdot R \cdot \overline{I}$	$W + R + I + G$	$\overline{GI}$ Before TO

$\overline{GI}$ = Negative transition of Gate input.

W = Write Timer Latches Command.

R = Timer Reset (CR10 = 1 or External RESET = 0)

N = 16-Bit Number in Counter Latch.

TO = Counter Time Out (All Zero Condition)

I = Interrupt for a given timer.

*All time intervals shown above assume the Gate ($\overline{GI}$) and Clock ($\overline{CI}$) signals are synchronized to the system clock (E) with the specified setup and hold time requirements.



MOTOROLA

SYNCHRONOUS SERIAL DATA ADAPTER (SSDA)

The MC6852 Synchronous Serial Data Adapter provides a bidirectional serial interface for synchronous data information interchange. It contains interface logic for simultaneously transmitting and receiving standard synchronous communications characters in bus organized systems such as the M6800 Microprocessor systems.

The bus interface of the MC6852 includes select, enable, read/write, interrupt, and bus interface logic to allow data transfer over an 8-bit bidirectional data bus. The parallel data of the bus system is serially transmitted and received by the synchronous data interface with synchronization, fill character insertion/deletion, and error checking. The functional configuration of the SSDA is programmed via the data bus during system initialization. Programmable control registers provide control for variable word lengths, transmit control, receive control, synchronization control, and interrupt control. Status, timing and control lines provide peripheral or modem control.

Typical applications include floppy disk controllers, cassette or cartridge tape controllers, data communications terminals, and numerical control systems.

- Programmable Interrupts from Transmitter, Receiver, and Error Detection Logic
- Character Synchronization on One- or Two-Sync Codes
- External Synchronization Available for Parallel-Serial Operation
- Programmable Sync Code Register
- Up to 1.5 MHz Transmission
- Peripheral/Modem Control Functions
- Three Bytes of FIFO Buffering on Both Transmit and Receive
- 7-, 8-, or 9-Bit Transmission
- Optional Even and Odd Parity
- Parity, Overrun, and Underflow Status

MC6852

(1.0 MHz)

MC68A52

(1.5 MHz)

MC68B52

(2.0 MHz)

MOS

(N-CHANNEL, SILICON-GATE)

**SYNCHRONOUS SERIAL
DATA ADAPTER**



P SUFFIX
PLASTIC PACKAGE
CASE 709

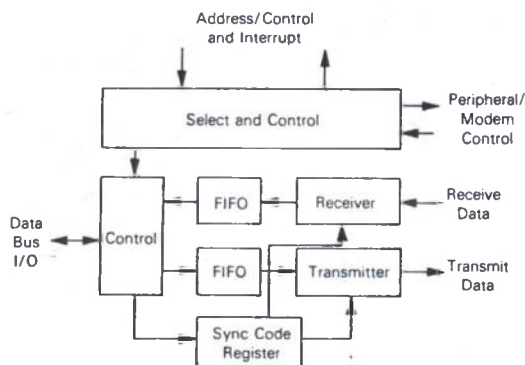


L SUFFIX
CERAMIC PACKAGE
CASE 716



S SUFFIX
CERDIP PACKAGE
CASE 623

SYNCHRONOUS SERIAL DATA ADAPTER BLOCK DIAGRAM



PIN ASSIGNMENT

VSS	1	24	CTS
Rx Data	2	23	DCD
Rx CLK	3	22	D0
Tx CLK	4	21	D1
SM/DTR	5	20	D2
Tx Data	6	19	D3
IRQ	7	18	D4
TUF	8	17	D5
RESET	9	16	D6
CS	10	15	D7
RS	11	14	E
VCC	12	13	R/W

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{in}	-0.3 to +7.0	V
Operating Temperature Range MC6852, MC68A52, MC68B52 MC6852C, MC68A52C	T_A	T_L to T_H 0 to +70 -40 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Plastic Package	θ_{JA}	120	°C/W
Ceramic Package		60	
Cerdip Package		65	

POWER CONSIDERATIONS

The average chip-junction temperature, T_J , in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

P_{PORT} = Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K + (T_J + 273^\circ\text{C}) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D(T_A + 273^\circ\text{C}) + \theta_{JA} \cdot P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A .

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ Vdc} \pm 5\%$, $V_{SS} = 0$, $T_A = T_L$ to T_H unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	$V_{SS} + 2.0$	—	—	V
Input Low Voltage	V_{IL}	—	—	$V_{SS} + 0.8$	V
Input Leakage Current ($V_{in} = 0$ to 5.25 V) Tx CLK, Rx CLK, Rx Data, Enable, RESET, RS, R/W, CS, DCD, CTS	I_{in}	—	1.0	2.5	μA
Three-State (Off-State) Input Current ($V_{in} = 0.4$ to 2.4 V, $V_{CC} = 5.25$ V) D0-D7	I_{IZ}	—	2.0	10	μA
Output High Voltage ($I_{Load} = -205 \mu\text{A}$, Enable Pulse Width < 25 μs) ($I_{Load} = -100 \mu\text{A}$, Enable Pulse Width < 25 μs) D0-D7 Tx Data, DTR, TUF	V_{OH}	$V_{SS} + 2.5$ $V_{SS} + 2.4$	— —	— —	V
Output Low Voltage ($I_{Load} = 1.6 \text{ mA}$, Enable Pulse Width < 25 μs)	V_{OL}	—	—	$V_{SS} + 0.4$	V
Output Leakage Current (Off-State) ($V_{OH} = 2.4 \text{ V}$) D0-D7 All Other Inputs	I_{OZ}	—	1.0	10	μA
Internal Power Dissipation (Measured at $T_A = T_L$)	P_{INT}	—	300	525	mW
Input Capacitance ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0 \text{ MHz}$) D0-D7 All Other Inputs	C_{in}	—	—	12.5 7.5	pF
Output Capacitance ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0 \text{ MHz}$) Tx Data, SM/DTR, TUF IRQ	C_{out}	—	—	10 5.0	pF

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0\text{ V} \pm 5\%$, $V_{SS}=0$, $T_A=T_L$ to T_H unless otherwise noted)

Characteristic	Symbol	MC6852		MC68A52		MC68B52		Unit
		Min	Max	Min	Max	Min	Max	
Serial Clock Pulse Width, Low (Figure 1)	PW _{CL}	700	—	400	—	280	—	ns
Serial Clock Pulse Width, High (Figure 2)	PW _{CH}	700	—	400	—	280	—	ns
Serial Clock Frequency (Rx CLK, Tx CLK)	f _C	—	600	—	1000	—	1500	kHz
Receive Data Setup Time (Figure 3, 7)	t _{RDSU}	350	—	200	—	160	—	ns
Receive Data Hold Time (Figure 3)	t _{RDH}	350	—	200	—	160	—	ns
Sync Match Delay Time (Figure 3)	t _{SM}	—	1.0	—	0.666	—	0.500	μs
Clock-to-Data Delay for Transmitter (Figure 4)	t _{DD}	—	1.0	—	0.666	—	0.500	μs
Transmitter Underflow (Figures 4, 6)	t _{TUF}	—	1.0	—	0.666	—	0.500	μs
DTR Delay Time (Figure 5)	t _{DTR}	—	1.0	—	0.666	—	0.500	μs
Interrupt Request Release Time (Figure 5)	t _{IR}	—	1.6	—	1.1	—	0.850	μs
RESET Pulse Width	t _{RESET}	1.0	—	0.666	—	0.500	—	μs
CTS Setup Time (Figure 6)	t _{CTS}	200	—	150	—	120	—	ns
DCD Setup Time (Figure 7)	t _{DCD}	500	—	350	—	250	—	ns
Input Rise and Fall Times (Except Enable)	t _r , t _f	—	1.0*	—	1.0*	—	1.0*	μs

*1.0 μs or 10% of the pulse width, whichever is smaller

FIGURE 1 — CLOCK PULSE WIDTH, LOW-STATE

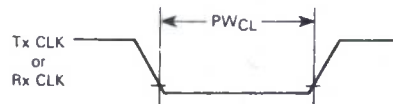


FIGURE 2 — CLOCK PULSE WIDTH, HIGH-STATE

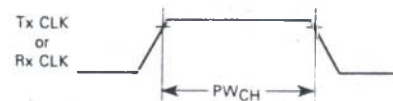
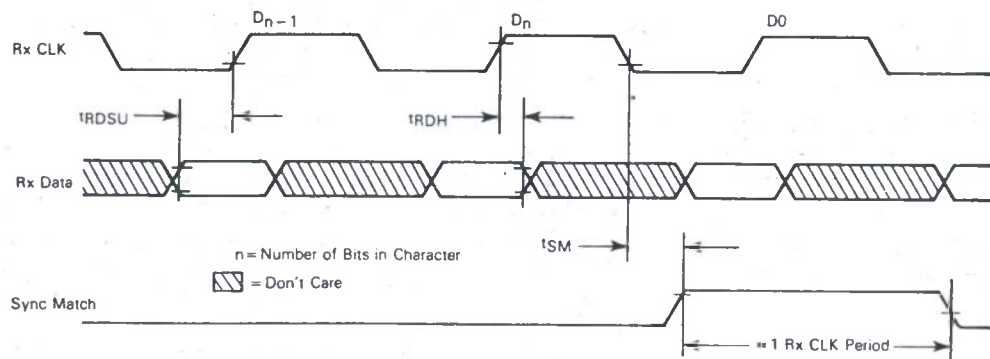


FIGURE 3 — RECEIVE DATA SETUP AND HOLD TIMES AND SYNC MATCH DELAY TIME



Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted

FIGURE 4 — TRANSMIT DATA OUTPUT DELAY AND TRANSMITTER UNDERFLOW DELAY TIME

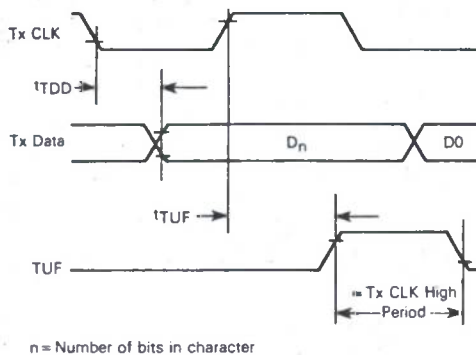


FIGURE 5 — DATA TERMINAL READY AND INTERRUPT REQUEST RELEASE TIMES

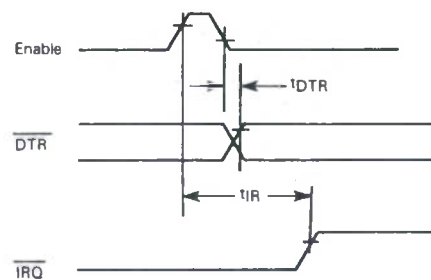


FIGURE 6 — CLEAR-TO-SEND SETUP TIME

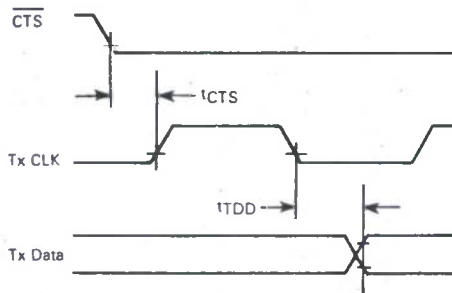
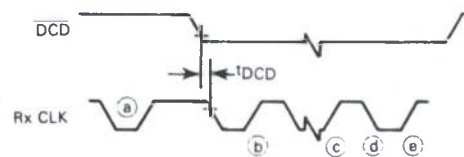


FIGURE 7 — DATA CARRIER DETECT SETUP TIME



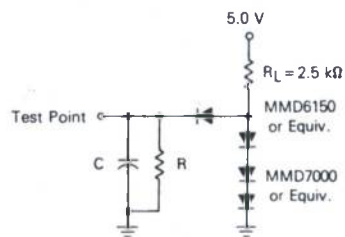
Notes:

- Must occur before $\overline{DCD}$ goes low.
- First data bit placed in Rx shift register.
- Last data bit of byte placed in Rx shift register.
- Rx data byte transferred from shift register to Rx FIFO.
- Clock edge required for generation of $\overline{IRQ}$ by RDA status.

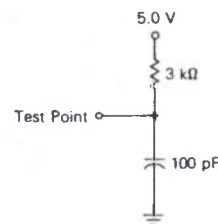
Note: Refer to Figure 3 for the Rx data setup and hold times.

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

BUS TIMING TEST LOADS

Load A
(D0-D7, $\overline{DTR}$, Tx Data, TUF)

$C = 130 \text{ pF}$ for D0-D7
 $= 30 \text{ pF}$ for $\overline{DTR}$, Tx Data, and TUF

Load B
($\overline{IRQ}$ Only)

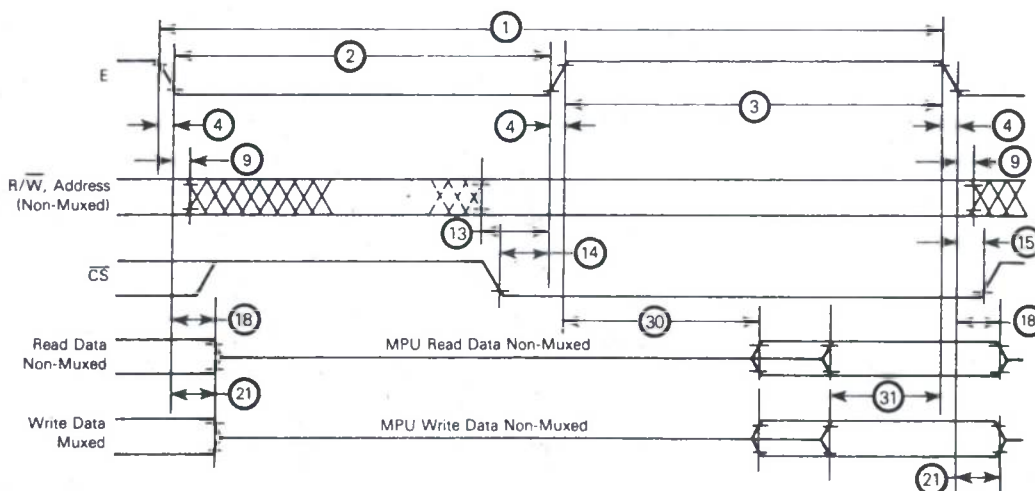
$R = 11.7 \text{ k}\Omega$ for D0-D7
 $= 24 \text{ k}\Omega$ for $\overline{DTR}$, Tx Data, and TUF

BUS TIMING CHARACTERISTICS (See Notes 1 and 2)

Indent Number	Characteristic	Symbol	MC6852		MC68A52		MC68B52		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1.0	10	0.67	10	0.5	10	μs
2	Pulse Width, E Low	PW_{EL}	430	—	280	—	210	—	ns
3	Pulse Width, E High	PW_{EH}	450	—	280	—	220	—	ns
4	Clock Rise and Fall Time	t_r, t_f	—	25	—	25	—	20	ns
9	Address Hold Time	t_{AH}	10	—	10	—	10	—	ns
13	Address Setup Time Before E	t_{AS}	80	—	60	—	40	—	ns
14	Chip Select Setup Time Before E	t_{CS}	80	—	60	—	40	—	ns
15	Chip Select Hold Time	t_{CH}	10	—	10	—	10	—	ns
18	Read Data Hold Time	t_{DHR}	20	50*	20	50*	30	50*	ns
21	Write Data Hold Time	t_{DHW}	10	—	10	—	10	—	ns
30	Output Data Delay Time	t_{DDR}	—	290	—	180	—	150	ns
31	Input Data Setup Time	t_{DSW}	165	—	80	—	60	—	ns

*The data bus output buffers are no longer sourcing or sinking current by t_{DHRmax} (High Impedance).

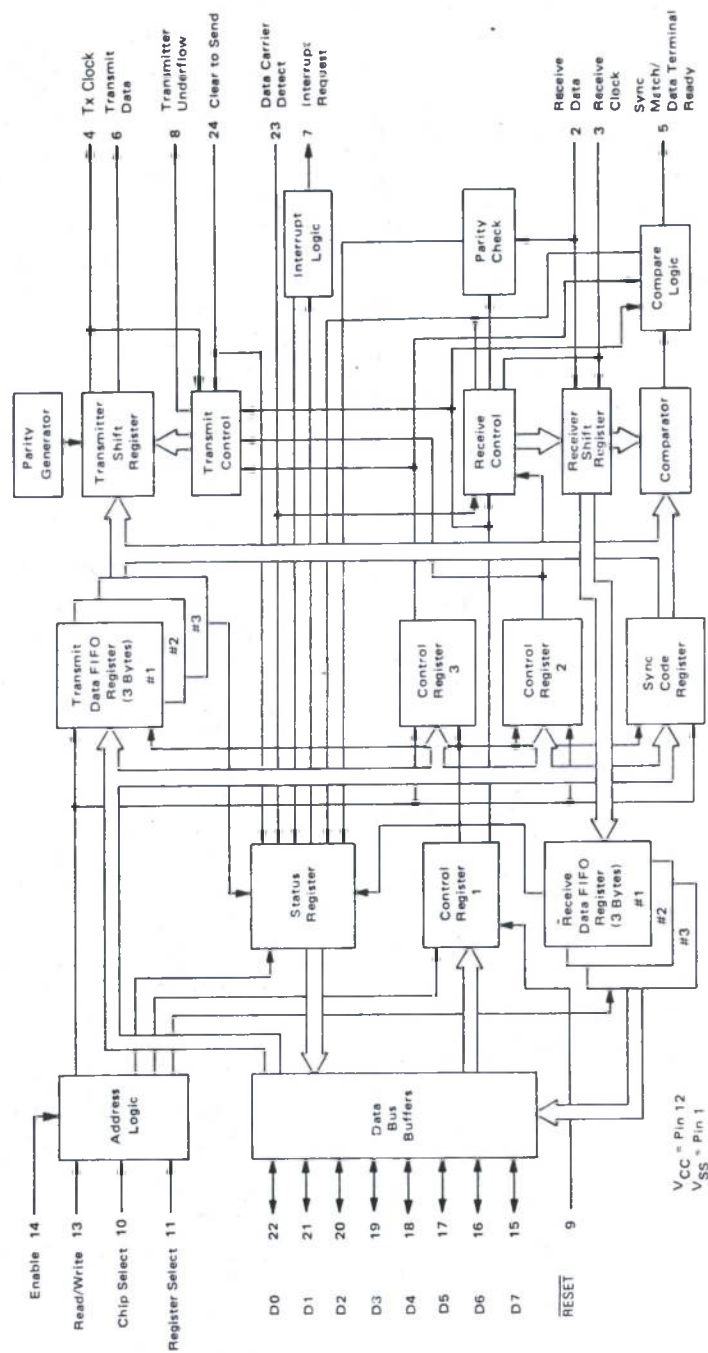
FIGURE 8 — BUS TIMING CHARACTERISTICS
(READ/WRITE INFORMATION)



Notes:

1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

EXPANDED BLOCK DIAGRAM



DEVICE OPERATION

At the bus interface, the SSDA appears as two addressable memory locations. Internally, there are seven registers: two read-only and five write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control 1, Control 2, Control 3, Sync Code and Transmit Data. The serial interface consists of serial input and output lines with independent clocks, and four peripheral/modem control lines.

Data to be transmitted is transferred directly into the 3-byte Transmit Data First-In First-Out (FIFO) Register from the data bus. Availability of the input to the FIFO is indicated by the TDRA bit in the Status Register; once data is entered, it moves through the FIFO to the last empty location. Data at the output of the FIFO is automatically transferred from the FIFO to the Transmitter Shift Register as the shift register becomes available to transmit the next character. If data is not available from the FIFO (underflow condition), the Transmitter Shift Register is automatically loaded with either a sync code or an all "1's" character. The transmit section may be programmed to append even, odd, or no parity to the transmitted word. An external control line (Clear-to-Send) is provided to inhibit the transmitter without clearing the FIFO.

Serial data is accumulated in the receiver based on the synchronization mode selected. In the external sync mode, used for parallel-serial operation, the receiver is synchronized by the DCD (Data Carrier Detect) input (Figure 9) and transfers successive bytes of data to the input of the Receiver FIFO. The single-sync-character mode requires that a match occur between the Sync Code Register and one incoming character before data transfer to the FIFO begins. The two-sync-character mode requires that two sync codes be received in sequence to establish synchronization. Subsequent to synchronization in any mode, data is accumulated in the shift register, and parity is optionally checked. An indication of parity error is carried through the Receiver FIFO with each character to the last empty location. Availability of a word at the FIFO output is indicated by the RDA status bit in the Status Register, as is a parity error (PE).

The SSDA and its internal registers are selected by RS, CS, Read/Write (R/W) and Enable control lines. To configure the SSDA, Control Registers are selected and the appropriate bits set. The Status Register is addressable for reading status.

Other I/O lines, in addition to Clear-to-Send (CTS) and Data Carrier Detect (DCD), include SM/DTR (Sync Match/Data Terminal Ready) and Transmitter Underflow (TUF). The transmitter and receiver each have individual clock inputs allowing simultaneous operation under separate clock control. Signals to the microprocessor are the Data Bus and Interrupt Request (IRQ).

INITIALIZATION

During a power-on sequence, the SSDA is reset via the RESET input and internally latched in a reset condition to prevent erroneous output transitions. The Receiver Shift Register is set to all "1's". The Sync Code Register, Control Register 2, and Control Register 3 should be programmed prior to the programmed release of the Transmitter and/or Receiver Reset bits; these bits in Control Register 1 should be cleared after the RESET line has gone high.

TRANSMITTER OPERATION

Data is transferred to the transmitter section in parallel form by means of the data bus and Transmit Data FIFO. The Transmit Data FIFO is a 3-byte register whose status is indicated by the Transmitter Data Register Available status bit (TDRA) and its associated interrupt enable bit. Data is transferred through the FIFO on negative edges of Enable (E) pulses. Two data transfer modes are provided in the SSDA. The 1-byte transfer mode provides for writing data to the transmitter section (and reading from the receiver section) one byte at a time. The 2-byte transfer mode provides for writing two data characters in succession.

Data will automatically transfer from the last register location in the Transmit Data FIFO (when it contains data) to the Transmitter Shift Register during the last half of the last bit of the previous character. A character is transferred into the Shift Register by the Transmitter Clock. Data is transmitted *LSB first*, and odd or even parity can be optionally appended. The unused bit positions in short word length characters, from the data bus, are "don't cares". (Note: The data bus inputs may be reversed for applications requiring the MSB to be transferred first, e.g., IBM format for floppy disks; however, care must be taken to properly program the control registers — Table 1 will have its bit positions reversed.)

When the Shift Register becomes empty, and data is not available for transfer from the Transmit Data FIFO, an "underflow" occurs, and a character is inserted into the transmitter data stream to maintain character synchronization. The character transmitted on underflow will be either a "Mark" (all "1's") or the contents of the Sync Code Register, depending upon the state of the Transmit Sync Code on Underflow control bit. The underflow condition is indicated by a pulse (≈ 1 Tx CLK high period) on the Underflow output (when in Tx Sync on underflow mode). The Underflow output occurs coincident with the transfer of the last half of the last bit preceding the underflow character. The Underflow status bit is set until cleared by means of the Clear Underflow control bit. This output may be used in floppy disk systems to synchronize write operations and for appending CRCs.

Transmission is initiated by clearing the Transmitter Reset bit in Control Register 1. When the Transmitter Reset bit is cleared, the first full positive half-cycle of the Transmit Clock will initiate the transmit cycle, with the transmission of data or underflow characters beginning on the negative edge of the Transmit Clock pulse which started the cycle. If the Transmit Data FIFO was not loaded, an underflow character will be transmitted (see Figure 4).

The Clear-to-Send (CTS) input provides for automatic control of the transmitter by means of external system hardware; e.g., the modem CTS output provides the control in a data communications system. The CTS input resets and inhibits the transmitter section when high, but does not reset the Transmit Data FIFO. The TDRA status bit is inhibited by CTS being high in either the one-sync character or two-sync character mode of operation. In the external sync mode, TDRA is unaffected by CTS in order to provide Transmitter Data FIFO status for preloading and operating the transmitter under the control of the CTS input. When the Transmitter Reset bit (Tx Rs) is set, the Transmit Data FIFO is cleared and the TDRA status bit is cleared. After one E clock has occurred, the Transmit Data FIFO becomes available for new data with TDRA inhibited.

RECEIVER OPERATION

Data and a presynchronized clock are provided to the SSDA receiver section by means of the Receive Data (Rx Data) and Receive Clock (Rx CLK) inputs. The data is a continuous stream of binary data bits without means for identifying character boundaries within the stream. It is, therefore, necessary to achieve character synchronization for the data at the *beginning* of the data block. Once synchronization is achieved, it is assumed to be retained for all successive characters within the block.

Data communications systems utilize the detection of sync codes during the initial portion of the preamble to establish character synchronization. This requires the detection of a single code or two successive sync codes. Floppy disk and cartridge tape units require sixteen bits of defined preamble and cassettes require eight bits of preamble to establish the reference for the start of record. All three are functionally equivalent to the detection of sync codes. Systems which do not utilize code detection techniques require custom logic external to the SSDA for character synchronization and use of the parallel-to-serial (external sync) mode. (Note: The Receiver Shift Register is set to ones when reset.)

SYNCHRONIZATION

The SSDA provides three operating modes with respect to character synchronization: one-sync-character mode, two-sync-character mode, and external sync mode. The external sync mode requires synchronization and control of the receiving section through the Data Carrier Detect (DCD) input (see Figure 7). This external synchronization could consist of direct line control from the transmitting end of the serial data link or from external logic designed to detect the start of the message block. The one-sync-character mode searches on a bit-by-bit basis until a match is achieved between the data in the Shift Register and the Sync Code Register. The match indicates character synchronization is complete and will be retained for the message block. In the two-sync-character mode, the receiver searches for the first sync code match on a bit-by-bit basis and then looks for a second *successive* sync code character prior to establishing character synchronization. If the second sync code character is not received, the bit-by-bit search for the first sync code is resumed.

Sync codes received prior to the completion of synchronization (one or two character) are not transferred to the Receive Data FIFO. Redundant sync codes during the preamble or sync codes which occur as "fill characters" can automatically be stripped from the data, when the Strip Sync control bit is set, to minimize system loading. The character synchronization will be retained until cleared by means of the Clear Sync bit, which also inhibits synchronization search when set.

RECEIVING DATA

Once synchronization has been achieved, subsequent characters are automatically transferred into the Receive Data FIFO and clocked through the FIFO to the last empty location by E pulses (MPU System $\phi 2$). The Receiver Data Available status bit (RDA) indicates when data is available to be read from the last FIFO location (#3) when in the 1-byte transfer mode. The 2-byte transfer mode causes the RDA status bit to indicate data is available when the last two FIFO

register locations are full. Data being available in the Receive Data FIFO causes an interrupt request if the Receiver Interrupt Enable (RIE) bit is set. The MPU will then read the SSDA Status Register which will indicate that data is available for the MPU read from the Receive Data FIFO register. The IRQ and RDA status bits are reset by a read from the FIFO. If more than one character has been received and is resident in the Receive Data FIFO, subsequent E clocks will cause the FIFO to update and the RDA and IRQ status bits will again be set. The read data operation for the 2-byte transfer mode requires an intervening E clock between reads to allow the FIFO data to shift. Optional parity is automatically checked as data is received, and the parity status condition is maintained with each character until the data is read from the Receive Data FIFO. Parity errors will cause an interrupt request if the Error Interrupt Enable (EIE) has been set. The parity bit is not transferred to the data bus but must be checked in the Status Register. NOTE: In the 2-byte transfer mode, parity should be checked prior to reading the second byte, since a FIFO read clears the error bit.

Other status bits which pertain to the receiver section are Receiver Overrun and Data Carrier Detect (DCD). The Overrun status bit is automatically set when a transfer of a character to the Receive Data FIFO occurs and the first register of the Receive Data FIFO is full. Overrun causes an interrupt if Error Interrupt Enable (EIE) has been set. The transfer of the overrunning character into the FIFO causes the previous character in the FIFO input register location to be lost. The Overrun status bit is cleared by reading the Status Register (when the overrun condition is present), followed by a Receive data FIFO Register read. Overrun cannot occur and be cleared without providing an opportunity to detect its occurrence via the Status Register.

A positive transition on the DCD input causes an interrupt if the EIE control bit has been set. The interrupt caused by DCD is cleared by reading the Status Register when the DCD status bit is high, followed by a Receive data FIFO read. The DCD status bit will subsequently follow the state of the DCD input when it goes low.

INPUT/OUTPUT FUNCTIONS

SSDA INTERFACE SIGNALS FOR MPU

The SSDA interfaces to the MC6800 MPU with an 8-bit bi-directional data bus, a chip-select line, a register-select line, an interrupt-request line, read/write line, an enable line, and a reset line. These signals, in conjunction with the MC6800 VMA output, permit the MPU to have complete control over the SSDA.

SSDA Bi-Directional Data (D0-D7) — The bi-directional data lines (D0-D7) allow for data transfer between the SSDA and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an SSDA read operation.

SSDA Enable (E) — The Enable signal, E, is a high-impedance TTL-compatible input that enables the bus input/output data buffers, clocks data to and from the SSDA, and moves data through the FIFO Registers.

Read/Write (R/W) — The Read/Write line is a high-impedance input that is TTL compatible and is used to control the direction of data flow through the SSDA's input/output data bus interface. When Read/Write is high (MPU read cycle), SSDA output drivers are turned on if the chip is selected and a selected register is read. When it is low, the SSDA output drivers are turned off and the MPU writes into a selected register. The Read/Write signal is also used to select read-only or write-only registers within the SSDA.

Chip Select ($\overline{CS}$) — This high-impedance TTL-compatible input line is used to address the SSDA. The SSDA is selected when $\overline{CS}$ is low. VMA should be used in generating the $\overline{CS}$ input to insure that false selects will not occur. Transfers of data to and from the SSDA are then performed under the control of the Enable signal, Read/Write, and Register Select.

Register Select (RS) — The Register Select line is a high-impedance input that is TTL compatible. A high level is used to select Control Registers C2 and C3, the Sync Code Register, and the Transmit/Receive Data Registers. A low level selects the Control 1 and Status Registers (see Table 1).

Interrupt Request ($\overline{IRQ}$) — Interrupt Request is a TTL compatible, open-drain (no internal pullup), active low output that is used to interrupt the MPU. The Interrupt Request remains low until cleared by the MPU.

RESET Input — The RESET input provides a means of resetting the SSDA from an external source. In the low state, the RESET input causes the following:

1. Receiver Reset (Rx Rs) and Transmitter Reset (Tx Rs) bits are set causing both the receiver and transmitter sections to be held in a reset condition.
2. Peripheral Control bits PC1 and PC2 are reset to zero, causing the SM/DTR output to be high.
3. The Error Interrupt Enable (EIE) bit is reset.
4. An internal synchronization mode is selected.
5. The Transmitter Data Register Available (TDRA) status bit is cleared and inhibited.
6. The Receiver Shift Register is set to 1's.

When RESET returns high (the inactive state), the transmitter and receiver sections will remain in the reset state until the Receiver Reset and Transmitter Reset bits are cleared via the data bus under software control. The control Register bits affected by RESET (Rx Rs, Tx Rs, PC1, PC2, EIE, and E/I Sync) cannot be changed when RESET is low.

CLOCK INPUTS

Separate high-impedance TTL-compatible inputs are provided for clocking of transmitted and received data.

Transmit Clock (Tx CLK) — The Transmit Clock input is used for the clocking of transmitted data. The transmitter shifts data on the negative transition of the clock.

Receive Clock (Rx CLK) — The Receive Clock input is used for clocking in received data. The clock and data must be synchronized externally. The receiver samples the data on the positive transition of the clock.

SERIAL INPUT/OUTPUT LINES

Receive Data (Rx Data) — The Receive Data line is a high-impedance TTL-compatible input through which data is received in a serial format.

Transmit Data (Tx Data) — The Transmit Data output line transfers serial data to a modem or other peripheral.

PERIPHERAL/MODEM CONTROL

The SSDA includes several functions that permit limited control of a peripheral or modem. The functions included are Clear-to-Send, Sync Match/Data Terminal Ready, Data Carrier Detect, and Transmitter Underflow.

Clear-to-Send ($\overline{CTS}$) — The $\overline{CTS}$ input provides a real-time inhibit to the transmitter section (the Tx Data FIFO is not disturbed). A positive $\overline{CTS}$ transition resets the Tx Shift Register and inhibits the TDRA status bit and its associated interrupt in both the one-sync-character and two-sync-character modes of operation. TDRA is not affected by the $\overline{CTS}$ input in the external sync mode.

The positive transition of $\overline{CTS}$ is stored within the SSDA to insure that its occurrence will be acknowledged by the system. The stored $\overline{CTS}$ information and its associated $\overline{IRQ}$ (if enabled) are cleared by writing a "1" in the Clear $\overline{CTS}$ bit in Control Register 3 or in the Transmitter Reset bit. The $\overline{CTS}$ status bit subsequently follows the $\overline{CTS}$ input when it goes low.

The $\overline{CTS}$ input provides character timing for transmitter data when in the external sync mode. Transmission is initiated on the negative transition of the first full positive clock pulse of the transmitter clock (Tx CLK) after the release of $\overline{CTS}$ (see Figure 6).

Data Carrier Detect ($\overline{DCD}$) — The $\overline{DCD}$ input provides a real-time inhibit to the receiver section (the Rx FIFO is not disturbed). A positive $\overline{DCD}$ transition resets and inhibits the receiver section except for the Receive FIFO and the RDRA status bit and its associated $\overline{IRQ}$.

The positive transition of $\overline{DCD}$ is stored within the SSDA to insure that its occurrence will be acknowledged by the system. The stored $\overline{DCD}$ information and its associated $\overline{IRQ}$ (if enabled) are cleared by reading the Status Register and then the Receiver FIFO, or by writing a "1" into the Receiver Reset bit. The $\overline{DCD}$ status bit subsequently follows the $\overline{DCD}$ input when it goes low. The $\overline{DCD}$ input provides character synchronization timing for the receiver during the external sync mode of operation. The receiver will be initialized and data will be sampled on the positive transition of the first full Receive Clock cycle after release of $\overline{DCD}$ (see Figure 7).

Sync Match/Data Terminal Ready (SM/DTR) — The SM/DTR output provides four functions (see Table 1) depending on the state of the PC1 and PC2 control bits. When the Sync Match mode is selected (PC="1", PC2="0"), the output provides a one-bit-wide pulse when a sync code is detected. This pulse occurs for each sync code match even if the receiver has already attained synchronization. The SM output is inhibited when PC2="1". The DTR mode (PC1="0") provides an output level corresponding to the complement of PC2 ($\overline{DTR}$ ="0" when PC2="1"). (See Table 1.)

TABLE 1 — SSDA PROGRAMMING MODEL

Register	Control Inputs		Address Control		Register Content							
	RS	R/W	AC2	AC1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status (S)	0	1	X	X	Interrupt Request (IRQ)	Receiver Parity Error (PE)	Receiver Overrun (Rx Ovrn)	Transmitter Underflow (TUF)	Clear-to-Send (CTS)	Data Carrier Detect (DCD)	Transmitter Data Register Available (TDRA)	Receiver Data Available (RDA)
Control 1 (C1)	0	0	X	X	Address Control 2 (AC2)	Address Control 1 (AC1)	Receiver Interrupt Enable (RIE)	Transmitter Interrupt Enable (TIE)	Clear Sync	Strip Sync Characters (Strip Sync)	Transmitter Reset (Tx Rs)	Receiver Reset (Rx Rs)
Receive Data FIFO	1	1	X	X	D7	D6	D5	D4	D3	D2	D1	D0
Control 2 (C2)	1	0	0	0	Error Interrupt Enable (EIE)	Transmit Sync Code on Underflow (Tx Sync)	Word Length Select 3 (WS3)	Word Length Select 2 (WS2)	Word Length Select 1 (WS1)	1-Byte/2-Byte Transfer (1-Byte/2-Byte)	Peripheral Control 2 (PC2)	Peripheral Control 1 (PC1)
Control 3 (C3)	1	0	0	1	Not Used	Not Used	Not Used	Not Used	Clear Transmitter Underflow Status (CTUF)	Clear CTS Status (Clear CTS)	One-Sync-Character/Two-Sync-Character Mode Control (1 Sync/2 Sync)	External/Internal Sync Mode Control (E/I Sync)
Sync Code	1	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0
Transmit Data FIFO	1	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0

X = Don't care

STATUS REGISTER

IRQ	Bit 7	The IRQ flag is cleared when the source of the IRQ is cleared. The source is determined by the enables in the Control Registers: TIE, RIE, EIE.
Bits 6-0 indicate the SSDA status at a point in time, and can be reset as follows:		
PE	Bit 6	Read Rx Data FIFO, or a "1" into Rx Rs (C1 Bit 0).
Rx Ovrn	Bit 5	Read Status and then Rx Data FIFO, or a "1" into Rx Rs (C1 Bit 0).
TUF	Bit 4	A "1" into CTUF (C3 Bit 3) or into Tx Rs (C1 Bit 1).
CTS	Bit 3	A "1" into Clear CTS (C3 Bit 2) or a "1" into Tx Rs (C1 Bit 1).
DCD	Bit 2	Read Status and then Rx Data FIFO or a "1" into Rx Rs (C1 Bit 0).
TDRA	Bit 1	Write into Tx Data FIFO.
RDA	Bit 0	Read Rx Data FIFO.

CONTROL REGISTER 1

AC2, AC1	Bits 7, 6	Used to access other registers, as shown above.
RIE	Bit 5	When "1", enables interrupt on RDA (S Bit 0).
TIE	Bit 4	When "1", enables interrupt on TDRA (S Bit 1).
Clear Sync	Bit 3	When "1", clears receiver character synchronization.
Strip Sync	Bit 2	When "1", strips all sync codes from the received data stream.
Tx Rs	Bit 1	When "1", resets and inhibits the transmitter section.
Rx Rs	Bit 0	When "1", resets and inhibits the receiver section.

CONTROL REGISTER 3

CTUF	Bit 3	When "1", clears TUF (S Bit 4), and IRQ if enabled.
Clear CTS	Bit 2	When "1", clears CTS (S Bit 3), and IRQ if enabled.
1 Sync/2 Sync	Bit 1	When "1", selects the one-sync-character mode; when "0", selects the two-sync-character mode.
E/I Sync	Bit 0	When "1", selects the external sync mode; when "0", selects the internal sync mode.

CONTROL REGISTER 2

EIE	Bit 7	When "1", enables the PE, Rx Ovrn, TUF, CTS, and DCD interrupt flags (S Bits 6 through 2).
Tx Sync	Bit 6	When "1", allows sync code contents to be transferred on underflow, and enables the TUF Status bit and output. When "0", an all mark character is transmitted on underflow.
WS3, 2, 1	Bits 5-3	Word Length Select

Bit 5 WS3	Bit 4 WS2	Bit 3 WS1	Word Length
0	0	0	6 Bits + Even Parity
0	0	1	6 Bits + Odd Parity
0	1	0	7 Bits
0	1	1	8 Bits
1	0	0	7 Bits + Even Parity
1	0	1	7 Bits + Odd Parity
1	1	0	8 Bits + Even Parity
1	1	1	8 Bits + Odd Parity

1-Byte/2-Byte	Bit 2	When "1", enables the TDRA and RDA bits to indicate when a 1-byte transfer can occur; when "0", the TDRA and RDA bits indicate when a 2-byte transfer can occur.
PC2, PC1	Bits 1-0	SM/DTR Output Control

Bit 1 PC2	Bit 0 PC1	SM/DTR Output at Pin 5
0	0	1
0	1	Pulse  1-Bit Wide, on SM
1	0	0
1	1	SM Inhibited, 0

NOTE: When the SSDA is used in applications requiring the MSB of data to be received and transmitted first, the data bus inputs to the SSDA may be reversed (D0 to D7, etc.). Caution must be used when this is done since the bit positions in this table will be reversed, and the parity should not be selected.

Transmitter Underflow (TUF) — The Underflow output indicates the occurrence of a transfer of a "fill character" to the Transmitter Shift Register when the last location (#3) in the Transmit Data FIFO is empty. The Underflow output pulse is approximately one Tx CLK high period wide and occurs during the last half of the last bit of the character preceding the "Underflow" (see Figure 4). The Underflow output pulse does not occur when the Tx Sync bit is in the reset state.

SSDA REGISTERS

Seven registers in the SSDA can be accessed by means of the data bus. The registers are defined as read-only or write-only according to the direction of information flow. The Register Select input (RS) selects two registers in each state, one being read-only and the other write-only. The Read/Write input (R/W) defines which of the two selected registers will actually be accessed. Four registers (two read-only and two write-only) can be accessed via the bus at any particular time. These registers and the required addressing are defined in Table 1.

CONTROL REGISTER 1 (C1)

Control Register 1 is an 8-bit write-only register that can be directly addressed from the data bus. Control Register 1 is accessed when RS = "0" and R/W = "0".

Receiver Reset (Rx Rs), C1 Bit 0 — The Receiver Reset control bit provides both a reset and inhibit function to the receiver section. When Rx Rs is set, it clears the receiver control logic, sync logic, error logic, Rx Data FIFO, Control, Parity Error status bit, and DCD interrupt. The Receiver Shift Register is set to ones. The Rx Rs bit must be cleared after the occurrence of a low level on RESET in order to enable the receiver section of the SSDA.

Transmitter Reset (Tx Rs), C1 Bit 1 — The Transmitter Reset control bit provides both a reset and inhibit function to the transmitter section. When Tx Rs is set, it clears the transmitter control section, Transmitter Shift Register, Tx Data FIFO Control (the Tx Data FIFO can be reloaded after one E clock pulse), the Transmitter Underflow status bit, and the CTS interrupt, and inhibits the TDRA status bit (in the one-sync-character and two-sync-character modes). The Tx Rs bit must be cleared after the occurrence of a low level on RESET in order to enable the transmitter section of the SSDA. If the Tx FIFO is not preloaded, it must be loaded immediately after the Tx Rs release to prevent a transmitter underflow condition.

Strip Synchronization Characters (Strip Sync), C1 Bit 2 — If the Strip Sync bit is set, the SSDA will automatically strip all received characters which match the contents of the Sync Code Register. The characters used for synchronization (one or two characters of sync) are always stripped from the received data stream.

Clear Synchronization (Clear Sync), C1 Bit 3 — The Clear Sync control bit provides the capability of dropping receiver character synchronization and inhibiting resynchronization. The Clear Sync bit is set to clear and inhibit receiver synchronization in all modes and is reset to zero to enable resynchronization.

Transmitter Interrupt Enable (TIE), C1 Bit 4 — TIE enables both the Interrupt Request output (IRQ) and Interrupt Request status bit to indicate a transmitter service request. When TIE is set and the TDRA status bit is high, the IRQ output will go low (the active state) and the IRQ status bit will go high.

Receiver Interrupt Enable (RIE), C1 Bit 5 — RIE enables both the Interrupt Request output (IRQ) and the Interrupt Request status bit to indicate a receiver service request. When RIE is set and the RDA status bit is high, the IRQ output will go low (the active state) and the IRQ status bit will go high.

Address Control 1 (AC1) and Address Control 2 (AC2), C1 Bits 6 and 7 — AC1 and AC2 select one of the write-only registers -- Control 2, Control 3, Sync Code, or Tx Data FIFO -- as shown in Table 1, when RS = "1" and R/W = "0".

CONTROL REGISTER 2 (C2)

Control Register 2 is an 8-bit write-only register which can be programmed from the data bus when the Address Control bits in Control Register 1 (AC1 and AC2) are reset, RS = "1" and R/W = "0".

Peripheral Control (PC1) and Peripheral Control 2 (PC2), C2 Bits 0 and 1 — Two control bits, PC1 and PC2, determine the operating characteristics of the Sync Match/DTR output. PC1, when high, selects the Sync Match mode. PC2 provides the inhibit/enable control for the SM/DTR output in the Sync Match mode. A one-bit-wide pulse is generated at the output when PC2 is "0", and a match occurs between the contents of the Sync Code Register and the incoming data even if sync is inhibited (Clear Sync bit = "1"). The Sync Match pulse is referenced to the negative edge of Rx - CLK pulse causing the match (see Figure 3).

The Data Terminal Ready (DTR) mode is selected when PC1 is low. When PC2 = "1" the SM/DTR output = "0" and vice versa. The operation of PC2 and PC1 is summarized in Table 1.

1-Byte/2-Byte Transfer (1-Byte/2-Byte), C2, Bit 2 — When 1-Byte/2-Byte is set, the TDRA and RDA status bits will indicate the availability of their respective data FIFO registers for a single-byte data transfer. Alternately, if 1-Byte/2-Byte is reset, the TDRA and RDA status bits indicate when two bytes of data can be moved without a second status read. An intervening Enable pulse must occur between data transfers.

Word Length Selects (WS1, WS2, WS3), C2 Bits 3, 4, 5 — Word Length Select bits WS1, WS2, and WS3 select word lengths of 7, 8, or 9 bits including parity as shown in Table 1.

Transmit Sync Code on Underflow (Tx Sync), C2 Bit 6 — When Tx Sync is set, the transmitter will automatically send a sync character when data is not available for transmission. If Tx Sync is reset, the transmitter will transmit a Mark character (including the parity bit position) on underflow. When the underflow is detected, a pulse approximately one Tx CLK high period wide will occur on the underflow output.

if the Tx Sync bit is set. Internal parity generation is inhibited during underflow except for sync code fill character transmission in 8-bit plus parity word lengths.

Error Interrupt Enable (EIE), C2 Bit 7 — When EIE is set, the $\overline{\text{IRQ}}$ status bit will go high and the $\overline{\text{IRQ}}$ output will go low if:

1. A receiver overrun occurs. The interrupt is cleared by reading the Status Register and reading the Rx Data FIFO.
2. DCD input has gone to a "1". The interrupt is cleared by reading the Status Register and reading the Rx Data FIFO.
3. A parity error exists for the character in the last location (#3) of the Rx Data FIFO. The interrupt is cleared by reading the Rx Data FIFO.
4. The CTS input has gone to a "1". The interrupt is cleared by writing a "1" in the Clear CTS bit, C3 bit 2, or by a Tx Reset.
5. The transmitter has underflowed (in the Tx Sync on Underflow mode). The interrupt is cleared by writing a "1" into the Clear Underflow, C3 bit 3, or Tx Reset.

When EIE is a "0", the $\overline{\text{IRQ}}$ status bit and the $\overline{\text{IRQ}}$ output are disabled for the above error conditions. A low level on the RESET input resets EIE to "0".

CONTROL REGISTER 3 (C3)

Control Register 3 is a 4-bit write-only register which can be programmed from the data bus when $\text{RS} = "1"$ and $\text{R}/\text{W} = "0"$ and Address Control bit $\text{AC1} = "1"$ and $\text{AC2} = "0"$.

External/Internal Sync Mode Control (E/I Sync), C3, Bit 0 — When the E/I Sync Mode bit is high, the SSDA is in the external sync mode and the receiver synchronization logic is disabled. Synchronization can be achieved by means of the DCD input or by starting Rx CLK at the midpoint of data bit 0 of a character with DCD low. Both the transmitter and receiver sections operate as parallel — serial converters in the External Sync mode. The Clear Sync bit in Control Register 1 acts as a receiver sync inhibit when high to provide a bus controllable inhibit. The Sync Code Register can serve as a transmitter fill character register and a receiver match register in this mode. A "low" on the RESET input resets the E/I Sync Mode bit placing the SSDA in the internal sync mode.

One-Sync-Character/Two-Sync-Character Mode Control (1-Sync/2-Sync), C3 Bit 1 — When the 1-Sync/2-Sync bit is set, the SSDA will synchronize on a single match between the received data and the contents of the Sync Code Register. When the 1-Sync/2-Sync bit is reset, two successive sync characters must be received prior to receiver synchronization. If the second sync character is not detected, the bit-by-bit search resumes from the first bit in the second character. See the description of the Sync Code Register for more details.

Clear CTS Status (Clear CTS), C3 Bit 2 — When a "1" is written into the Clear CTS bit, the stored status and interrupt are cleared. Subsequently, the CTS status bit reflects the

state of the CTS input. The Clear CTS control bit does not affect the CTS input nor its inhibit of the transmitter section. The Clear CTS command bit is self-clearing, and writing a "0" into this bit is a nonfunctional operation.

Clear Transmit Underflow Status (CTUF), C3 Bit 3 — When a "1" is written into the CTUF status bit, the CTUF bit and its associated interrupt are reset. The CTUF command bit is self-clearing and writing a "0" into this bit is a nonfunctional operation.

SYNC CODE REGISTER

The Sync Code Register is an 8-bit register for storing the programmable sync code required for received data character synchronization in the one-sync-character and two-sync-character modes. The Sync Code Register also provides for stripping the sync/fill characters from the received data (a programmable option) as well as automatic insertion of fill characters in the transmitted data stream. The Sync Code Register is not utilized for receiver character synchronization in the external sync mode; however, it provides storage of receiver match and transmit fill characters.

The Sync Code Register can be loaded when AC2 and AC1 are a "1" and "0", respectively, and $\text{R}/\text{W} = "0"$ and $\text{RS} = "1"$.

The Sync Code Register may be changed after the detection of a match with the received data (the first sync code having been detected) to synchronize with a double-word sync pattern. (This sync code change must occur prior to the completion of the second character.) The sync match (SM) output can be used to interrupt the MPU system to indicate that the first eight bits have matched. The service routine would then change the sync match register to the second half of the pattern. Alternately, the one-sync-character mode can be used for sync codes for 16 or more bits by using software to check the second and subsequent bytes after reading them from the FIFO.

The detection of the sync code can be programmed to appear on the Sync Match/DTR output by writing a "1" in PC1 (C2 bit 0) and a "0" in PC2 (C2 bit 1). The Sync Match output will go high for one bit time beginning at the character interface between the sync code and the next character (see Figure 3).

PARITY FOR SYNC CHARACTER

Transmitter

Transmitter does not generate parity for the sync character except 9-bit mode.

- 9-bit (8-bit + parity)...8-bit sync character + parity
- 8-bit (7-bit + parity)...8-bit sync character (no parity)
- 7-bit (6-bit + parity)...7-bit sync character (no parity)

Receiver

At Synchronization

Receiver automatically strips the sync character(s) (two sync characters if '2 sync' mode is selected) which is used to establish synchronization. Parity is not checked for these sync characters.

After Synchronization Is Established

When 'strip sync' bit is selected, the sync characters (fill characters) are stripped and parity is not checked for the stripped sync (fill) characters. When "strip sync" bit is not selected (low), the sync character is assumed to be normal data and it is transferred into FIFO after parity checking. (When non-parity format is selected, parity is not checked.)

Strip Sync (C1, Bit 2)	WS0-WS2 (Data Format) (C2, Bits 3-5)	
1	X	No transfer of sync code No parity Check of sync code
0	With Parity	*Transfer data and sync codes Parity check
0	Without Parity	*Transfer data and sync codes No parity check

*Subsequent to synchronization.

It is necessary to consider parity in the selected sync character in the following cases. Data Format is (6+parity), (7+parity), strip sync is not selected (low), and when sync code is used as a fill character after synchronization.

The transmitter sends a sync character without parity, but the receiver checks the parity as if it is normal data. Therefore, the sync character should be chosen to match the parity check selected for the receiver in this special case. See the following section for unused bit assignment in short-word length.

RECEIVE DATA FIRST-IN FIRST-OUT REGISTER (Rx Data FIFO)

The Receive Data FIFO Register consists of three 8-bit registers which are used for buffer storage of received data. Each 8-bit register has an internal status bit which monitors its full or empty condition. Data is always transferred from a full register to an adjacent empty register. The transfer from register to register occurs on E pulses. The RDA status bit will be high when data is available in the last location of the Rx Data FIFO.

In an Overrun condition, the overrunning character will be transferred into the full first stage of the FIFO register and will cause the loss of that data character. Successive overruns continue to overwrite the first register of the FIFO. This destruction of data is indicated by means of the Overrun status bit. The Overrun bit will be set when the overrun occurs and remains set until the Status Register is read, followed by a read of the Rx Data FIFO.

Unused data bits for short word lengths (including the parity bit) will appear as "0's" on the data bus when the Rx Data FIFO is read.

TRANSMIT DATA FIRST-IN FIRST-OUT REGISTER (Tx Data FIFO)

The Transmit Data FIFO Register consists of three 8-bit registers which are used for buffer storage of data to be transmitted. Each 8-bit register has an internal status bit which monitors its full or empty condition. Data is always transferred from a full register to an adjacent empty register. The transfer is clocked by E pulses.

The TDRA status bit will be high if the Tx Data FIFO is available for data.

Unused data bits for short word lengths will be handled as "don't cares." The parity bit is not transferred over the data bus since the SSDA generates parity at transmission.

When an Underflow occurs, the Underflow character will be either the contents of the Sync Code Register or an all "1's" character. The underflow will be stored in the Status Register until cleared and will appear on the Underflow output as a pulse approximately one Tx CLK high period wide.

STATUS REGISTER (S)

The Status Register is an 8-bit read-only register which provides the real-time status of the SSDA and the associated serial data channel. Reading the Status Register is a non-destructive process. The method of clearing status bits depends upon the function each bit represents and is discussed for each bit in the register.

Receiver Data Available (RDA), S Bit 0 — The Receiver Data Available status bit indicates when receiver data can be read from the Rx Data FIFO. The receiver data being present in the last register (#3) of the FIFO causes RDA to be high for the 1-byte transfer mode. The RDA bit being high indicates that the last two registers (#2 and #3) are full when in the 2-byte transfer mode. The second character can be read without a second status read (to determine that the character is available). An E pulse must occur between reads of the Rx Data FIFO to allow the FIFO to shift. Status must be read on a word-by-word basis if receiver data error checking is important. The RDA status bit is reset automatically when data is not available.

Transmitter Data Register Available (TDRA), S Bit 1 — The TDRA status bit indicates that data can be loaded into the Tx Data FIFO Register. The first register (#1) of the Tx Data FIFO being empty will be indicated by a high level in the TDRA status bit in the 1-byte transfer mode. The first two registers (#1 and #2) must be empty for TDRA to be high when in the 2-byte transfer mode. The Tx Data FIFO can be loaded with two bytes without an intervening status read; however, one E pulse must occur between loads. TDRA is inhibited by the Tx Reset or RESET. When Tx Reset is set, the Tx Data FIFO is cleared and then released on the next E clock pulse. The Tx Data FIFO can then be loaded with up to three characters of data, even though TDRA is inhibited. This feature allows preloading data prior to the release of Tx Reset. A high level on the CTS input inhibits the TDRA status bit in either sync mode of operation (one-sync-character or two-sync-character). CTS does not affect TDRA in the external sync mode. This enables the SSDA to operate under the control of the CTS input with TDRA indicating the status of the Tx Data FIFO. The CTS input does not clear the Tx Data FIFO in any operating mode.

Data Carrier Detect (DCD), S Bit 2 — A positive transition on the DCD input is stored in the SSDA until cleared by reading both Status and Rx Data FIFO. A "1" written into Rx Rs also clears the stored DCD status. The DCD status bit, when set, indicates that the DCD input has gone high. The reading of Status followed by reading of the Receive Data FIFO allows Bit 2 of subsequent Status reads to indicate the state of the DCD input until the next positive transition.

Clear-to-Send (CTS), S Bit 3 — A positive transition on the CTS input is stored in the SSDA until cleared by writing a "1" into the Clear CTS control bit or the Tx Rs bit. The CTS status bit, when set, indicates that the CTS input has gone high. The Clear CTS command (a "1" into C3 Bit 2) allows Bit 3 of subsequent Status reads to indicate the state of the CTS input until the next positive transition.

Transmitter Underflow (TUF), S Bit 4 — When data is not available for the transmitter, an underflow occurs and is so indicated in the Status Register (in the Tx Sync on underflow mode). The underflow status bit is cleared by writing a "1" into the Clear Underflow (CTUF) control bit or the Tx Rs bit. TUF indicates that a sync character will be transmitted as the next character. A TUF is indicated on the output *only* when the contents of the Sync Code Register is to be transferred (transmit sync code on underflow = "1").

Receiver Overrun (Rx Ovrn), S Bit 5 — Overrun indicates data has been received when the Rx Data FIFO is full,

resulting in data loss. The Rx Ovrn status bit is set when overrun occurs. The Rx Ovrn status bit is cleared by reading Status followed by reading the Rx Data FIFO or by setting the Rx Rs control bit.

Receiver Parity Error (PE), S Bit 6 — The parity error status bit indicates that parity for the character in the last register of the Rx Data FIFO did not agree with selected parity. The parity error is cleared when the character to which it pertains is read from the Rx Data FIFO or when Rx Rs occurs. The DCD input does not clear the Parity Error or Rx Data FIFO status bits.

Interrupt Request (IRQ), S Bit 7 — The Interrupt Request status bit indicates when the IRQ output is in the active state (IRQ output = "0"). The IRQ status bit is subject to the same interrupt enables (RIE, TIE, and EIE) as the IRQ output. The IRQ status bit simplifies status inquiries for polling systems by providing single bit indication of service requests.

CL8023

Low Power Amplifier

INTERSIL

μ A733/C, LM733/C

Differential Video Amplifier

Linear Integrated Circuits

FEATURES

- 120 MHz Bandwidth
- 250 k Ω Input Resistance
- Selectable Gains of 10, 100, and 400
- No Frequency Compensation Required

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 8 V
Differential Input Voltage	± 5 V
Common Mode Input Voltage	± 6 V
Output Current	10 mA
Internal Power Dissipation	
Metal Can	500 mW
Flatpak	570 mW
DIP	670 mW
Operating Temperature Range (Note 1)	
Military (733)	-55°C to +125°C
Commercial (733C)	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 second time limit)	300°C

Ceramic DIP

Temperature Range:
Military (-55°C to +125°C)
Commercial (0°C to +70°C)

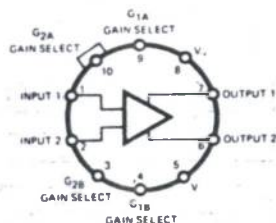
Type

Circuit

INTERSIL, INC. Circuit

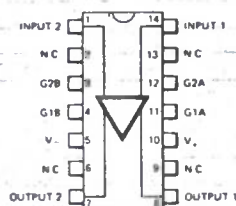
CONNECTION DIAGRAMS

10-LEAD METAL CAN
(TOP VIEW)



Note: Pin 5 connected to case.

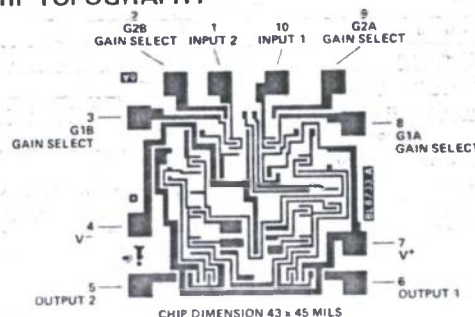
14-LEAD DIP
(TOP VIEW)



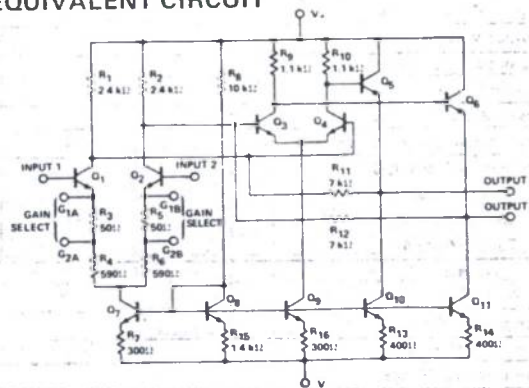
GENERAL DESCRIPTION

The 733 is a monolithic two-stage Differential Input, Differential Output Video Amplifier. Internal series-shunt feedback is used to obtain wide bandwidth, low phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. It offers fixed gains of 10, 100 or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding and in high speed thin film or plated wire memories.

CHIP TOPOGRAPHY



EQUIVALENT CIRCUIT



PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE	ORDER NUMBERS
μ A733HM	-55°C to +125°C	10 Lead Can	μ A733HM TB
μ A733HC	0°C to +70°C	10 Lead Metal Can	μ A733HC TB
μ A733DM	-55°C to +125°C	14 Lead DIP	μ A733DM DD
μ A733DC	0°C to +70°C	14 Lead DIP	μ A733DC DD
LM733H	-55°C to +125°C	10 Lead Can	LM733 TB
LM733CH	0°C to +70°C	14 Lead DIP	LM733CTB
LM733D	-55°C to +125°C	10 Lead Can	LM733 DD
LM733CD	0°C to +70°C	14 Lead DIP	LM733 CDD
LM733CN	0°C to +70°C	14 Lead DIP	LM733 CPD

733M ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_S = \pm 6.0\text{ V}$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain					
Gain 1 (Note 2)		300	400	500	
Gain 2 (Note 3)		190	100	110	
Gain 3 (Note 4)		9.0	10	11	
Bandwidth	$R_S = 50\Omega$				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	$R_S = 50\Omega, V_{OUT} = 1\text{ V}_{pp}$				
Gain 1			10.5		ns
Gain 2			4.5	10	ns
Gain 3			2.5		ns
Propagation Delay	$R_S = 50\Omega, V_{OUT} = 1\text{ V}_{pp}$				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		k Ω
Gain 2		20	30		k Ω
Gain 3			250		k Ω
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	3.0	μA
Input Bias Current			9.0	20	μA
Input Noise Voltage	$R_S = 50\Omega, BW = 1\text{ kHz to } 10\text{ MHz}$		12		μV_{rms}
Input Voltage Range		± 1.0			V
Common Mode Rejection Ratio					
Gain 2	$V_{CM} = \pm 1\text{ V}, f \leq 100\text{ kHz}$	60	86		dB
Gain 2	$V_{CM} = \pm 1\text{ V}, f = 5\text{ MHz}$		60		dB
Supply Voltage Rejection Ratio					
Gain 2	$\Delta V_S = \pm 0.5\text{ V}$	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.0	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		V_{pp}
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA

The following specifications apply for $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$

Differential Voltage Gain					
Gain 1 (Note 2)		200		600	
Gain 2 (Note 3)		80		120	
Gain 3 (Note 4)		8.0		12	
Input Resistance					
Gain 2		8.0			k Ω
Input Offset Current				5.0	μA
Input Bias Current				40	μA
Input Voltage Range		± 1.0			V
Common Mode Rejection Ratio		50			dB
Supply Voltage Rejection Ratio		50			dB
Output Offset Voltage					
Gain 1				1.5	V
Gain 2 and Gain 3				1.2	V
Output Swing		2.5			V_{pp}
Output Sink Current		2.2			mA
Positive Supply Current				27	mA

733C ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_S = \pm 6.0\text{ V}$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain					
Gain 1 (Note 2)		250	400	600	
Gain 2 (Note 3)		80	100	120	
Gain 3 (Note 4)		8.0	10	12	
Bandwidth	$R_S = 50\Omega$				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	$R_S = 50\Omega$, $V_{OUT} = 1\text{ V}_{pp}$		10.5		ns
Gain 1			4.5	12	ns
Gain 2			2.5		ns
Gain 3					ns
Propagation Delay	$R_S = 50\Omega$, $V_{OUT} = 1\text{ V}_{pp}$				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		k Ω
Gain 2		10	30		k Ω
Gain 3			250		k Ω
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	5.0	μA
Input Bias Current			9.0	30	μA
Input Noise Voltage	$R_S = 50\Omega$, BW = 1 kHz to 10 MHz		12		μV_{rms}
Input Voltage Range		± 1.0			V
Common Mode Rejection Ratio					
Gain 2	$V_{CM} = \pm 1\text{ V}$, $f \leq 100\text{ kHz}$	60	86		dB
Gain 2	$V_{CM} = \pm 1\text{ V}$, $f = 5\text{ MHz}$		60		dB
Supply Voltage Rejection Ratio					
Gain 2	$\Delta V_S = \pm 0.5\text{ V}$	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.5	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		V_{pp}
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA
The following specifications apply for $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$					
Differential Voltage Gain					
Gain 1 (Note 2)		250		600	
Gain 2 (Note 3)		80		120	
Gain 3 (Note 4)		8.0		12	
Input Resistance—Gain 2		8.0			k Ω
Input Offset Current				6.0	μA
Input Bias Current				40	μA
Input Voltage Range		± 1.0			V
Common Mode Rejection Ratio					
Gain 2	$V_{CM} = \pm 1\text{ V}$, $f \leq 100\text{ kHz}$	50			dB
Supply Voltage Rejection Ratio					
Gain 2	$\Delta V_S = \pm 0.5\text{ V}$	50			dB
Output Offset Voltage (All Gain)				1.5	V
Output Voltage Swing		2.8			V_{pp}
Output Sink Current		2.5			mA
Power Supply Current				27	mA

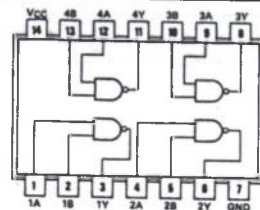
14/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

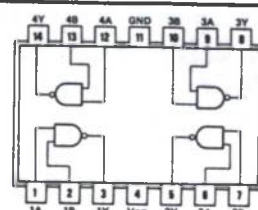
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

00

positive logic:
 $Y = \overline{AB}$



SN5400 (J) SN7400 (J, N)
SN54H00 (J) SN74H00 (J, N)
SN54L00 (J) SN74L00 (J, N)
SN54LS00 (J, W) SN74LS00 (J, N)
SN54S00 (J, W) SN74S00 (J, N)



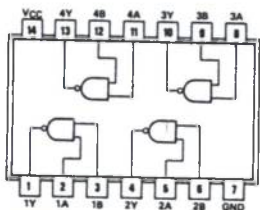
SN5400 (W)
SN54H00 (W)
SN54L00 (T)

See page 6-2

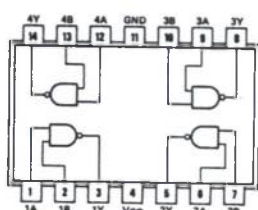
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

01

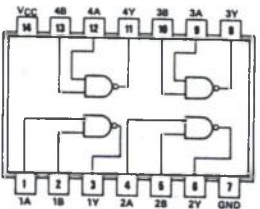
positive logic:
 $Y = \overline{AB}$



SN5401 (J) SN7401 (J, N)
SN54LS01 (J, W) SN74LS01 (J, N)



SN5401 (W)
SN54H01 (W)
SN54L01 (T)



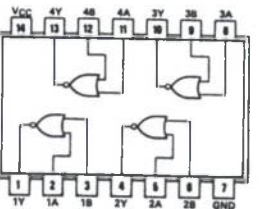
SN54H01 (J) SN74H01 (J, N)

See page 6-4

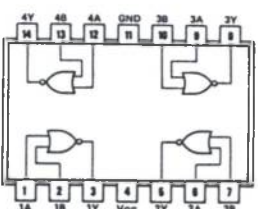
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

02

positive logic:
 $Y = \overline{A+B}$



SN5402 (J) SN7402 (J, N)
SN54H02 (J) SN74H02 (J, N)
SN54L02 (J) SN74L02 (J, N)
SN54LS02 (J, W) SN74LS02 (J, N)
SN54S02 (J, W) SN74S02 (J, N)



SN5402 (W)
SN54L02 (T)

See page 6-8

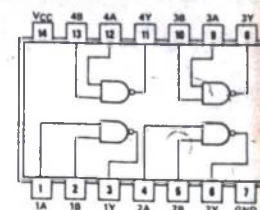
54/74 FAMILIES OF COMPATIBLE TTL CIRCUIT

PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

03

positive logic:
 $Y = \overline{AB}$



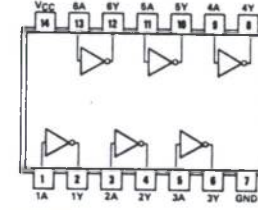
SN5403 (J) SN7403 (J, N)
SN54L03 (J) SN74L03 (J, N)
SN54LS03 (J, W) SN74LS03 (J, N)
SN54S03 (J, W) SN74S03 (J, N)

See page 6-4

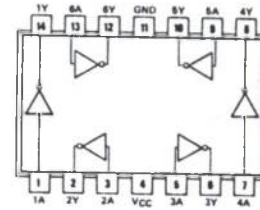
HEX INVERTERS

04

positive logic:
 $Y = \overline{A}$



SN5404 (J) SN7404 (J, N)
SN54H04 (J) SN74H04 (J, N)
SN54L04 (J) SN74L04 (J, N)
SN54LS04 (J, W) SN74LS04 (J, N)
SN54S04 (J, W) SN74S04 (J, N)



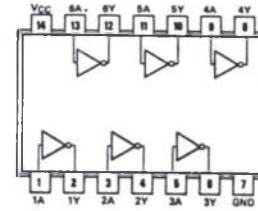
SN5404 (W)
SN54H04 (W)
SN54L04 (T)

See page 6-2

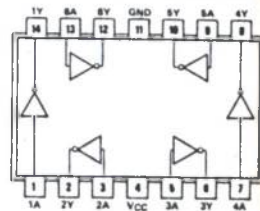
HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

05

positive logic:
 $Y = \overline{A}$



SN5405 (J) SN7405 (J, N)
SN54H05 (J) SN74H05 (J, N)
SN54L05 (J) SN74L05 (J, N)
SN54LS05 (J, W) SN74LS05 (J, N)
SN54S05 (J, W) SN74S05 (J, N)



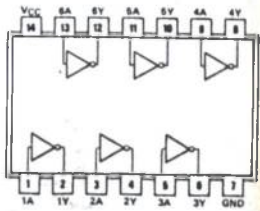
SN5405 (W)
SN54H05 (W)

See page 6-4

HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

06

positive logic:
 $Y = \overline{A}$



SN5406 (J, W) SN7406 (J, N)

See page 6-24

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

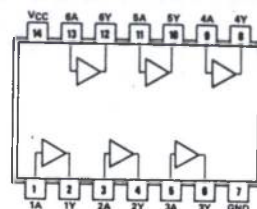
PIN ASSIGNMENTS (TOP VIEWS)

HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

07

positive logic:
 $Y = A$

See page 6-24



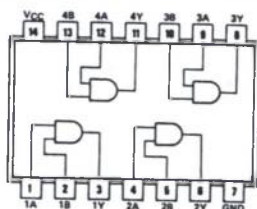
SN5407 (J, W) SN7407 (J, N)

QUADRUPLE 2-INPUT
POSITIVE-AND GATES

08

positive logic:
 $Y = AB$

See page 6-10



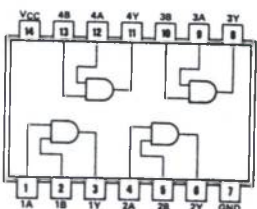
SN5408 (J, W) SN7408 (J, N)
SN54LS08 (J, W) SN74LS08 (J, N)
SN54S08 (J, W) SN74S08 (J, N)

QUADRUPLE 2-INPUT
POSITIVE-AND GATES
WITH OPEN-COLLECTOR OUTPUTS

09

positive logic:
 $Y = AB$

See page 6-12



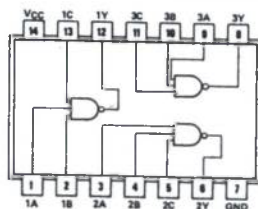
SN5409 (J, W) SN7409 (J, N)
SN54LS09 (J, W) SN74LS09 (J, N)
SN54S09 (J, W) SN74S09 (J, N)

TRIPLE 3-INPUT
POSITIVE-NAND GATES

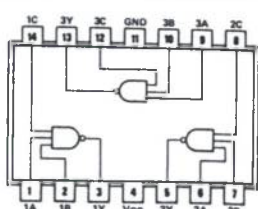
10

positive logic:
 $Y = \overline{ABC}$

See page 6-2



SN5410 (J) SN7410 (J, N)
SN64H10 (J) SN74H10 (J, N)
SN64L10 (J) SN74L10 (J, N)
SN64LS10 (J, W) SN74LS10 (J, N)
SN64S10 (J, W) SN74S10 (J, N)



SN5410 (W)
SN64H10 (W)
SN64L10 (T)

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

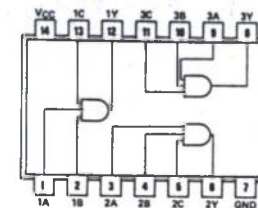
PIN ASSIGNMENTS (TOP VIEWS)

TRIPLE 3-INPUT
POSITIVE-AND GATES

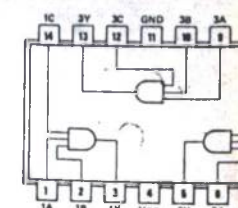
11

positive logic:
 $Y = ABC$

See page 6-10



SN54H11 (J) SN74H11 (J, N)
SN64LS11 (J, W) SN74LS11 (J, N)
SN64S11 (J, W) SN74S11 (J, N)



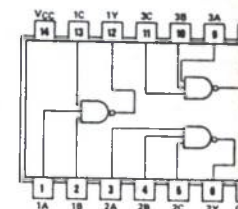
SN54H11 (W)

TRIPLE 3-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

12

positive logic:
 $Y = \overline{ABC}$

See page 6-4



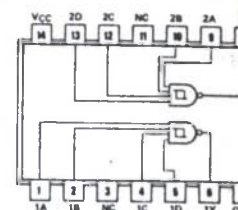
SN5412 (J, W) SN7412 (J, N)
SN64LS12 (J, W) SN74LS12 (J, N)

DUAL 4-INPUT
POSITIVE-NAND
SCHMITT TRIGGERS

13

positive logic:
 $Y = \overline{ABCD}$

See page 6-14



SN5413 (J, W) SN7413 (J, N)
SN64LS13 (J, W) SN74LS13 (J, N)

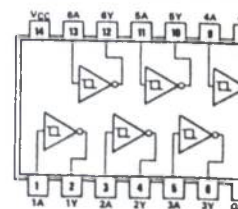
NC—No Internal connection

HEX SCHMITT-TRIGGER
INVERTERS

14

positive logic:
 $Y = \overline{A}$

See page 6-14



SN5414 (J, W) SN7414 (J, N)
SN64LS14 (J, W) SN74LS14 (J, N)

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

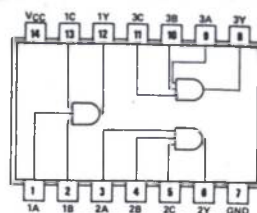
PIN ASSIGNMENTS (TOP VIEWS)

TRIPLE 3-INPUT
POSITIVE-AND GATES
WITH OPEN-COLLECTOR OUTPUTS

15

positive logic:
 $Y = ABC$

See page 6-12



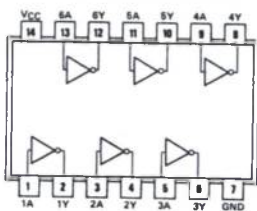
SN54H15 (J, W) SN74H15 (J, N)
SN54LS15 (J, W) SN74LS15 (J, N)
SN54S15 (J, W) SN74S15 (J, N)

HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

16

positive logic:
 $Y = \bar{A}$

See page 6-24



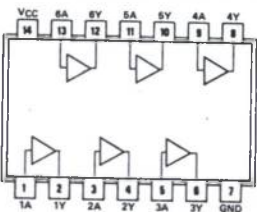
SN5416 (J, W) SN7416 (J, N)

HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

17

positive logic:
 $Y = A$

See page 6-24



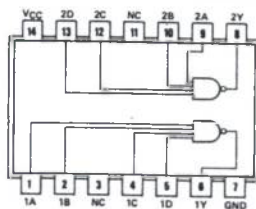
SN5417 (J, W) SN7417 (J, N)

DUAL 4-INPUT
POSITIVE-NAND GATES

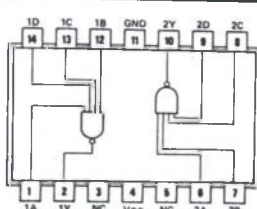
20

positive logic:
 $Y = \overline{ABCD}$

See page 6-2



SN5420 (J) SN7420 (J, N)
SN54H20 (J) SN74H20 (J, N)
SN54L20 (J) SN74L20 (J, N)
SN54LS20 (J, W) SN74LS20 (J, N)
SN54S20 (J, W) SN74S20 (J, N)



SN5420 (W)
SN54H20 (W)
SN54L20 (T)

NC—No internal connection

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

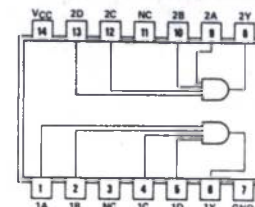
PIN ASSIGNMENTS (TOP VIEWS)

DUAL 4-INPUT
POSITIVE-AND GATES

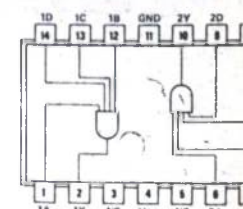
21

positive logic:
 $Y = ABCD$

See page 6-10



SN54H21 (J) SN74H21 (J, N)
SN54LS21 (J, W) SN74LS21 (J, N)



SN54H21 (W)

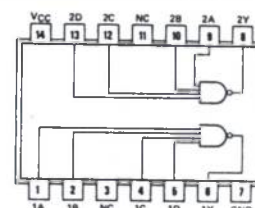
NC—No internal connection

DUAL 4-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

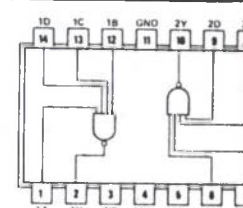
22

positive logic:
 $Y = \overline{ABCD}$

See page 6-4



SN5422 (J, W) SN7422 (J, N)
SN54H22 (J) SN74H22 (J, N)
SN54LS22 (J, W) SN74LS22 (J, N)
SN54S22 (J, W) SN74S22 (J, N)



SN54H22 (W)

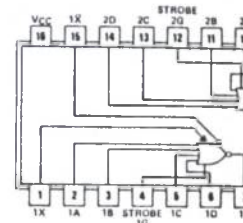
NC—No internal connection

EXPANDABLE DUAL 4-INPUT
POSITIVE-NOR GATES
WITH STROBE

23

positive logic:
 $1Y = \overline{1G(1A+1B+1C+1D)+X}$
 $2Y = \overline{2G(2A+2B+2C+2D)}$
 $X = \text{output of SN5460/SN7460}$

See page 6-39



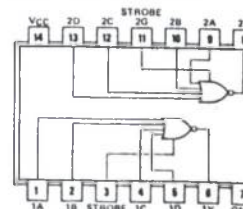
SN5423 (J, W) SN7423 (J, N)

DUAL 4-INPUT
POSITIVE-NOR GATES
WITH STROBE

25

positive logic:
 $Y = \overline{G(A+B+C+D)}$

See page 6-8



SN5425 (J, W) SN7425 (J, N)

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

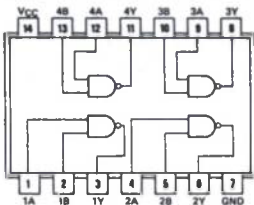
PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT
HIGH-VOLTAGE INTERFACE
POSITIVE-NAND GATES

26

positive logic:
 $Y = \overline{AB}$

See pages 6-24 and 6-26



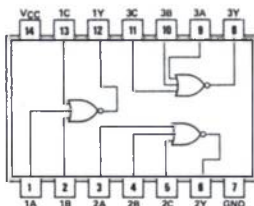
SN5426 (J) SN7426 (J, N)
SN54LS26 (J, W) SN74LS26 (J, N)

TRIPLE 3-INPUT
POSITIVE-NOR GATES

27

positive logic:
 $Y = \overline{A+B+C}$

See page 6-8



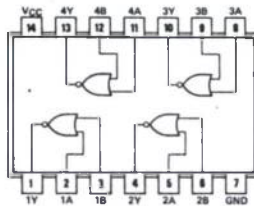
SN5427 (J, W) SN7427 (J, N)
SN54LS27 (J, W) SN74LS27 (J, N)

QUADRUPLE 2-INPUT
POSITIVE-NOR BUFFERS

28

positive logic:
 $Y = \overline{A+B}$

See page 6-20



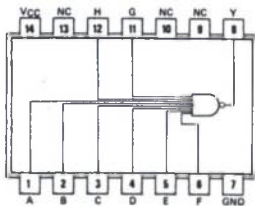
SN5428 (J, W) SN7428 (J, N)
SN54LS28 (J, W) SN74LS28 (J, N)

8-INPUT
POSITIVE-NAND GATES

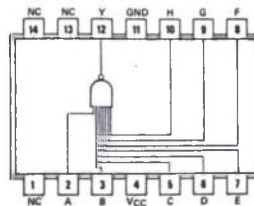
30

positive logic:
 $Y = \overline{ABCDEFGH}$

See page 6-2



SN5430 (J) SN7430 (J, N)
SN54H30 (J) SN74H30 (J, N)
SN54L30 (J) SN74L30 (J, N)
SN54LS30 (J, W) SN74LS30 (J, N)
SN54S30 (J, W) SN74S30 (J, N)



SN5430 (W)
SN54H30 (W)
SN54L30 (T)
NC—No internal connection

54/74 FAMILIES OF COMPATIBLE TTL CIRCUIT

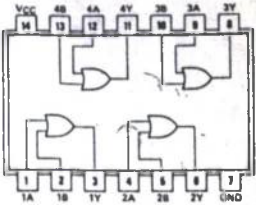
PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT
POSITIVE-OR GATES

32

positive logic:
 $Y = A+B$

See page 6-28



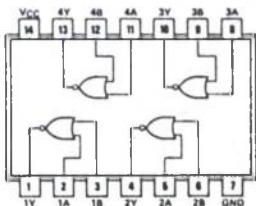
SN5432 (J, W) SN7432 (J, N)
SN54LS32 (J, W) SN74LS32 (J, N)
SN54S32 (J, W) SN74S32 (J, N)

QUADRUPLE 2-INPUT
POSITIVE-NOR BUFFERS
WITH OPEN-COLLECTOR OUTPUTS

33

positive logic:
 $Y = \overline{A+B}$

See pages 6-24 and 6-26



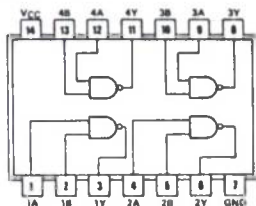
SN5433 (J, W) SN7433 (J, N)
SN54LS33 (J, W) SN74LS33 (J, N)

QUADRUPLE 2-INPUT
POSITIVE-NAND BUFFERS

37

positive logic:
 $Y = \overline{AB}$

See page 6-20



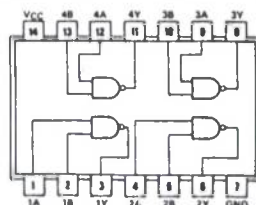
SN5437 (J, W) SN7437 (J, N)
SN54LS37 (J, W) SN74LS37 (J, N)
SN54S37 (J, W) SN74S37 (J, N)

QUADRUPLE 2-INPUT
POSITIVE-NAND BUFFERS
WITH OPEN-COLLECTOR OUTPUTS

38

positive logic:
 $Y = \overline{AB}$

See pages 6-24 and 6-26



SN5438 (J, W) SN7438 (J, N)
SN54LS38 (J, W) SN74LS38 (J, N)
SN54S38 (J, W) SN74S38 (J, N)

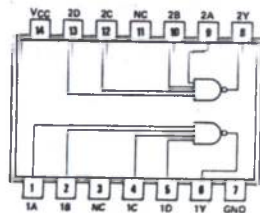
74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

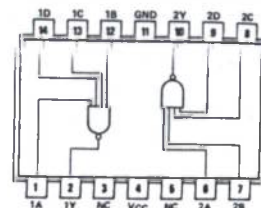
DUAL 4-INPUT
POSITIVE-NAND BUFFERS

40

positive logic:
Y = ABCD



SN5440 (J) SN7440 (J, N)
SN54H40 (J) SN74H40 (J, N)
SN54LS40 (J, W) SN74LS40 (J, N)
SN54S40 (J, W) SN74S40 (J, N)



SN5440 (W)
SN54H40 (W)

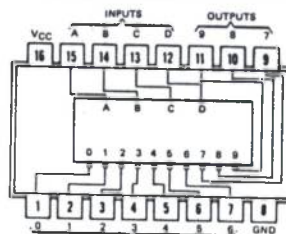
NC—No internal connection

4 LINE-TO-10-LINE DECODERS

42 BCD-TO-DECIMAL

43 EXCESS-3-TO-DECIMAL

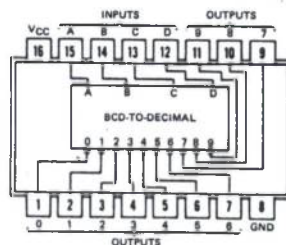
44 EXCESS-3-GRAY-TO-DECIMAL



SN5442A (J, W) SN7442A (J, N)
SN54L42 (J) SN74L42 (J, N)
SN54LS42 (J, W) SN74LS42 (J, N)
SN5443A (J, W) SN7443A (J, N)
SN54L43 (J) SN74L43 (J, N)
SN5444A (J, W) SN7444A (J, N)
SN54L44 (J) SN74L44 (J, N)

BCD-TO-DECIMAL DECODER/DRIVER

45 LAMP, RELAY, OR MOS DRIVER
80-mA CURRENT SINK
OUTPUTS OFF FOR INVALID CODES



SN5445 (J, W) SN7445 (J, N)

See page 7-20

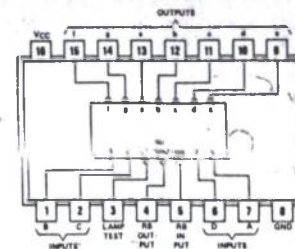
54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

46 ACTIVE-LOW, OPEN-COLLECTOR, 30-V OUTPUTS

47 ACTIVE-LOW, OPEN-COLLECTOR, 15-V OUTPUTS

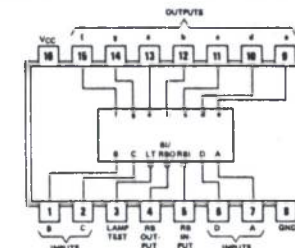


SN5446A (J, W) SN7446A (J, N)
SN54L46 (J) SN74L46 (J, N)
SN5447A (J, W) SN7447A (J, N)
SN54L47 (J) SN74L47 (J, N)
SN54LS47 (J, W) SN74LS47 (J, N)

See page 7-22

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

48 INTERNAL PULL-UP OUTPUTS

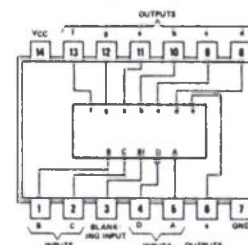


SN5448 (J, W) SN7448 (J, N)
SN54LS48 (J, W) SN74LS48 (J, N)

See page 7-22

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

49 OPEN-COLLECTOR OUTPUTS



SN5449 (W)
SN54LS49 (J, W) SN74LS49 (J, N)

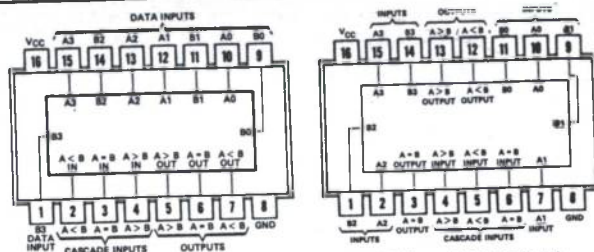
See page 7-22

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

4-BIT MAGNITUDE COMPARATORS

85

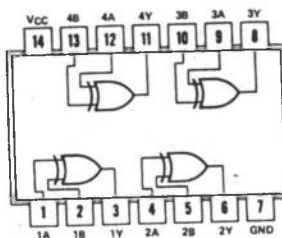


SN5485 (J, W) SN7485 (J, N)
SN54LS85 (J, W) SN74LS85 (J, N)
SN54S85 (J, W) SN74S85 (J, N)

See page 7-57

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

86 $Y = A \oplus B = \bar{A}B + A\bar{B}$



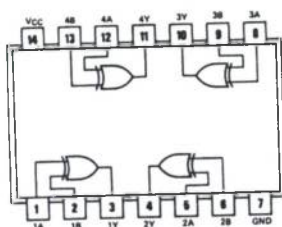
SN5486 (J, W) SN7486 (J, N)
SN54LS86 (J, W) SN74LS86 (J, N)
SN54S86 (J, W) SN74S86 (J, N)

FUNCTION TABLE

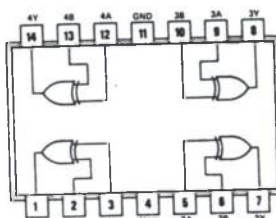
INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

See page 7-65



SN54L86 (J) SN74L86 (J, N)



SN54L86 (T)

4-BIT TRUE/COMPLEMENT, ZERO/ONE ELEMENTS

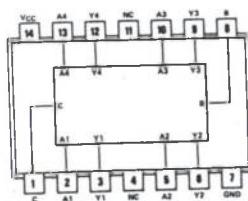
87

CONTROL INPUTS		OUTPUTS			
B	C	Y1	Y2	Y3	Y4
L	L	A1	A2	A3	A4
L	H	A1	A2	A3	A4
H	L	H	H	H	H
H	H	L	L	L	L

H = high level, L = low level

A1, A2, A3, A4 = the level of the respective A input

See page 7-70



SN54H87 (J, W) SN74H87 (J, N)
NC—No internal connection

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

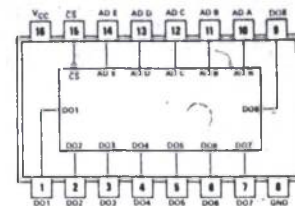
PIN ASSIGNMENTS (TOP VIEWS)

256-BIT READ-ONLY MEMORIES

88

32 8-BIT WORDS
OPEN-COLLECTOR OUTPUTS

See Bipolar Microcomputer Components Data Book, LCC4270



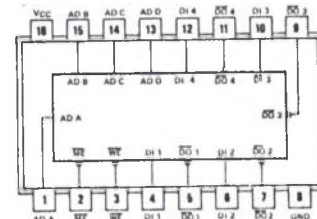
SN5488A (J, W) SN7488A (J, N)

64-BIT READ/WRITE MEMORIES

89

16 4-BIT WORDS

See Bipolar Microcomputer Components Data Book, LCC4270



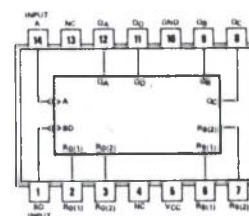
SN7489 (J, N)

DECADE COUNTERS

90

DIVIDE-BY-TWO AND DIVIDE-BY FIVE

See Page 7-72



SN5490A (J, W) SN7490A (J, N)
SN54L90 (J, T) SN74L90 (J, N)
SN54LS90 (J, W) SN74LS90 (J, N)

NC—No internal connection

PIN ASSIGNMENTS (TOP VIEWS)

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

106

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	J K	Q	$\bar{Q}$
L	H	X	X X	H	L
H	L	X	X X	L	H
L	L	X	X X	H*	H*
H	H	↓	L L	Q_0	$\bar{Q}_0$
H	H	↓	L L	H	L
H	H	↓	L L	L	H
H	H	↓	H H	TOGGLE	
H	H	X	X X	Q_0	$\bar{Q}_0$

SN54H106 (J, W) SN74H106 (J, N)

See page 6-52

DUAL J-K FLIP-FLOPS WITH CLEAR

107

FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J K	Q	$\bar{Q}$	
L	X	X X	L	H	
H	↓	L L	Q_0	$\bar{Q}_0$	
H	↓	L L	H	L	
H	↓	L L	L	H	
H	↓	H H	TOGGLE		

SN54107 (J) SN74107 (J, N)
SN54LS107A (J) SN74LS107A (J, N)

See pages 6-46 and 6-56

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

108

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	J K	Q	$\bar{Q}$
L	H	X	X X	H	L
H	L	X	X X	L	H
L	L	X	X X	H*	H*
H	H	↓	L L	Q_0	$\bar{Q}_0$
H	H	↓	L L	H	L
H	H	↓	L L	L	H
H	H	↓	H H	TOGGLE	
H	H	X	X X	Q_0	$\bar{Q}_0$

SN54H108 (J, W) SN74H108 (J, N)

See page 6-52

See explanation of function tables on page 3-8.
This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

PIN ASSIGNMENTS (TOP VIEWS)

DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

109

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	J K	Q	$\bar{Q}$
L	H	X	X X	H	L
H	L	X	X X	L	H
L	L	X	X X	H*	H*
H	H	↑	L L	L	H
H	H	↑	H L	TOGGLE	
H	H	↑	L H	Q_0	$\bar{Q}_0$
H	H	↑	H H	H	L
H	H	L	X X	Q_0	$\bar{Q}_0$

SN54109 (J, W) SN74109 (J, N)
SN54LS109A (J, W) SN74LS109A (J, N)

See pages 6-46 and 6-56

AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

110

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	J K	Q	$\bar{Q}$
L	H	X	X X	H	L
H	L	X	X X	L	H
L	L	X	X X	H*	H*
H	H	↓	L L	Q_0	$\bar{Q}_0$
H	H	↓	H L	H	L
H	H	↓	L H	L	H
H	H	↓	H H	TOGGLE	

SN54110 (J, W) SN74110 (J, N)

positive logic: J = J1·J2·J3
K = K1·K2·K3

See page 6-46

NC—No internal connection

DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

111

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	J K	Q	$\bar{Q}$
L	H	X	X X	H	L
H	L	X	X X	L	H
L	L	X	X X	H*	H*
H	H	↓	L L	Q_0	$\bar{Q}_0$
H	H	↓	H L	H	L
H	H	↓	L H	L	H
H	H	↓	H H	TOGGLE	

SN54111 (J, W) SN74111 (J, N)

See page 6-46

See explanation of function tables on page 3-8.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

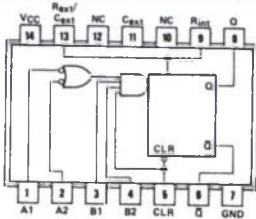
PIN ASSIGNMENTS (TOP VIEWS)

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

122 FUNCTION TABLE

CLEAR	INPUTS				OUTPUTS	
	A1	A2	B1	B2	Q	$\bar{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	↓	↑
H	L	X	H	↑	↓	↑
H	X	L	↑	H	↓	↑
H	X	L	H	↑	↓	↑
H	H	↓	H	H	↓	↑
H	↓	↓	H	H	↓	↑
H	↓	H	H	H	↓	↑
↑	L	X	H	H	↓	↑
↑	X	L	H	H	↓	↑

- NOTES: 1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
2. For accurate repeatable pulse widths, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.



SN54122 (J, W) SN74122 (J, N)
SN54L122 (J, T) SN74L122 (J, N)
SN54LS122 (J, W) SN74LS122 (J, N)
*122 ... R_{int} = 10 kΩ NOM
*L122 ... R_{int} = 20 kΩ NOM
*LS122 ... R_{int} = 10 kΩ NOM

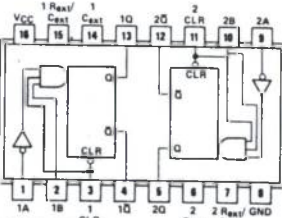
NC—No internal connection

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

123 FUNCTION TABLE

CLEAR	INPUTS		OUTPUTS	
	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	↓	↑
H	↓	↑	↓	↑
↑	L	H	↓	↑

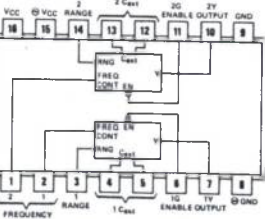
See page 6-76



SN54123 (J, W) SN74123 (J, N)
SN54L123 (J) SN74L123 (J, N)
SN54LS123 (J, W) SN74LS123 (J, N)

DUAL VOLTAGE-CONTROLLED OSCILLATORS

124



SN54LS124 (J, W) SN74LS124 (J, N)
SN54S124 (J, W) SN74S124 (J, N)

NC—No internal connection

See page 7-123

See explanation of function tables on page 3-8.

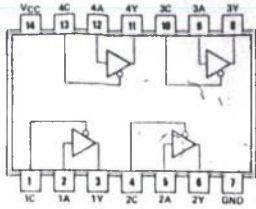
PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

125

positive logic:
Y = A
Output is off (disabled) when C is high.

See page 6-33



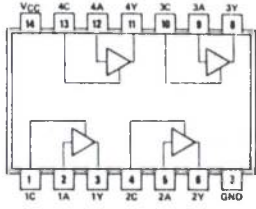
SN54125 (J, W) SN74125 (J, N)
SN54LS125A (J, W) SN74LS125A (J, N)

QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

126

positive logic:
Y = A
Output is off (disabled) when C is low.

See page 6-33



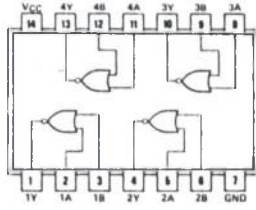
SN54126 (J, W) SN74126 (J, N)
SN54LS126A (J, W) SN74LS126A (J, N)

SN54128 ... 75-OHM LINE DRIVER
SN74128 ... 50-OHM LINE DRIVER

128

positive logic:
Y = A+B

See page 6-22



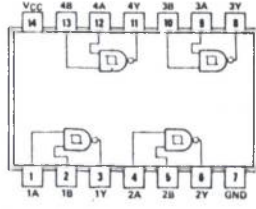
SN54128 (J, W) SN74128 (J, N)

QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

132

positive logic:
Y = AB

See page 6-14



SN54132 (J, W) SN74132 (J, N)
SN54LS132 (J, W) SN74LS132 (J, N)
SN54S132 (J, W) SN74S132 (J, N)

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

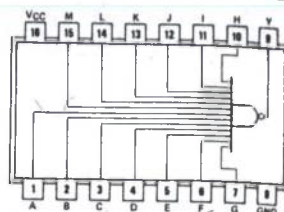
13-INPUT POSITIVE-NAND GATES

133

positive logic:

$$Y = \overline{ABCDEFGHIJKLM}$$

See page 6-2



SN54S133 (J, W) SN74S133 (J, N)

12-INPUT POSITIVE-NAND GATES WITH THREE-STATE OUTPUTS

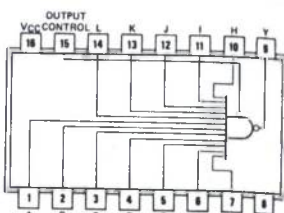
134

positive logic:

$$Y = \overline{ABCDEFGHIJKL}$$

Output is off (disabled) when output control is high.

See page 6-33



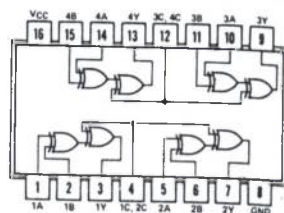
SN54S134 (J, W) SN74S134 (J, N)

QUAD EXCLUSIVE-OR/NOR GATES

135

positive logic: $Y = (A \oplus B) \oplus C = \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} + ABC$

See page 7-129



SN54S135 (J, W) SN74S135 (J, N)

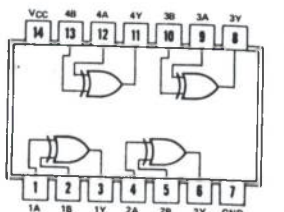
NC—No internal connection

QUAD EXCLUSIVE-OR GATES

136

positive logic: $Y = A \oplus B = \overline{A}\overline{B} + A\overline{B}$

See page 7-131



SN54136 (J, W) SN74136 (J, N)
SN54LS136 (J, W) SN74LS136 (J, N)

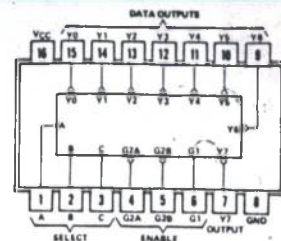
54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEW)

3-TO-8 LINE DECODERS/MULTIPLEXERS

138

See page 7-134

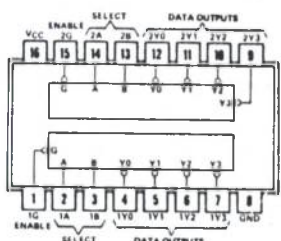


SN54LS138 (J, W) SN74LS138 (J, N)
SN54S138 (J, W) SN74S138 (J, N)

DUAL 2-TO-4 LINE DECODERS/MULTIPLEXERS

139

See page 7-134



SN54LS139 (J, W) SN74LS139 (J, N)
SN54S139 (J, W) SN74S139 (J, N)

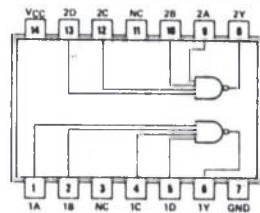
DUAL 4-INPUT POSITIVE-NAND 50-OHM LINE DRIVERS

140

positive logic:

$$Y = \overline{ABCD}$$

See page 6-22



SN54S140 (J, W) SN74S140 (J, N)

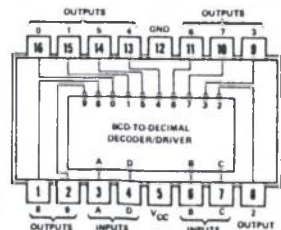
NC—No internal connection

BCD-TO-DECIMAL DECODER/DRIVER

141

DRIVES COLD-CATHODE
INDICATOR TUBES

See page 7-138



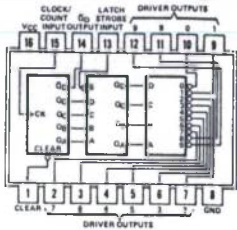
SN74141 (J, N)

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

COUNTER/LATCH/DECODER/DRIVER

142 DIVIDE-BY-10 COUNTER
4-BIT LATCH
4-BIT TO 7-SEGMENT DECODER
NIXIE ‡ TUBE DRIVER



SN74142 (J, N)

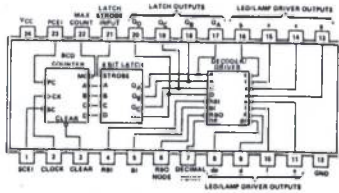
See page 7-140

‡Nixie is a registered trademark of the Burroughs Corp.

COUNTERS/LATCHES/DECODERS/DRIVERS

143 15 mA CONSTANT CURRENT
1- TO 5-V OUTPUT RANGE

144 UP TO 15-V INDICATORS
UP TO 25 mA
OPEN-COLLECTOR OUTPUT

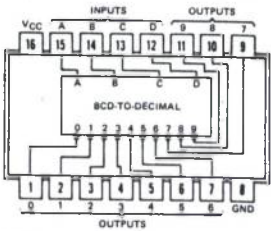


SN54143 (J, W) SN74143 (J, N)
SN54144 (J, W) SN74144 (J, N)

See page 7-143

BCD-TO-DECIMAL DECODERS/DRIVERS FOR LAMPS, RELAYS, MOS

145 BCD-TO-DECIMAL

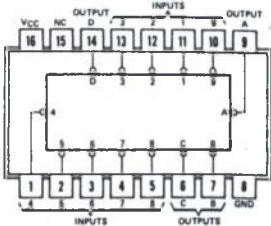


SN54145 (J, W) SN74145 (J, N)
SN54LS145 (J, W) SN74LS145 (J, W)

See page 7-148

10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODERS

147



SN54147 (J, W) SN74147 (J, N)
SN54LS147 (J, W) SN74LS147 (J, N)
NC - No internal connection

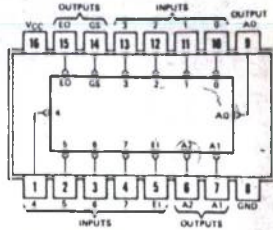
See page 7-151

54/74 FAMILIES OF COMPATIBLE TTL CIRCUIT

PIN ASSIGNMENTS (TOP VIEWS)

8-LINE-TO-3-LINE OCTAL PRIORITY ENCODERS

148

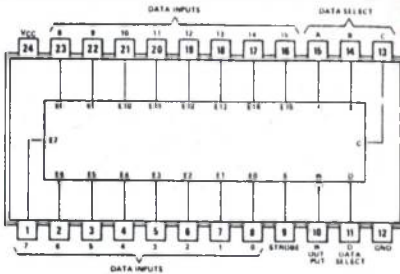


SN54148 (J, W) SN74148 (J, N)
SN54LS148 (J, W) SN74LS148 (J, N)

See page 7-151

1-OF-16 DATA SELECTORS/MULTIPLEXERS

150

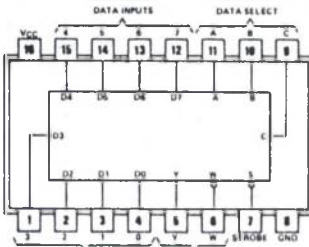


SN54150 (J, W) SN74150 (J, N)

See page 7-157

1-OF-8 DATA SELECTORS/MULTIPLEXERS

151

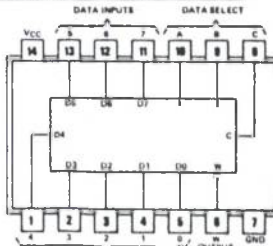


SN54151A (J, W) SN74151A (J, N)
SN54LS151 (J, W) SN74LS151 (J, N)
SN54S151 (J, W) SN74S151 (J, N)

See page 7-157

1-OF-8 DATA SELECTORS/MULTIPLEXERS

152



SN54152A (W)
SN54LS152 (W)

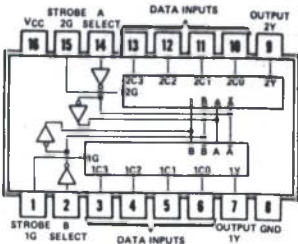
See page 7-157

4/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEW)

DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

153

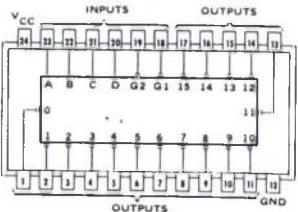


SN54153 (J, W) SN74153 (J, N)
SN54L153 (J) SN74L153 (J, N)
SN54LS153 (J, W) SN74LS153 (J, N)
SN54S153 (J, W) SN74S153 (J, N)

See page 7-165

4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS

154



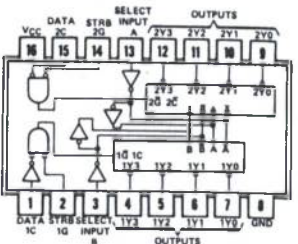
SN54154 (J, W) SN74154 (J, N)
SN54L154 (J) SN74L154 (J, N)

See page 7-171

DECODERS/DEMULTIPLEXERS

- DUAL 2- TO 4-LINE DECODER
- DUAL 1- TO 4-LINE DEMULTIPLEXER
- 3- TO 8-LINE DECODER
- 1- TO 8-LINE DEMULTIPLEXER

155 TOTEM-POLE OUTPUTS



SN54155 (J, W) SN74155 (J, N)
SN54LS155 (J, W) SN74LS155 (J, N)
SN54S155 (J, W) SN74S155 (J, N)

156 OPEN-COLLECTOR OUTPUTS

See page 7-175

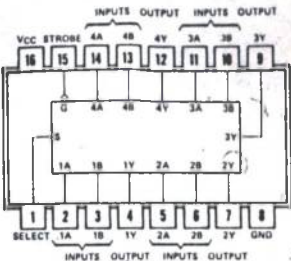
54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEW)

QUAD 2- TO 1-LINE DATA SELECTORS/MULTIPLEXERS

157 NONINVERTED DATA OUTPUTS

158 INVERTED DATA OUTPUTS

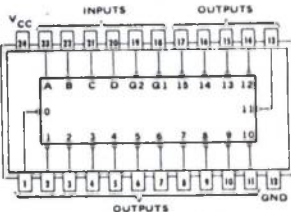


SN54157 (J, W) SN74157 (J, N)
SN54L157 (J) SN74L157 (J, N)
SN54LS157 (J, W) SN74LS157 (J, N)
SN54S157 (J, W) SN74S157 (J, N)
SN54LS158 (J, W) SN74LS158 (J, N)
SN54S158 (J, W) SN74S158 (J, N)

See page 7-181

4- TO 16-LINE DECODERS/DEMULTIPLEXERS

159 OPEN-COLLECTOR OUTPUTS

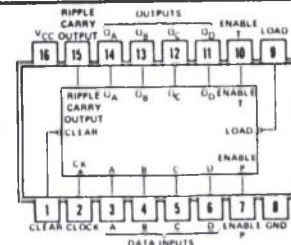


SN54159 (J, W) SN74159 (J, N)

See page 7-188

SYNCHRONOUS 4-BIT COUNTERS

- 160 DECADE, DIRECT CLEAR
- 161 BINARY, DIRECT CLEAR
- 162 DECADE, SYNCHRONOUS CLEAR
- 163 BINARY, SYNCHRONOUS CLEAR



SN54160 (J, W) SN74160 (J, N)
SN54LS160A (J, W) SN74LS160A (J, N)
SN54161 (J, W) SN74161 (J, N)
SN54LS161A (J, W) SN74LS161A (J, N)
SN54162 (J, W) SN74162 (J, N)
SN54LS162A (J, W) SN74LS162A (J, N)
SN54S162 (J, W) SN74S162 (J, N)
SN54163 (J, W) SN74163 (J, N)
SN54LS163A (J, W) SN74LS163A (J, N)
SN54S163 (J, W) SN74S163 (J, N)

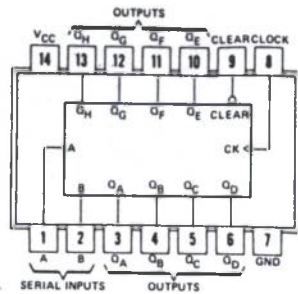
See page 7-190

14/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

8-BIT PARALLEL OUTPUT SERIAL SHIFT REGISTERS

164 ASYNCHRONOUS CLEAR

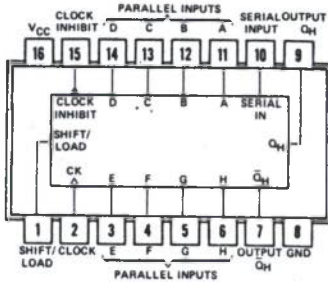


SN54164 (J, W) SN74164 (J, N)
SN54L164 (J, T) SN74L164 (J, N)
SN54LS164 (J, W) SN74LS164 (J, N)

See page 7-206

PARALLEL-LOAD 8-BIT SHIFT REGISTERS WITH COMPLEMENTARY OUTPUTS

165

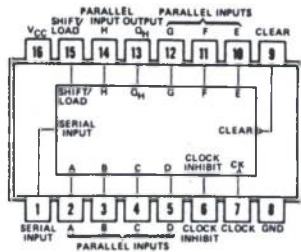


SN54165 (J, W) SN74165 (J, N)
SN54LS165 (J, W) SN74LS165 (J, N)

See page 7-212

8-BIT SHIFT REGISTERS

166 PARALLEL/SERIAL INPUT SERIAL OUTPUT



SN54166 (J, W) SN74166 (J, N)
SN54LS166 (J, W) SN74LS166 (J, N)

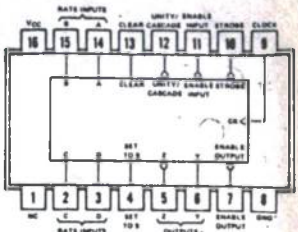
See page 7-217

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEW)

SYNCHRONOUS DECADE RATE MULTIPLIERS

167



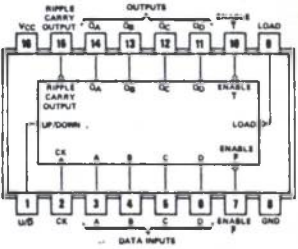
SN54167 (J, W) SN74167 (J, N)

See page 7-222

NC - No internal connection

4-BIT UP/DOWN SYNCHRONOUS COUNTERS

168 DECADE
169 BINARY

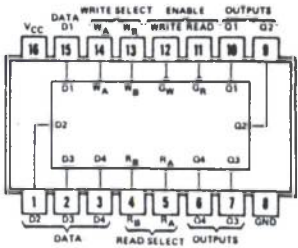


SN54LS168A (J, W) SN74LS168A (J, N)
SN54S168 (J, W) SN74S168 (J, N)
SN54LS169A (J, W) SN74LS169A (J, N)
SN54S169 (J, W) SN74S169 (J, N)

See page 7-226

4-BY-4 REGISTER FILES

170 SEPARATE READ/WRITE ADDRESSING
SIMULTANEOUS READ AND WRITE
OPEN-COLLECTOR OUTPUTS
EXPANDABLE TO 1024 WORDS



SN54170 (J, W) SN74170 (J, N)
SN54LS170 (J, W) SN74LS170 (J, N)

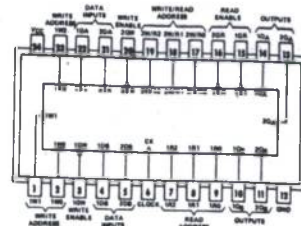
See page 7-237

74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

16-BIT REGISTER FILE

- 172** INDEPENDENT READ/WRITE ADDRESSING
SIMULTANEOUS READ/WRITE
8-WORDS OF TWO BITS EACH
3-STATE OUTPUTS

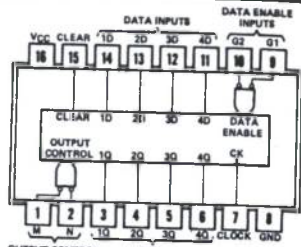


SN74172 (J, N)

See page 7-245

4-BIT D-TYPE REGISTERS

- 173** 3-STATE OUTPUTS

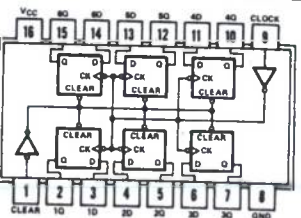


SN54173 (J, W) SN74173 (J, N)
SN54LS173 (J, W) SN74LS173 (J, N)

See page 7-249

HEX D-TYPE FLIP-FLOPS

- 174** SINGLE RAIL OUTPUTS
COMMON DIRECT CLEAR

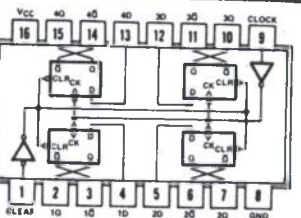


SN54174 (J, W) SN74174 (J, N)
SN54LS174 (J, W) SN74LS174 (J, N)
SN54S174 (J, W) SN74S174 (J, N)

See page 7-253

QUAD D-TYPE FLIP-FLOPS

- 175** COMPLEMENTARY OUTPUTS
COMMON DIRECT CLEAR



SN54175 (J, N) SN74175 (J, N)
SN54LS175 (J, W) SN74LS175 (J, N)
SN54S175 (J, W) SN74S175 (J, N)

See page 7-253

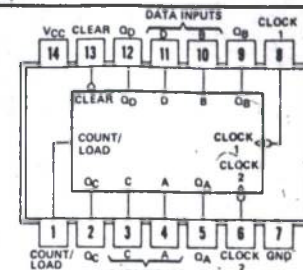
54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

PRESETABLE COUNTERS/LATCHES

- 176** DECADE (BI-QUINARY)

- 177** BINARY

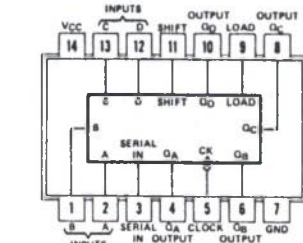


SN54176 (J, W) SN74176 (J, N)
SN54177 (J, W) SN74177 (J, N)

See page 7-259

4-BIT UNIVERSAL SHIFT REGISTERS

- 178**

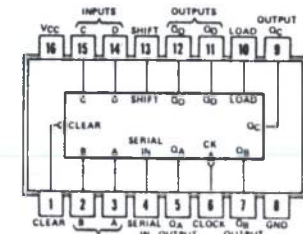


SN54178 (J, W) SN74178 (J, N)

See page 7-265

4-BIT UNIVERSAL SHIFT REGISTERS

- 179** DIRECT CLEAR
Q_D COMPLEMENTARY OUTPUTS

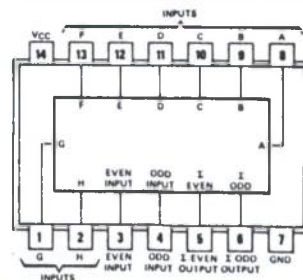


SN54179 (J, W) SN74179 (J, N)

See page 7-265

9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

- 180**



SN54180 (J, W) SN74180 (J, N)

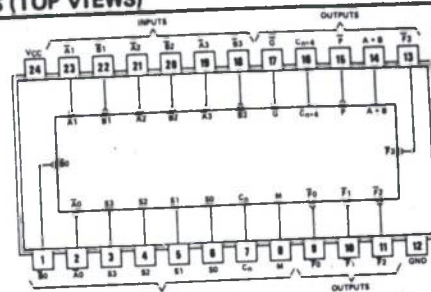
See page 7-269

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

181 16 ARITHMETIC OPERATIONS
16 LOGIC FUNCTIONS

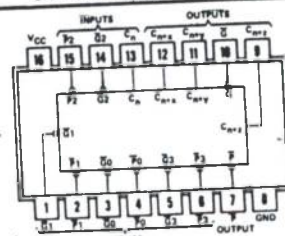


SN54181 (J, W) SN74181 (J, N)
SN54LS181 (J, W) SN74LS181 (J, N)
SN54S181 (J, W) SN74S181 (J, N)

See page 7-271

LOOK-AHEAD CARRY GENERATORS

182

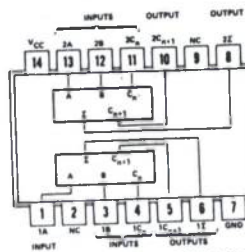


SN54182 (J, W) SN74182 (J, N)
SN54S182 (J, W) SN74S182 (J, N)

See page 7-282

DUAL CARRY-SAVE FULL ADDERS

183



SN54LS183 (J, W) SN74LS183 (J, N)
SN54H183 (J, W) SN74H183 (J, N)

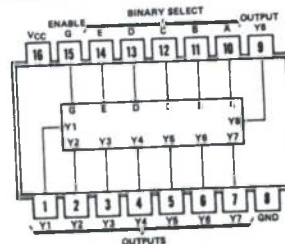
See page 7-287

CODE CONVERTERS

CASCADEABLE TO N-BITS

184 BCD-TO-BINARY

185 BINARY-TO-BCD



SN54184 (J, W) SN74184 (J, N)
SN54185A (J, W) SN74185A (J, N)

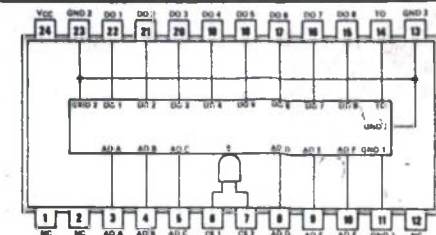
See page 7-290

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

512-BIT PROGRAMMABLE READ-ONLY MEMORIES

186 64 8-BIT WORDS
OPEN-COLLECTOR OUTPUTS



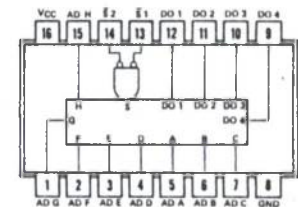
See Bipolar Microcomputer Components Data Book, LCC4270

SN54186 (J, W) SN74186 (J, N)

NC - No internal connection

1024-BIT READ-ONLY MEMORIES

187 256 4-BIT WORDS
OPEN-COLLECTOR OUTPUTS

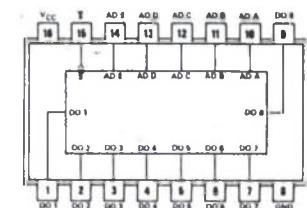


See Bipolar Microcomputer Components Data Book, LCC4270

SN54187 (J, W) SN74187 (J, N)

256-BIT PROGRAMMABLE READ-ONLY MEMORIES

188 32 8-BIT WORDS
OPEN-COLLECTOR OUTPUTS

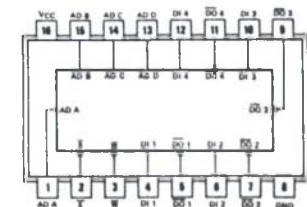


See Bipolar Microcomputer Components Data Book, LCC4270

SN54188A (J, W) SN74188A (J, N)
SN54S188 (J, W) SN74S188 (J, N)

64-BIT RANDOM-ACCESS MEMORIES

189 16 4-BIT WORDS
THREE-STATE OUTPUTS



See Bipolar Microcomputer Components Data Book, LCC4270

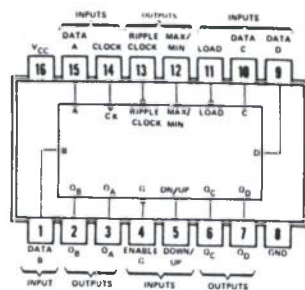
SN54S189 (J, W) SN74S189 (J, N)

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

SYNCHRONOUS UP/DOWN COUNTERS

190 BCD
191 BINARY

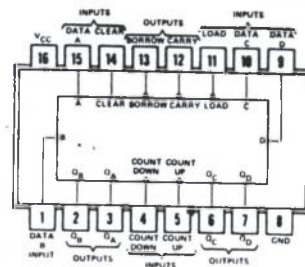


SN54190 (J, W) SN74190 (J, N)
SN54LS190 (J, W) SN74LS190 (J, N)
SN54191 (J, W) SN74191 (J, N)
SN54LS191 (J, W) SN74LS191 (J, N)

See page 7-296

SYNCHRONOUS UP/DOWN DUAL CLOCK COUNTERS

192 BCD WITH CLEAR
193 BINARY WITH CLEAR

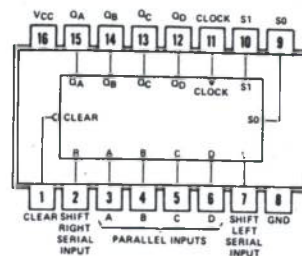


SN54192 (J, W) SN74192 (J, N)
SN54L192 (J) SN74L192 (J, N)
SN54LS192 (J, W) SN74LS192 (J, N)
SN54193 (J, W) SN74193 (J, N)
SN54L193 (J) SN74L193 (J, N)
SN54LS193 (J, W) SN74LS193 (J, N)

See page 7-306

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

194



SN54194 (J, W) SN74194 (J, N)
SN54LS194A (J, W) SN74LS194A (J, N)
SN54S194 (J, W) SN74S194 (J, N)

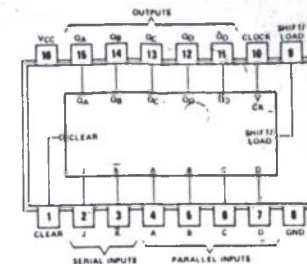
See page 7-316

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

4-BIT PARALLEL-ACCESS SHIFT REGISTERS

195

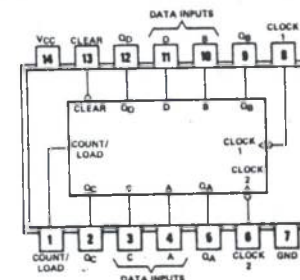


SN54195 (J, W) SN74195 (J, N)
SN54LS195A (J, W) SN74LS195A (J, N)
SN54S195 (J, W) SN74S195 (J, N)

See page 7-324

PRESETABLE COUNTERS/LATCHES

196 DECADE/BI-QUINARY
197 BINARY

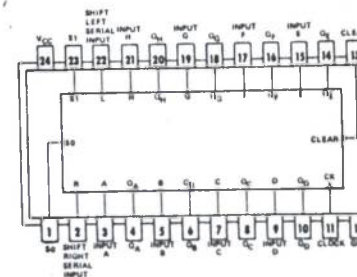


SN54196 (J, W) SN74196 (J, N)
SN54LS196 (J, W) SN74LS196 (J, N)
SN54S196 (J, W) SN74S196 (J, N)
SN54197 (J, W) SN74197 (J, N)
SN54LS197 (J, W) SN74LS197 (J, N)
SN54S197 (J, W) SN74S197 (J, N)

See page 7-331

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

198



SN54198 (J, W) SN74198 (J, N)

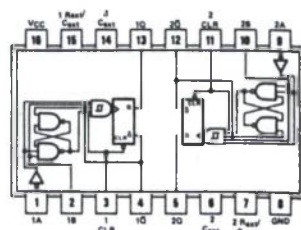
See page 7-338

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

DUAL MONOSTABLE MULTIVIBRATORS

221

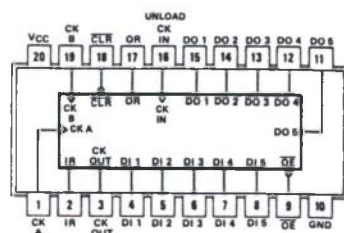


See page 6-68

SN54221 (J, W) SN74221 (J, N)
SN54LS221 (J, W) SN74LS221 (J, N)

ASYNCHRONOUS FIRST IN, FIRST OUT MEMORIES

225 16 5-BIT WORDS

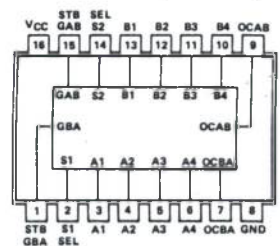


See Bipolar Microcomputer Components Data Book, LCC4270

SN74S225 (J, N)

4-BIT PARALLEL LATCHED BUS TRANSCEIVERS

226 3-STATE OUTPUTS

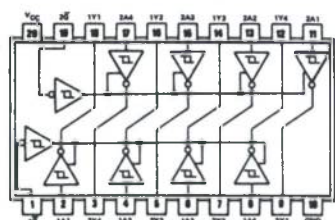


See page 7-345

SN54S226 (J, W) SN74S226 (J, N)

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

240 INVERTED 3-STATE OUTPUTS



See page 6-83

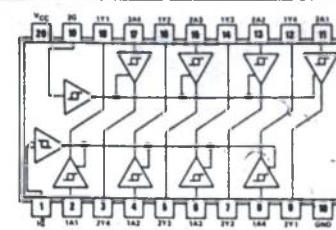
SN54LS240 (J) SN74LS240 (J, N)
SN54S240 (J) SN74S240 (J, N)

54/74 FAMILIES OF COMPATIBLE TTL CIRCUIT

PIN ASSIGNMENTS (TOP VIEWS)

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

241 NONINVERTED 3-STATE OUTPUTS

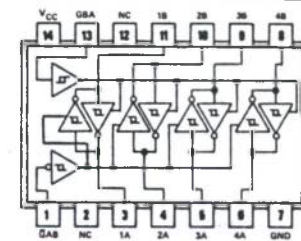


See page 6-83

SN54LS241 (J) SN74LS241 (J, N)
SN54S241 (J) SN74S241 (J, N)

QUADRUPLE BUS TRANSCEIVERS

242 INVERTED 3-STATE OUTPUTS

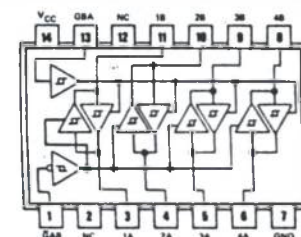


See page 6-87

SN54LS242 (J, W) SN74LS242 (J, N)
NC—No internal connection

QUADRUPLE BUS TRANSCEIVERS

243 NONINVERTED 3-STATE OUTPUTS

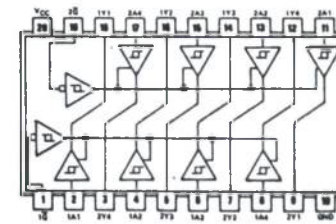


See page 6-87

SN54LS243 (J, W) SN74LS243 (J, N)
NC—No internal connection

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

244 NONINVERTED 3-STATE OUTPUTS



See page 6-83

SN54LS244 (J) SN74LS244 (J, N)

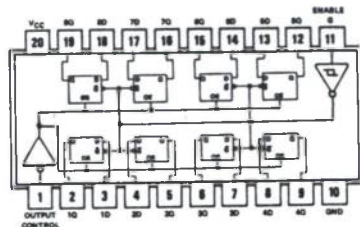
4/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

OCTAL D-TYPE LATCHES

373

3-STATE OUTPUTS
COMMON OUTPUT CONTROL
COMMON ENABLE



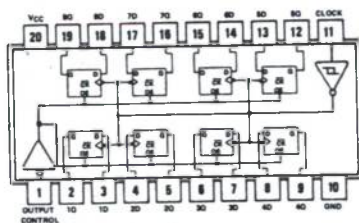
SN54LS373 (J) SN74LS373 (J, N)
SN54S373 (J) SN74S373 (J, N)

See page 7-471

OCTAL D-TYPE FLIP-FLOPS

374

3-STATE OUTPUTS
COMMON OUTPUT CONTROL
COMMON CLOCK

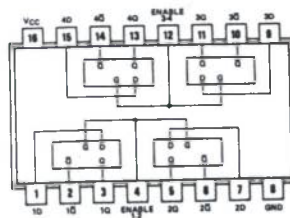


SN54LS374 (J) SN74LS374 (J, N)
SN54S374 (J) SN74S374 (J, N)

See page 7-471

4-BIT BISTABLE LATCHES

375



SN54LS375 (J, W) SN74LS375 (J, N)

See page 7-478

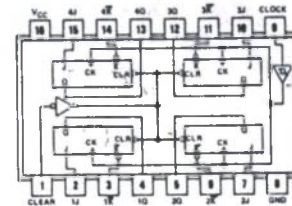
54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

QUAD J-K FLIP-FLOPS

376

COMMON CLOCK
COMMON CLEAR



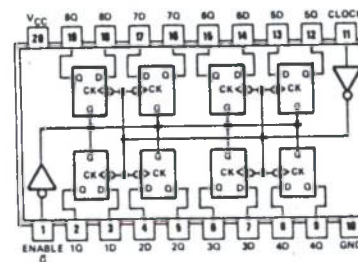
SN54376 (J, W) SN74376 (J, N)

See page 7-479

OCTAL D-TYPE FLIP-FLOPS

377

SINGLE-RAIL OUTPUTS
COMMON ENABLE
COMMON CLOCK



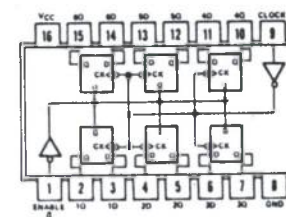
SN54LS377 (J) SN74LS377 (J, N)

See page 7-481

HEX D-TYPE FLIP-FLOPS

378

SINGLE-RAIL OUTPUTS
COMMON ENABLE
COMMON CLOCK



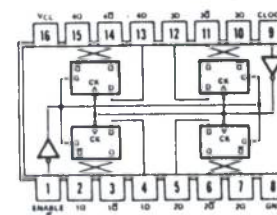
SN54LS378 (J, W) SN74LS378 (J, N)

See page 7-481

QUAD D-TYPE FLIP-FLOPS

379

DOUBLE-RAIL OUTPUTS
COMMON ENABLE
COMMON CLOCK



SN54LS379 (J, W) SN74LS379 (J, N)

See page 7-481

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

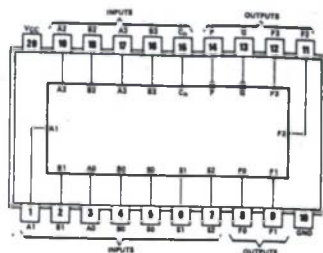
PIN ASSIGNMENTS (TOP VIEWS)

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

381

8 BINARY FUNCTIONS
USE 'S182 FOR LOOK-AHEAD CARRY

See page 7-484



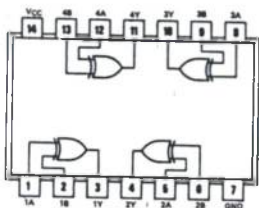
SN54S381(J) SN74S381(J, N)

QUAD 2-INPUT EXCLUSIVE-OR GATES

386

POSITIVE LOGIC:
 $Y = A \oplus B = \overline{A}B + A\overline{B}$

See page 7-487



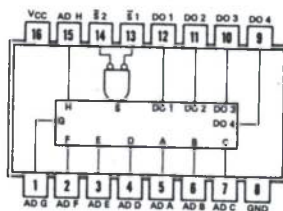
SN54LS386 (J, W) SN74LS386 (J, N)

1024-BIT PROGRAMMABLE READ-ONLY MEMORIES

387

256 4-BIT WORDS
OPEN-COLLECTOR OUTPUTS

See Bipolar Microcomputer Components Data Book, LCC4270



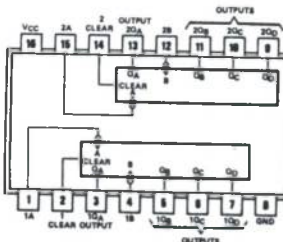
SN54S387 (J, W) SN74S387 (J, N)

DUAL DECADE COUNTERS

390

BI-QUINARY OR BCD SEQUENCES

See page 7-489



SN54390 (J, W) SN74390 (J, N)
SN54LS390 (J, W) SN74LS390 (J, N)

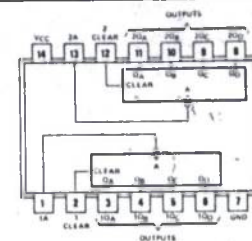
54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

DUAL 4-BIT BINARY COUNTERS

393

See page 7-489



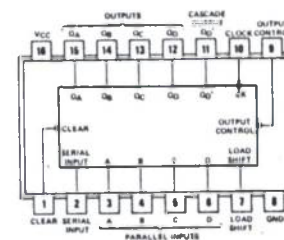
SN54393 (J, W) SN74393 (J, N)
SN54LS393 (J, W) SN74LS393 (J, N)

4-BIT UNIVERSAL SHIFT REGISTERS

395

3-STATE OUTPUTS

See page 7-496



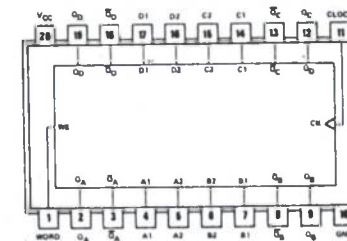
SN54LS395A (J, W) SN74LS395A (J, N)

QUAD 2-INPUT MULTIPLEXERS WITH STORAGE

398

DOUBLE-RAIL OUTPUTS

See page 7-499



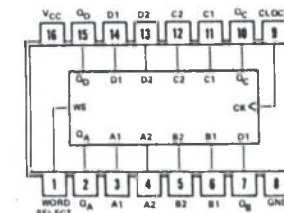
SN54LS398 (J) SN74LS398 (J, N)

QUAD 2-INPUT MULTIPLEXERS WITH STORAGE

399

SINGLE-RAIL OUTPUTS

See page 7-499



SN54LS399 (J, W) SN74LS399 (J, N)

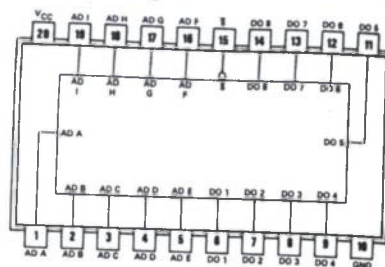
54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

PROGRAMMABLE READ-ONLY MEMORIES

472 3-STATE OUTPUTS

473 OPEN-COLLECTOR OUTPUTS



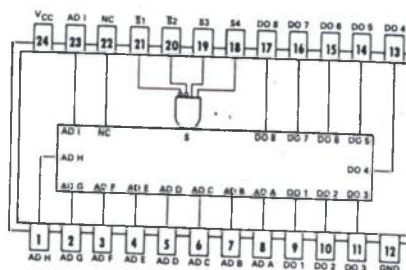
SN54S472 (J) SN74S472 (J, N)
SN54S473 (J) SN74S473 (J, N)

See Memory and Microprocessor Data Book, LCC 4270

PROGRAMMABLE READ-ONLY MEMORIES

474 3-STATE OUTPUTS

475 OPEN-COLLECTOR OUTPUTS



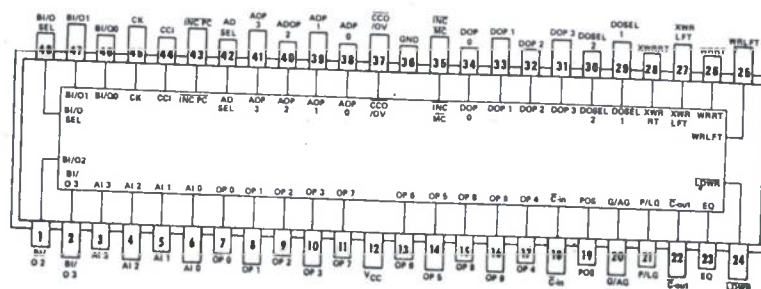
SN54S474 (J) SN74S474 (J, N)
SN54S475 (J) SN74S475 (J, N)

NC - No internal connection

See Memory and Microprocessor Data Book, LCC 4270

4-BIT SLICE PROCESSOR ELEMENTS

481



SN54S481 (J) SN74S481 (J, N)

See Memory and Microprocessor Data Book, LCC 4270

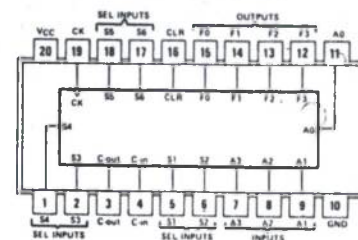
TEXAS INSTRUMENTS

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

4-BIT SLICE EXPANDABLE CONTROL ELEMENTS

482 CASCADABLE TO N-BITS

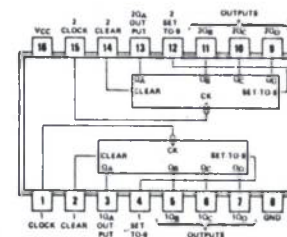


SN54S482 (J) SN74S482 (J, N)

See Bipolar Microcomputer Components Data Book, LCC4270

DUAL DECADE COUNTERS

490

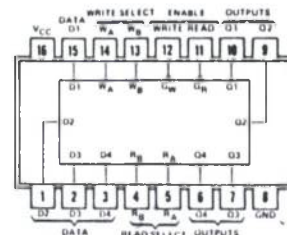


SN54490 (J, W) SN74490 (J, N)
SN54LS490 (J, W) SN74LS490 (J, N)

See page 7-520

4-BY-4 REGISTER FILES

670 3-STATE OUTPUTS
SIMULTANEOUS READ/WRITE
EXPANDABLE TO 1024 WORDS



SN54LS670 (J, W) SN74LS670 (J, N)

See page 7-526

Beckman Series 7545 and 7546 MICROPROCESSOR COMPATIBLE CMOS 12-BIT D-TO-A CONVERTERS

Effective date: June, 1979

Beckman Series 7545 and 7546 are the first CMOS 12-bit Digital-to-Analog Converters to offer the combination of complete 8-bit microprocessor compatibility, real 12-bit accuracy and TTL or CMOS logic input compatibility within a single package.

Their features include:

- 12-Bit Resolution
- $\pm 0.012\%$ linearity ($\pm \frac{1}{2}$ LSB in 12 bits) guaranteed over the operating temperature range (7545)
- Double buffered inputs—separate input and holding registers
- Microprocessor compatible 4-bit/8-bit byte input for 12-bit inputs from 8-bit microprocessors
- Serial or parallel input formats—switchable upon command
- TTL or CMOS input compatibility
- Commercial and military temperature range versions
- Low power CMOS internal circuitry
- All thin film application resistors included for superior stability and precision performance
- Low reference feedthrough for precision AC reference applications

Microprocessor Compatibility

Both Series 7545 and 7546 have two input registers separate from the switch holding register which can separately be enabled to accept a 12-bit input data word in 4-bit (most significant bits) and 8-bit (least significant bits) bytes from an 8-bit microprocessor bus.

True 12-Bit Performance

$\pm \frac{1}{2}$ LSB linearity ($\pm 0.012\%$ FSR) is guaranteed over the full operating temperature range for each model of series 7545. Similarly, worst case limits are specified for initial gain setting error and gain error temperature coefficient for both the 7545 and 7546 and for the Series 7546, zero offset and zero offset temperature coefficient are guaranteed.

Serial or Parallel Operation

Both series can operate in a serial input mode or a parallel input mode and, in fact, can alternately be switched from one mode to the other. In the serial mode, the four least significant bit input registers can be bypassed to allow processing 8-bit input words in the eight most significant bit locations.

The input registers and holding register are configured to allow either switch updating upon command using the enable lines, or in a continuous conversion mode by permanently enabling the transfer lines for parallel operation.

TTL or CMOS Compatible

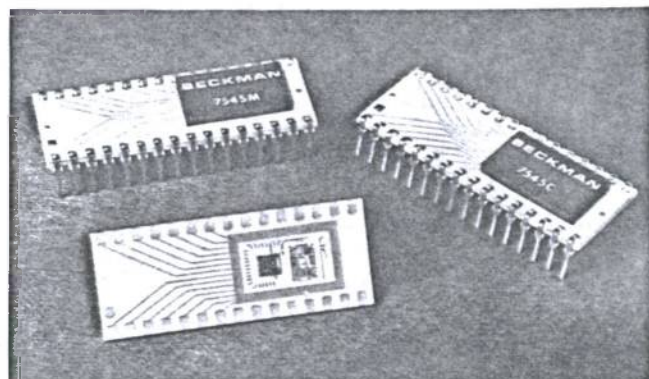
Both input registers utilize input translators which can accept either TTL inputs using a +5 volt supply or CMOS inputs using supply levels from +5 to +15 volts. Separate holding register and input register power supply lines allow this flexibility without compromising linearity.

Military and Commercial Versions

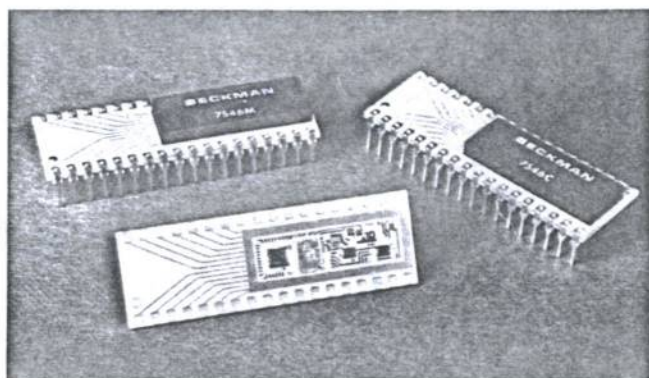
Commercial versions are available in a polymer sealed package (e.g., 7545C and 7546C) with performance specifications guaranteed over 0°C to $+70^{\circ}\text{C}$. The MIL range performance versions utilize an hermetically sealed package with performance guaranteed over -55°C to $+125^{\circ}\text{C}$ (e.g., 7545M and 7546M).

Internal Configuration

Precision thin film nichrome resistors are deposited on an alumina substrate to achieve optimum stability and uncompromised linearity and tracking performance. A separate CMOS chip contains the input level translators and shift registers, the DAC switch



Series 7545 Multiplying D-to-A Converter



Series 7546 General Purpose D-to-A Converter

holding register, the switch drivers and analog switches and is silicon nitride passivated to insure high reliability performance for both commercial and military requirements. These devices are assembled on a thick film substrate to provide the most cost effective overall assembly.

All units receive 100% electrical testing over the specified temperature range to assure reliable performance capabilities for both commercial and military versions.

General Purpose and Multiplying Models

Series 7545 is the four quadrant multiplying configuration designed for use with an external AC reference. Four quadrant multiplication is implemented by the bipolar digital proportioning of the AC reference. Two quadrant multiplication can be implemented by either unipolar proportioning of an AC reference or bipolar proportioning of a unipolar DC reference. The use of external reference and amplifier circuitry allows the maximum flexibility for supply levels and signal processing levels. For example, the maximum reference and output levels are determined by the amplifiers selected and their output voltage swing capability with respect to power supply levels. Series 7545 can be used with a wide range of supplies to accommodate TTL or CMOS system standard supply levels where the digital and analog subsystems operate on different supplies.

Series 7545 typically requires less than 10 mW of power consumption, making it an ideal choice for operation with low power

BECKMAN

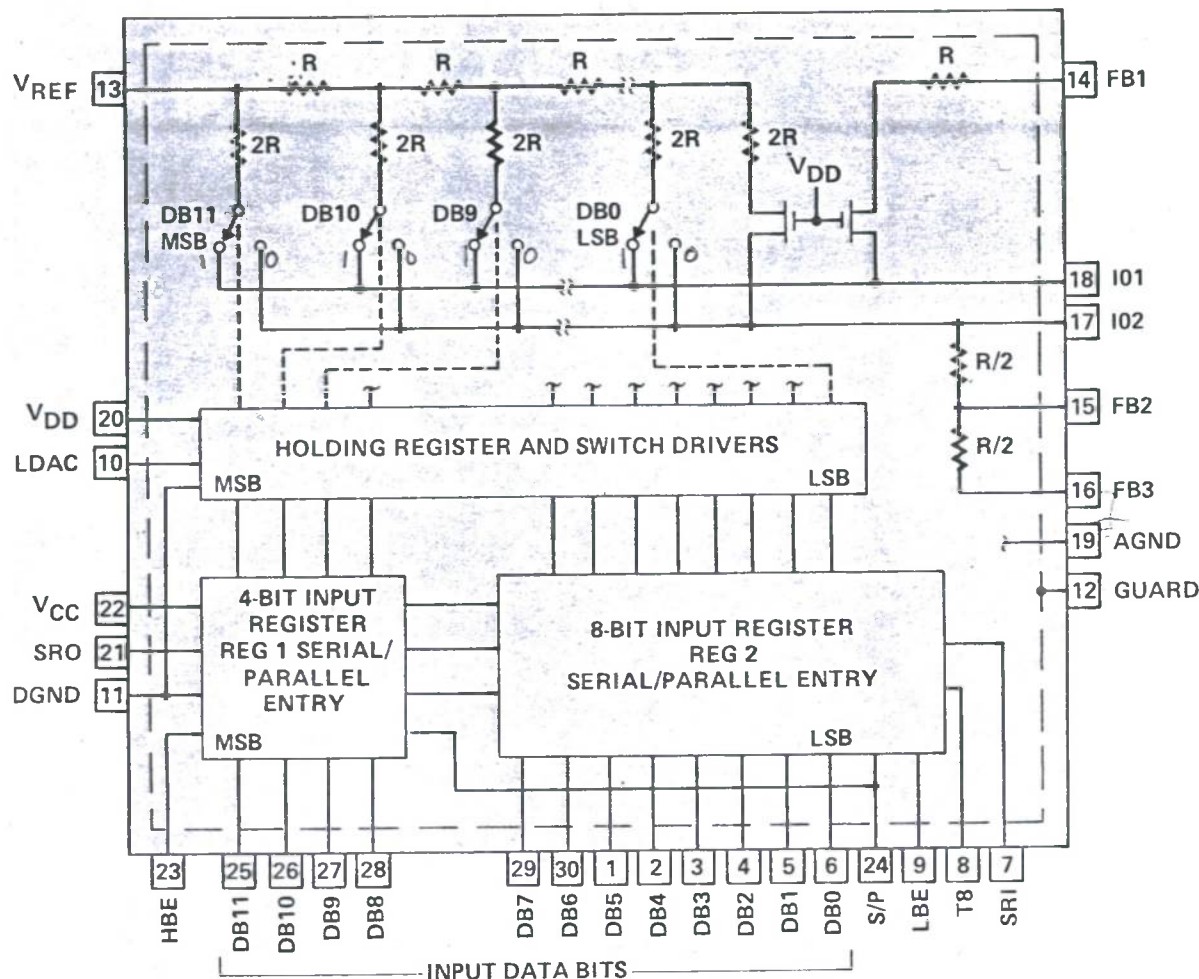


Figure 1. Series 7545 Block Diagram

external amplifiers in battery powered, portable instrumentation applications.

Series 7546 allows higher system density by providing a complete general purpose converter which contains a 10 volt DC reference and the op amp and feedback circuitry to achieve up to 5 mA of output drive capability without the addition of other external components.

The complete general purpose converter also eases the design and manufacturing task by incorporating preadjusted zero offset for the output buffer amplifier, the biasing amplifier for bipolar operation and, also, the internal reference. Each is precisely pretrimmed to guarantee initial tolerances which will satisfy most applications, although external adjustment is possible, if required. Series 7546 can also utilize the wide variety of supply levels anticipated for most digital systems applications utilizing a combination of CMOS or TTL and analog interface sections.

Series 7545 Operation

As shown in Figure 1, the input voltage, V_{REF} , is applied to a 20k binary weighted, R-2R ladder. Each 2R leg is connected to a pair of N-channel, MOS transistors. These transistors switch the binary weighted currents that flow in each 2R leg to either the I01 bus (logic "1" input) or to the I02 bus (logic "0" input). Normal operation requires operational amplifiers at I01 and I02 which maintain these nodes at ground or virtual ground potential.

Internal Compensation

The "on" resistance of the MOS transistor switches are binary weighted with the MSB set at 25 ohms. The linearity of the DAC is dependent upon the ratio accuracies of the switch resistances and not upon their absolute values. Excellent switch ratio tolerances account for small linearity errors even over the operating temperature range of the DAC. Also, the low power density in

the switching transistors eliminates transient thermal gradients normally encountered with bipolar current switches.

Feedback gain compensation for switch resistance is provided by an "on" switch in series with the internal "R" feedback resistor. This compensation transistor reduces gain drift errors to less than $2p/10^{\circ}/^{\circ}C$ and provides outstanding power supply rejection.

A second compensation transistor (unique to Series 7545 and 7546) compensates the R-2R ladder terminating resistor.

Digital Inputs

The input buffer register is divided into a 4-bit shift register that controls the four MSB's and an 8-bit shift register that controls the eight LSB's. A serial/parallel control line (S/P) allows data to be applied to the serial input through SRI or the parallel inputs, DB0-DB11. Separate enable lines (HBE and LBE) are provided for these registers. In the parallel mode when S/P is logic "0", data bits DB11 through DB8 will enter the input register when HBE is set to a logic "1". Data inputs DB0 through DB7 will enter their input buffer register when LBE is set to logic "1". This arrangement allows sequential loading of a 2-byte, 12-bit word from a single 8-bit data bus.

In the serial mode when S/P is logic "1", serial data appearing at the serial input (SRI) will be clocked into the input register on the positive transition of a pulse train applied simultaneously to HBE and LBE. The serial data in the input buffer can be recovered from the serial output pin, SRO.

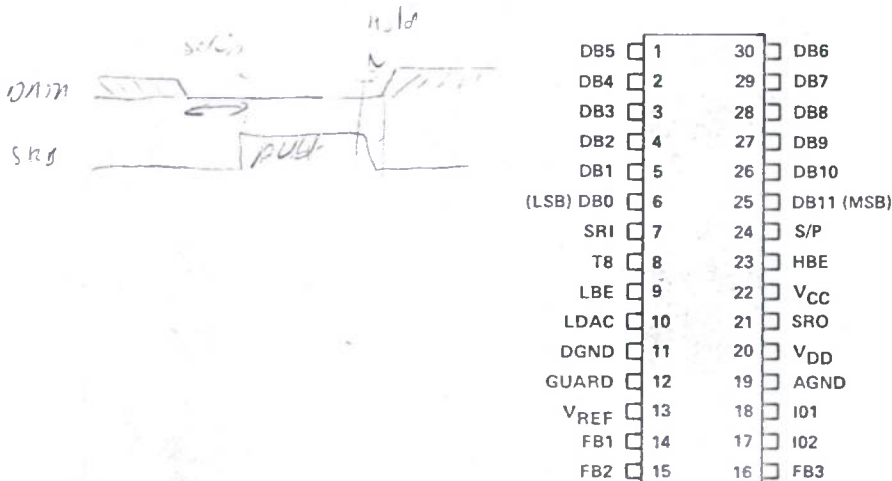
All logic inputs are provided with level shifters that operate from V_{CC} . All digital inputs are compatible with TTL logic levels when V_{CC} is connected to +5V and CMOS levels when V_{CC} is connected to a CMOS supply (see operating limits).

Table I—Series 7545 Performance Specifications (Note 1)

Parameter			Conditions	Minimum	Typical	Maximum	Units
Converter Transfer Characteristics	Resolution		T _B = "1"			12	bits
	Non-linearity	7545C	0°C ≤ T _C ≤ +70°C			±0.012	% FSR
		7545M	-55°C ≤ T _C ≤ +125°C			±0.012	% FSR
	Differential Non-linearity				±0.012		% FSR
	Initial Gain Setting		(Note 2)			±0.02	% FSR
	Gain Setting Tempco	7545C	0°C ≤ T _C ≤ +70°C		1	10	p/10 ⁶ /°C
		7545M	-55°C ≤ T _C ≤ +125°C		1	2	p/10 ⁶ /°C
Analog Output Characteristics	Reference Feedthrough		V _{REF} = 20V p-p; 10 kHz		1	10	mV p-p
	Settling Time		(Note 3)		2		μs
	Output Leakage	7545C	0°C ≤ T _C ≤ +70°C			25	nA
	Current (I _{O1} , I _{O2})	7545M	-55°C ≤ T _C ≤ +125°C			100	nA
	Output Capacitance (at I _{O1} , I _{O2})	C01	All Data Bits High		200		pF
		C02	All Data Bits High		150		pF
		C01	All Data Bits Low		125		pF
		C02	All Data Bits Low		70		pF
Reference Characteristics	Input Voltage Range					±10	V
	Input Resistance			18	20	22	kΩ
Digital Input Characteristics	TTL Logic Levels (Note 4)	Logic "1"	V _{CC} = +5V	3.0			V
		Logic "0"	V _{CC} = +5V			0.8	V
		I _{IL} ; I _{IH}	All Input Levels		+10 ⁻⁵	+1	μA
	Parallel Data & Serial 8-Bit Word						
	Data Set-up		t _{DW}	750			nsec
	Data Hold		t _{DH}	50			nsec
	Pulse Width		LDAC, HBE, LBE t ₀	500			nsec
	Serial Data 12-Bit Word						
	Data Set-up		t _{DW}	300			nsec
	Data Hold		t _{DH}	450			nsec
	Pulse Width		LDAC, HBE, LBE t ₀	500			nsec
Power Supply Characteristics	V _{CC} , V _{DD} Current					2	mA
	V _{CC} , V _{DD} Supply Rejection					10	p/10 ⁶ FSR/%
Temperature Ranges	Operating Temp. Range	7545C	Worst Case Limits Apply	0		+70	°C
		7545M	Worst Case Limits Apply	-55		+125	°C
Storage Temp. Range			Non-operating	-65		+150	°C

Notes: (7545)

1. Unless otherwise specified, performance guarantees apply for +10V ≤ V_{DD} ≤ +15V, +5V ≤ V_{CC} ≤ V_{DD} and V_{REF} = ±10V and specifications for 7545C apply over 0°C ≤ T_C ≤ +70°C and for 7545M over -55°C ≤ T_C ≤ +125°C.
2. The Internal feedback resistor, R (FB1 at pin 14) has been laser pre-trimmed to establish the proper gain ratio against the ladder impedance "R."
3. The output settling time for the multiplying configuration is almost entirely dependent on the external amplifier selected. The specification shown is for the output current I_{O1} for an FSR step settling to within 0.01% FSR.
4. Threshold levels shown are for TTL logic levels. For different V_{CC} levels typical in CMOS systems, see Figure 3.



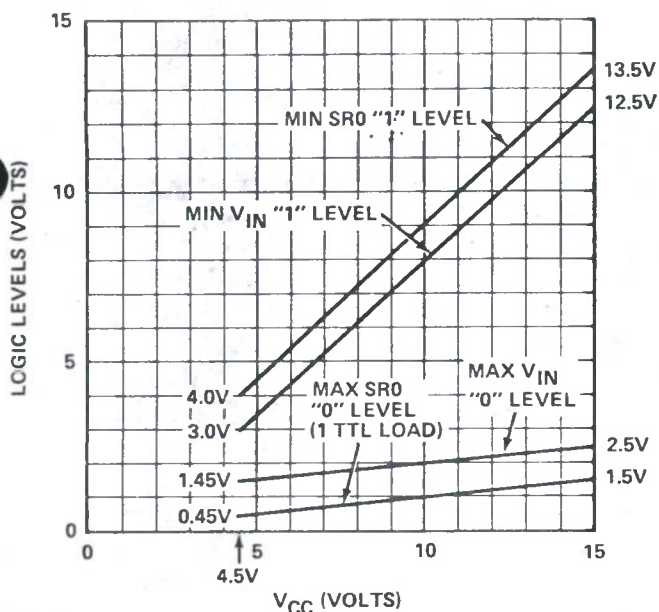


Figure 3. Logic Levels

Terminology

Differential Linearity is the difference between the actual output and the theoretical output between any two adjacent steps in the transfer function.

Gain is the ratio of the full scale range (FSR) to V_{REF} after the zero output error has been removed.

Gain Drift is the maximum change in gain at the temperature end points with respect to the $+25^{\circ}\text{C}$ value, divided by the corresponding temperature change expressed in parts per million of full scale range ($\text{p}/10^6/^{\circ}\text{C}$).

Non-Linearity is the deviation of the analog output from a straight line drawn between the two end points (all bit ON and all bits OFF).

Offset Drift is the maximum change in offset voltage at the temperature end points with respect to the $+25^{\circ}\text{C}$ value, divided by the corresponding temperature change expressed in parts per million of full scale range ($\text{p}/10^6/^{\circ}\text{C}$).

Settling Time is the total time (including slew time) for the output to settle to within the error band ($\pm 0.01\%$ FSR) about its value following an input change.

FSR is full scale range—FSR = 10V for unipolar 0 to -10V output, FSR = 20V for bipolar $+10\text{V}$ to -10V output.

Digital Input Codes (7545 and 7546)

The digital input codes for Series 7545 and 7546 D-to-A Converters are natural binary code. The MSB has a weight of (2^{-1}), and second bit has a weight of (2^{-2}), and so forth down to the LSB, which has a weight of 2^{-12} . Table III below shows the full-scale, half-scale and zero codes, and their respective analog outputs for both unipolar output and bipolar output.

Table III—Series 7545 and 7546 Digital Input Codes. ($V_{REF} = +10.000\text{V}$)

M S B	Digital Input (DB11-DB0)	L S B	Unipolar Configuration		Bipolar Configuration	
			Output (Fig. 7, 9)	Output (V)	Output (Fig. 8, 11)	Output (V)
FFF	1 1 1 1 1 1 1 1 1 1 1 1		$-V_{REF} (1.0 - 2^{-12})$	-9.9976	$-V_{REF} (1.0 - 2^{-11})$	-9.9952
SC1	1 0 0 0 0 0 0 0 0 0 0 1		$-V_{REF} (0.5 + 2^{-12})$	-5.0024	$-V_{REF} (2^{-11})$	-0.00488
SC0	1 0 0 0 0 0 0 0 0 0 0 0		$-V_{REF}/2$	-5.0000	0	0
7FF	0 1 1 1 1 1 1 1 1 1 1 1		$-V_{REF} (0.5 - 2^{-12})$	-4.9976	$+V_{REF} (2^{-11})$	$+0.00488$
1	0 0 0 0 0 0 0 0 0 0 0 1		$-V_{REF} (2^{-12})$	-0.00244	$+V_{REF} (1 - 2^{-11})$	$+9.9952$
0	0 0 0 0 0 0 0 0 0 0 0 0		0	0	$+V_{REF}$	$+10$

Terminal Designations

AGND	Analog Ground (see Power Supply Considerations).
DB0-DB11	Input Data Bits.
DGND	Digital Ground (see Power Supply Considerations).
FB1,2,3	Feedback Resistors (see Figures 1 and 2).
GUARD	Ground Plane (see Power Supply Considerations).
HBE	*High Byte Enable—In the parallel mode data at DB8 through DB11 is transferred into the input register when HBE reaches logic "1". In the serial mode, HBE is tied to LBE and is used to clock serial data into the input register.
I01,2	Current output buses normally at ground or virtual ground.
LBE	*Low Byte Enable—In the parallel mode data at DB0 through DB7 is transferred into the input register when LBE reaches logic "1". In the serial mode, LBE is tied to HBE and is used to clock serial data into the input register.
LDAC	*Load DAC—Logic "1" at LDAC transfers data from the input register to the holding register to update the DAC output.
OUTPUT	Converter Voltage Output (7546 only).
RADJ	Reference Adjust (see Applications Section).
REF(10V)	Internal Reference Output (7546 only) normally connected to V_{REF} reference input.
S/P	Serial/Parallel Control—Set at logic "1" for serial operation and logic "0" for parallel operation.
SRI	Serial Register Input.
SRO	Serial Register Output.
SUM	Output amplifier summing junction (7546 only).
T8	Truncate 8 allows 8-bit serial words to enter the eight most significant bit locations bypassing the four least significant bit locations. Set T8 at logic "0" for 8-bit serial operation. Also, DB0 through DB3 must be held at logic "0" during 8-bit operation. For 12-bit operation set T8 at logic "1".

*In parallel operation, LDAC, HBE and LBE can either be controlled by system timing or permanently wired to logic "1" to allow continuous parallel updating.

Maximum Ratings (7545 and 7546)

V_{REF} to GND	$\pm 25\text{V}$
V_{DD} to GND	$+17\text{V}$
V_{CC} to GND	$+17\text{V}$
V_{CC} to V_{DD}	$+0.4\text{V}$
I01, I02	$\pm 5\text{mA}$
I01 to GND; I02 to GND	-300mV to V_{DD}
Operating Temperature Range	-55°C to $+125^{\circ}\text{C}$
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Digital Input Voltage Range	V_{DD} to GND

Operation Cautions

- Do not apply voltages higher than V_{CC} to SRO.
- Do not apply voltages higher than V_{DD} or less than -300mV with respect to GND to any other input/output terminal except V_{REF} , FB1 or FB2.
- The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Store units in conductive foam.
- V_{CC} should never exceed V_{DD} by more than 0.4V .
- Unused inputs should be grounded or connected to V_{CC} .
- A 50ohm resistor should be connected in series with V_{DD} next to the decoupling capacitor, thus protecting the device during power on sequencing.

Power Supply Considerations

Significant improvement in high frequency noise rejection will result if individual converter circuits are decoupled from the power supply with small R-C networks. These should be located as close to the circuit as practical. Separate digital and analog ground returns designated DGND and AGND respectively, are provided so that noisy ground currents, normally associated with digital circuits can be separately returned to the system power supply ground. Both AGND and DGND must be connected to a common ground potential within the system. The converter will perform within specification with up to $\pm 0.5V$ between the two grounds.

A separate ground plane built into the DAC (GUARD) may be used to reduce leakage currents and feedthrough capacitance. It is recommended that this be connected to the analog ground (AGND) in most system applications.

Protective diodes shown in the application diagrams protect the device against voltage transients during power "on" and "off" sequencing. If V_{CC} and V_{DD} are derived from a common supply and the device's Absolute Maximum Ratings are strictly adhered to, these protective measures may be omitted.

12-Bit Parallel Loading (7545 and 7546)

The logic connections for loading 12-bit parallel data into the input register is shown in Figure 4. Data is transferred from the input buffer register to the holding register when the update line, LDAC is logic "1". (LDAC is a level-actuated function and must be held "high" at least 500 nanoseconds for proper data transfer to occur). When data is stable on the parallel inputs (DB0-DB12), it can be transferred on the positive edge of the enable pulse (logic "1" applied to HBE and LBE simultaneously for 500 ns min.). If LDAC is logic "0", the contents of the holding register are unaffected by the signals appearing on the data bit inputs.

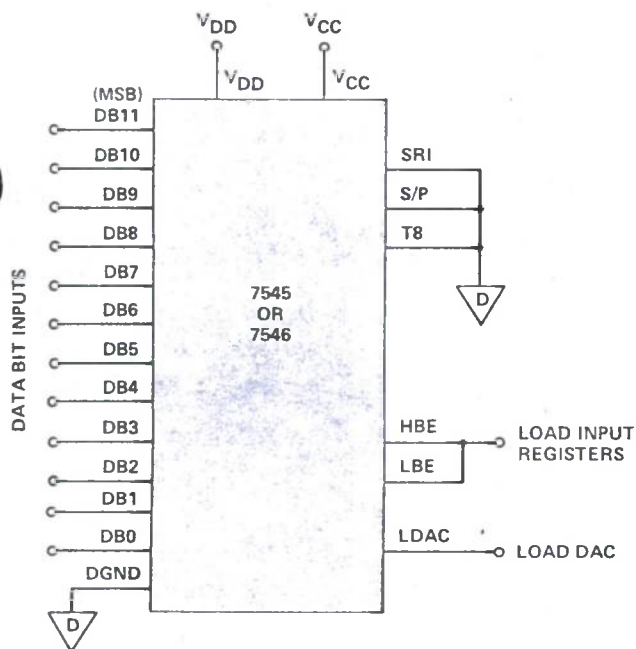


Figure 4. 12-Bit Parallel Loading

Two Byte Parallel Loading (7545 and 7546)

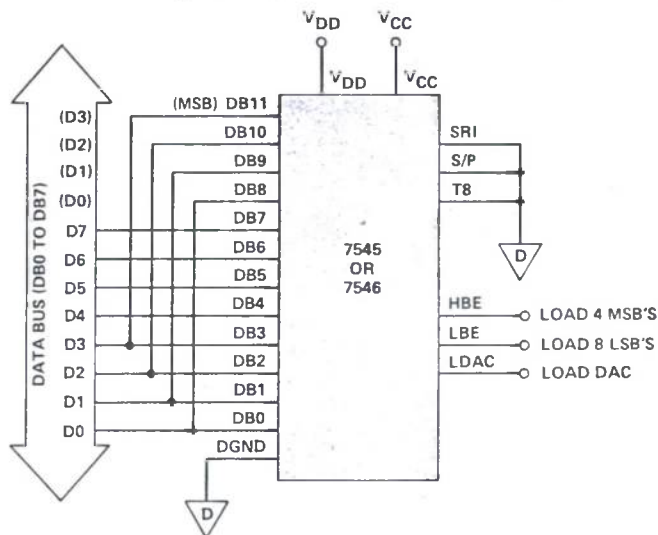
The configuration for two-byte loading of parallel data from a data bus is shown in Figure 5. As shown in the timing diagram, the least significant data byte (DB0-DB7) is loaded into the input buffer register on the positive transition of LBE. When the most significant data byte (DB8-DB11) is available on the bus, the input buffer register is loaded on the positive edge of HBE. Data is transferred from the input buffer register to the holding register when the DAC update line LDAC is logic "1".

Serial Data Input Loading (7545 and 7546)

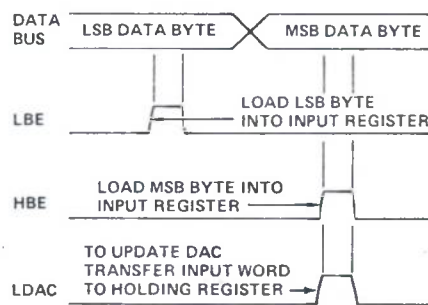
The connection and timing diagrams for serial loading are shown in Figure 6. Either an 8-bit or a 12-bit word may be loaded into the input register at SRI. If T8 is held to logic "0", the four least significant input latches in the input register are bypassed to provide serial loading of eight-bit words into the eight most significant bit locations. If T8 is held to a logic "1", the DAC will accept a 12-bit serial word. When loading a 12-bit word, exactly

12 positive edges of the clock are required at HBE and LBE to load serial data into the input register. Only 8 positive edges of the clock are required for an 8-bit word.

The serial data in the input buffer can be recovered from the serial output pin, SRO. The first bit loaded into the input register will appear at the shift register output, (SRO) either on the 12th positive clock edge ($T8 = "1"$) or on the 8th positive clock edge ($T8 = "0"$). S/P must be held at logic "1" for serial operation.

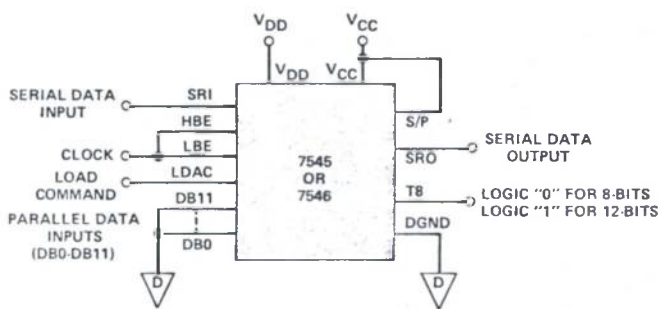


(a) Connection Diagram

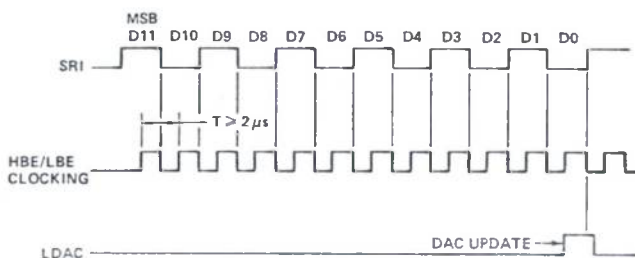


(b) Timing Diagram

Figure 5. Two Byte Parallel Loading (7545 and 7546)



(a) Connection Diagram



(b) Timing Diagram for 12-Bit Word

Figure 6. Serial Data Input Loading

Unipolar Operation (7545)

Figure 7 shows the circuit configuration for 7545 unipolar operation (0V to $-10V$). A protective diode is shown across the amplifier input which limits the amount of voltage which can appear across the terminals IO1 to ground during power turn-on or turn-off. Note that IO2 is connected to analog ground (AGND). Both DGND and AGND must be tied to a common ground somewhere in the system.

The specific zero offset circuit will be determined by the external amplifier selected. If a summing node approach is required, typical component values are shown in Figure 9. If a fast output amplifier is used, the feedback capacitor C1 is used to compensate for summing node capacitance.

The Zero Offset and Gain adjustments should be performed in the following order.

1. Zero Offset Adjustment—Adjust the amplifier output to zero (within ± 0.5 mV). (A zero offset appearing at the summing junction (IO1) will produce a gain error, therefore, the output should be set to zero by a method that will also set the summing junction voltage to zero.)
2. Gain Adjustment—Set R1 and R2 to zero ohms. Set DB0-DB11 to logic "1". If the output is greater than the required full scale value increase R1. If the output is less than the required full scale value increase R2.

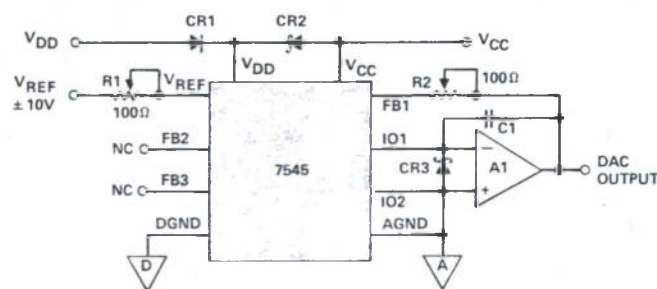


Figure 7. Unipolar Operation

Bipolar Operation (7545)

Figure 8 shows the circuit configuration for Series 7545 bipolar operation. Protective diodes and the feedback compensation capacitor are shown.

1. Zero Offset Adjustment—Adjust the offset of amplifiers A1 and A2 to zero. (A zero offset appearing at the summing junction will produce a gain error, therefore, the outputs should be set to zero by a method that will also set the summing junctions to zero.)
2. Gain Adjustment—Set the DAC register to all "0's". Set R1 and R2 to zero. If the DAC output is greater than $+V_{REF}$, increase R2 until it reads $+V_{REF}$. If the DAC output is less than $+V_{REF}$, increase R1 until it reads $+V_{REF}$. This assumes that reference adjustment which would otherwise be preferred is not possible.

Note that the bipolar gain resistors at FB2 and FB3 are precisely preset internal thin film resistors and their specification impact is included in the limits for "Gain Setting."

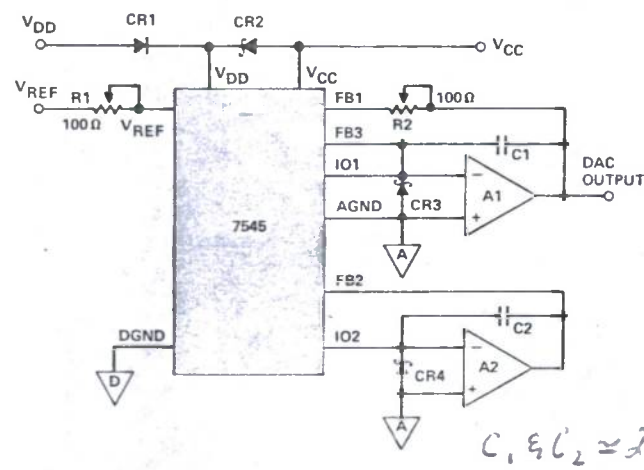


Figure 8. Bipolar Operation

Unipolar Operation (7546)

The 7546 general purpose converter includes the output buffer amplifiers A1 and A2 and an internal precision $+10V$ reference. Each amplifier has been individually laser preadjusted for zero offset at $+25^{\circ}C$. The feedback resistors (FB1, FB2 and FB3) have also been ratio matched to meet the gain tolerances specified. Additional adjustment may be accomplished as shown in Figure 9 for unipolar operation.

1. Zero Offset Adjustment—The DAC output can be adjusted to read precisely zero for a code of 000000000000 by adjusting the summing current into or out of the summing junction (SUM) as shown.
2. Gain Adjustment—Set all bits to "1" and adjust the reference potentiometer until the DAC output reads $-0.9976V$.

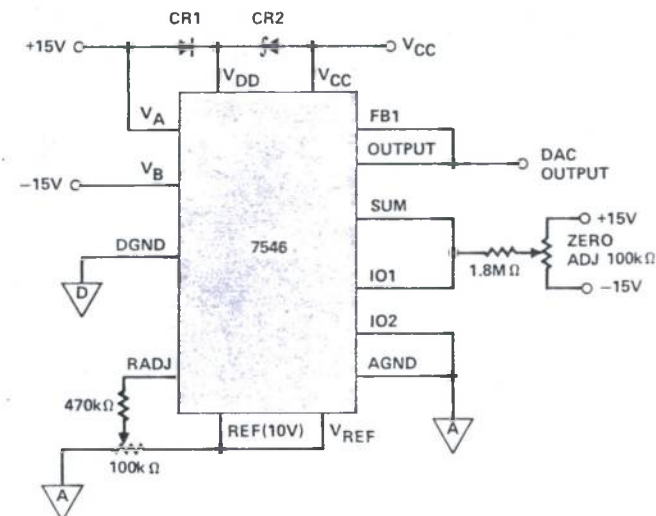


Figure 9. Unipolar Operation Utilizing Internal $+10V$ Reference

Unipolar Two Quadrant Multiplying DAC (7546)

Series 7546 can utilize an external AC reference to accomplish two quadrant multiplication (bipolar reference $\times$ unipolar digital input) as shown in Figure 10.

1. Gain Adjustment—Set DB0 to DB11 to all "0's" and set R1 and R2 to zero ohms. If the DAC output voltage is greater than $+V_{REF}$, increase R1 until it reads precisely $+V_{REF}$. If the DAC output is less than $+V_{REF}$, increase R2 until it reads precisely $+V_{REF}$.

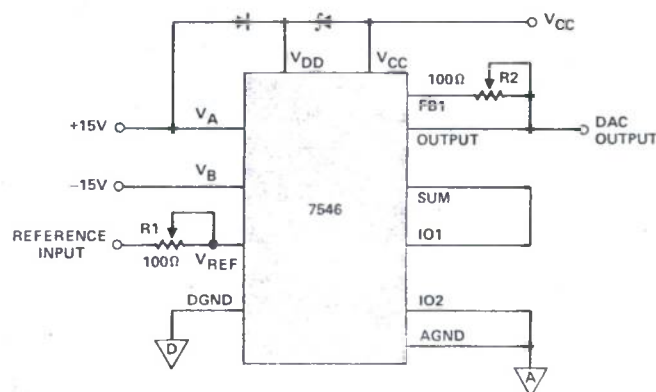


Figure 10. Unipolar Two Quadrant Multiplying DAC

Bipolar Operation (7546)

The circuit configuration for bipolar operation using the internal precision reference is shown in Figure 11.

1. Zero Offset Adjustment—The DAC output can be adjusted to read precisely zero for a code of 100000000000 by adjusting the current into or out of the summing junction (SUM) as shown.
2. Gain Adjustment—Set the DAC to all "0's" and adjust the reference adjust potentiometer until the DAC output reads +10.000V.

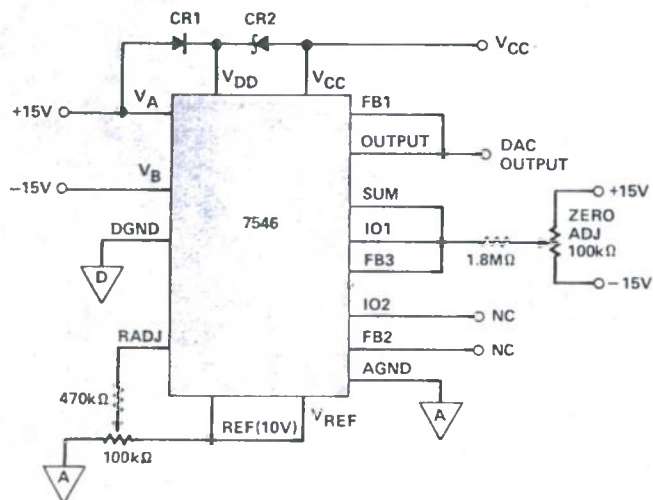
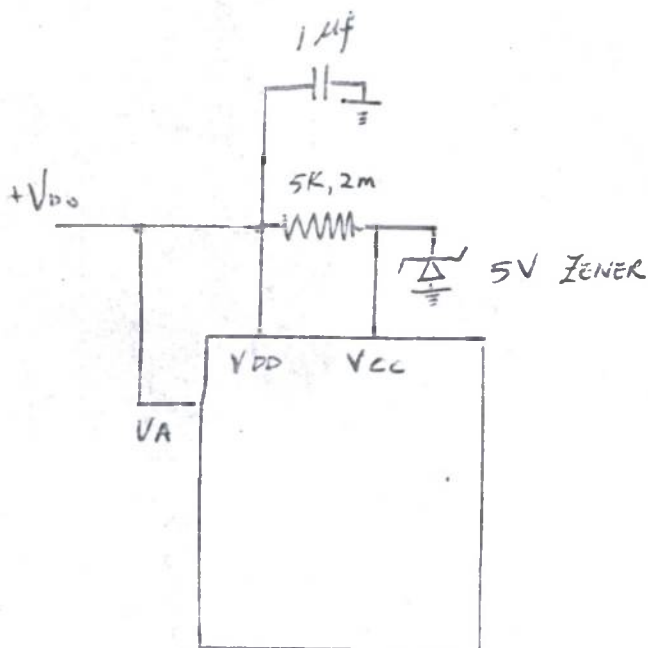


Figure 11. Bipolar Operation Using Internal +10V Reference



Four Quadrant Multiplying DAC (7546)

Series 7546 can operate as a four quadrant multiplier (bipolar digital input $\times$ bipolar reference) using an external reference as shown in Figure 12.

1. Gain Adjustment—Set DB0 to DB11 to all "0's" and set R1 and R2 to zero ohms. If the DAC output is greater than $+V_{REF}$, increase R1 until the output reads $+V_{REF}$. If the DAC output is less than $+V_{REF}$, increase R2 until it reads $+V_{REF}$.

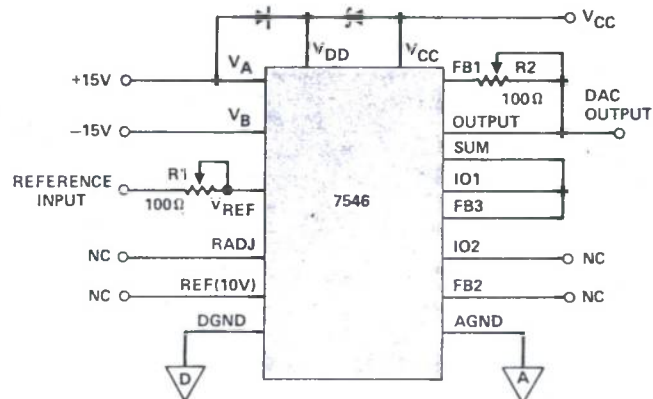


Figure 12. Four Quadrant Multiplying DAC



MOTOROLA

Specifications and Applications Information

QUAD LED SEGMENT DRIVER – MC75491 HEX LED DIGIT DRIVER – MC75492

The MC75491 and MC75492 are designed to interface MOS logic to common cathode light-emitting diode readouts in serially addressed multi-digit displays. Using a segment address and digit scan LED drive method in a time multiplexing system results in a minimizing of the number of required drivers.

- Low Input Current Requirement for MOS Compatibility
- Low Standby Power Drain
- Source or Sink Current Capability of 50 mA for MC75491
- Sink Current Capability of 250 mA for MC75492
- Four High-Gain Darlington Drivers in a Single Package – MC75491
- Six High-Gain Darlington Drivers in a Single Package – MC75492

MC75491
MC75492

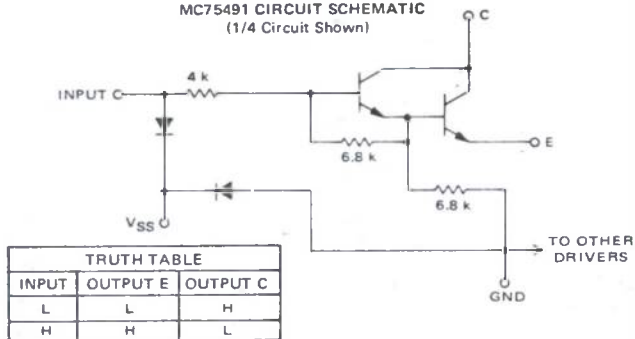
MULTIPLE LIGHT-EMITTING DIODE (LED) DRIVERS

SILICON MONOLITHIC
INTEGRATED CIRCUITS

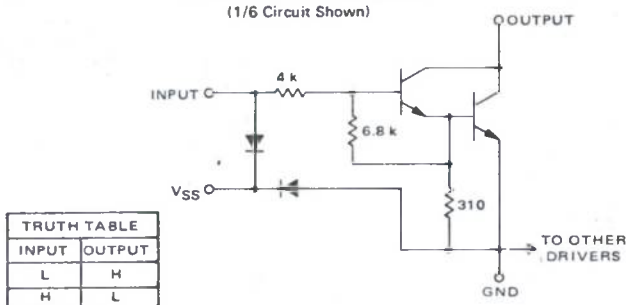


P SUFFIX
PLASTIC PACKAGE
CASE 646

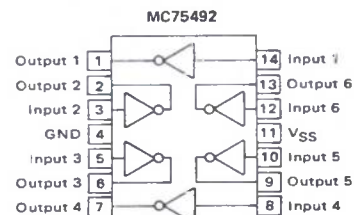
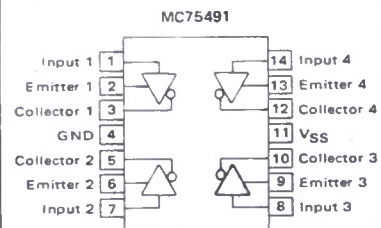
MC75491 CIRCUIT SCHEMATIC
(1/4 Circuit Shown)



MC75492 CIRCUIT SCHEMATIC
(1/6 Circuit Shown)



CONNECTION DIAGRAMS



MAXIMUM RATINGS ($T_A = 0$ to $+70^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value		Unit
		MC75491	MC75492	
Bias Supply Voltage (See Note 1)	V_{SS}	10	10	Vdc
Input Voltage (See Note 2)	V_{in}	-5.0 to V_{SS}	-5.0 to V_{SS}	Vdc
Collector Voltage (See Note 3)	V_C	10	10	Vdc
Collector-to-Emitter Voltage	V_{CE}	10	—	Vdc
Collector-to-Input Voltage	V_{CI}	10	10	Vdc
Emitter Voltage ($V_{in} \geq 5.0$ Vdc)	V_E	10	—	Vdc
Emitter-to-Input Voltage	V_{EI}	5.0	—	Vdc
Continuous Collector Current (Each Collector) (All Collectors)	I_C	50 200	250 600	mA mA
Power Dissipation (Package Limitation) Ceramic and Plastic Dual In-Line Packages Derate above $T_A = +25^\circ\text{C}$	P_D	830 6.6		mW mW/ $^\circ\text{C}$
Operating Temperature Range	T_A	0 to $+70$		$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to $+150$		$^\circ\text{C}$

Note 1. V_{SS} terminal voltage is with respect to any other device terminal.

Note 2. With the exception of the inputs, the GND terminal must always be the most negative device voltage for proper operation.

Note 3. Voltage values are with respect to GND terminal unless otherwise noted.

ELECTRICAL CHARACTERISTICS ($V_{SS} = 10$ Vdc, $T_A = 0$ to $+70^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC75491			MC75492			Unit
		Min	Typ	Max	Min	Typ	Max	
Low-Level Collector-to-Emitter Voltage ($V_{in} = 8.5$ V thru 1.0 k Ω , $I_{OL} = 50$ mA, $V_E = 5.0$ V) $T_A = +25^\circ\text{C}$ $T_A = 0$ to $+70^\circ\text{C}$	V_{CEL}	— —	0.9 —	1.2 1.5	— —	— —	— —	Vdc
High-Level Collector Current $V_{CH} = 10$ V, $V_E = 0$, $I_{in} = 40$ μA $V_{CH} = 10$ V, $V_E = 0$, $V_{in} = 0.7$ V	I_{CH}	— —	— —	100 100	— —	— —	— —	μA
Low-Level Output Voltage ($V_{in} = 6.5$ V thru 1.0 k Ω , $I_{OL} = 250$ mA) $T_A = +25^\circ\text{C}$ $T_A = 0$ to $+70^\circ\text{C}$	V_{OL}	— —	— —	— —	— —	0.9 —	1.2 1.5	Vdc
High-Level Output Current $V_{OH} = 10$ V, $I_{in} = 40$ μA $V_{OH} = 10$ V, $V_{in} = 0.5$ V	I_{OH}	— —	— —	— —	— —	— —	200 200	μA
Input Current at Maximum Input Voltage $V_{in} = 10$ V, $I_{OL} = 20$ mA	I_{in}	—	2.2	3.3	—	2.2	3.3	mA
Emitter Current — Reverse Bias $I_C = 0$, $V_{in} = 0$, $V_E = 5.0$ V	I_{ER}	—	—	100	—	—	—	μA
Bias Supply Current ($V_{SS} = 10$ V)	I_{SS}	—	—	1.0	—	—	1.0	mA

SWITCHING CHARACTERISTICS ($V_{SS} = 7.5$ V, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

Propagation Delay Time, High-to-Low Level $R_L = 200$ Ω , $V_{IH} = 4.5$ V, $C_L = 15$ pF, $V_E = 0$ $R_L = 39$ Ω , $V_{IH} = 7.5$ V, $C_L = 15$ pF	t_{PHL}	— —	20* —	— —	— —	— 40	— —	ns
Propagation Delay Time, Low-to-High Level $C_L = 15$ pF, $V_E = 0$, $R_L = 200$ Ω , $V_{IH} = 4.5$ Vdc $C_L = 15$ pF, $R_L = 39$ Ω , $V_{IH} = 7.5$ Vdc	t_{PLH}	— —	40* —	— —	— —	— 80	— —	ns

*To collector output.

MPY-8HJ

8 X 8 BIT PARALLEL MULTIPLIER

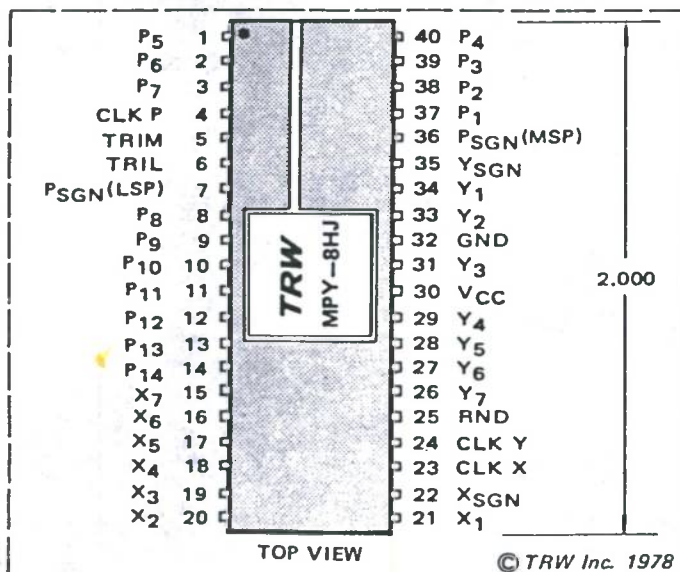
The MPY-8HJ multiplier is a high speed, TTL LSI device. It is a parallel two's complement multiplier with double precision output. It can be plugged into an MPY-8AJ socket, and be functionally equivalent. However, this newer multiplier has positive setup and zero hold times, which reduces system clocking complexity in many applications. Also, the RND control is now a registered input, making its timing and usage more convenient.

Four input/output registers are used in the MPY-8HJ multipliers. These registers are D-type flip-flops with a single phase TTL clock.

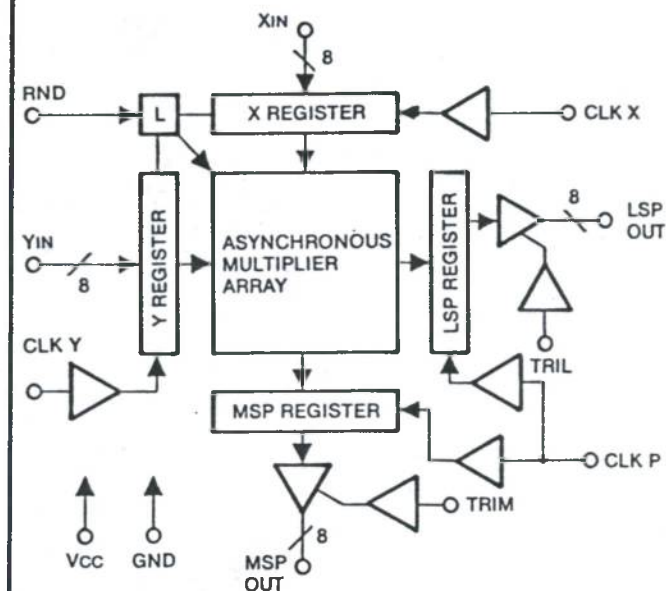
Applications for the MPY-8HJ multipliers include digital processing and high speed multiplication for fast, nonrecursive filters. They are ideal for extending the capabilities of mini/microcomputers, permitting hardware multiplication for increased computational speed, and are particularly useful for video processing.

FEATURES

- 8-by-8 parallel, two's complement multiplier
- Double precision product
- 65 nsec typical multiply time (MPY-8HJ)
- 45 nsec typical multiply time (MPY-8HJ-1)
- Much lower power than MSI equivalent multipliers
- Includes input/output positive edge-triggered registers
- Single chip, bipolar technology
- Single bus or multiport operation
- Radiation hard
- TTL input and output
- Three state outputs
- Single power supply, +5V
- 40 pin dual in-line package
- Pin compatible with MPY-8AJ
- Zero hold time on input registers



MPY-8HJ LOGICAL BLOCK DIAGRAM



CONTROLS

(Positive logic unless otherwise noted)

CLK X — X_{IN} Register Clock

CLK Y — Y_{IN} Register Clock

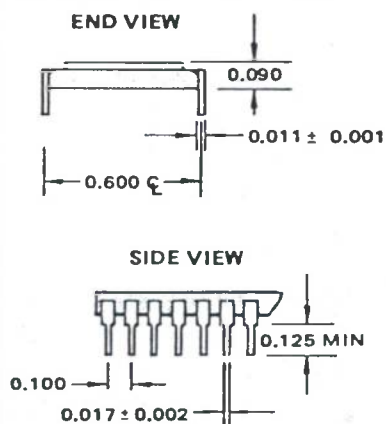
CLK P — Product Registers Clock

TRIL — LSP Three-State Control,
TRIM — MSP Three-State Control,
LOGIC 0 = Enable, LOGIC 1 = Disable

RND (LOGIC 1) — Adds 2⁻⁸ to product (fractional two's complement field — See Page 5 for I/O Format)

RND Latch is strobed by (CLK X or CLK Y)

PACKAGE INFORMATION



NOTE
DIMENSIONS IN INCHES

THERMAL CHARACTERISTICS

θ_{CA} (Still air) = 25°C/W

θ_{CA} (300 cfm) = 15°C/W

GENERAL SPECIFICATIONS

Absolute maximum ratings (above which the useful life may be impaired)

Supply voltage	-0.5 to 7.0 V
Input voltage	0 to 5.5 V
Output voltage	0 to 5.5 V
Operating temperature range (T _{case})	-55°C to 125°C
Storage temperature range	-65°C to 150°C
Lead temperature (10 seconds)	300°C
Junction temperature	175°C

Part Numbers

Commercial

MPY-8HJ
MPY-8HJ-1
MPY-12HJ
MPY-16HJ
MPY-24HJ

Military

MPY-8HJM
—
MPY-12HJM
MPY-16HJM
MPY-24HJM

Recommended operating conditions

	COMMERCIAL			MILITARY			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	4.75	5.0	5.25	4.5	5.0	5.5	V
High-level output current, I _{OH}			-0.4			-0.4	mA
Low-level output current, I _{OL}			4.0			4.0	mA
Clock pulse width, t _{PW} (measured at 1.5 V level)	25			30			nsec
Input register setup time, t _S (see Figure 6)	25			30			nsec
Input register hold time, t _H (see Figure 6)	0			0			nsec
Operating temperature (T _{ambient} for commercial, T _{case} for military)	0		70	-55		125	°C

Electrical characteristics over recommended temperature range (except as otherwise noted)

PARAMETER	TEST CONDITIONS	COMMERCIAL			MILITARY			UNIT
		MIN	TYP**	MAX	MIN	TYP**	MAX	
V _{IH} High-level input voltage		2.0			2.0			V
V _{IL} Low-level input voltage				0.8			0.8	V
V _{OH} High-level output voltage	V _{CC} = MIN I _{OH} = -0.4 mA	2.4	2.7		2.4	2.7		V
V _{OL} Low-level output voltage	V _{CC} = MIN I _{OL} = 4.0 mA		0.3	0.5		0.3	0.5	V
I _{IH} High-level input current	V _{CC} = MAX V _{IH} = 2.4			75			75	μA
I _{IL} Low-level input current	V _{CC} = MAX V _{IL} = 0.4			-0.4			-0.4	mA
I _{IH} Clocks*, three-states—high level input current	V _{CC} = MAX V _{IL} = 2.4			75			75	μA
I _{IL} Clocks*, three-states—low level input current	V _{CC} = MAX V _{IL} = 0.4			-1.0			-1.0	mA

*NOTE: Clock P is two equivalent clock loads.

Switching characteristics across V_{CC} and temperature ranges (except as otherwise noted)

PARAMETER	TEST CONDITIONS	TYP**	MAX		UNIT
			COMMERCIAL	MILITARY	
Output delay t _D	Load 1 (see Figure 5)	25	35	40	nsec
Three state output delay Output enable, t _{ENA} Output disable, t _{DIS}	Load 2 (see Figure 5)	25	35	40	nsec

**NOTE: At V_{CC} = 5.0 V, T_A = 25°C.

GENERAL INFORMATION

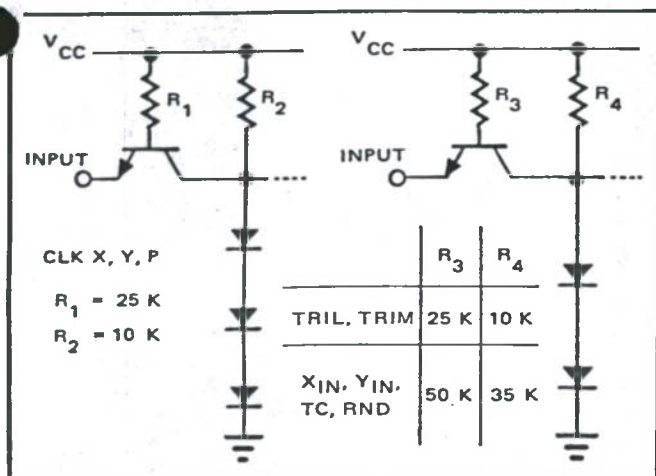


Figure 1. Equivalent Input Schematics

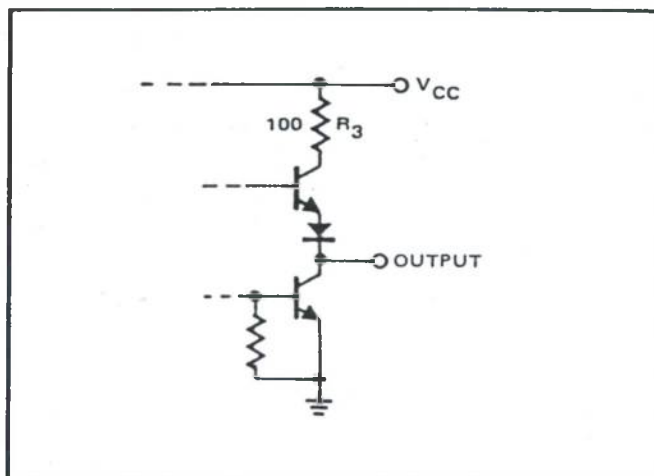


Figure 2. Output Schematic

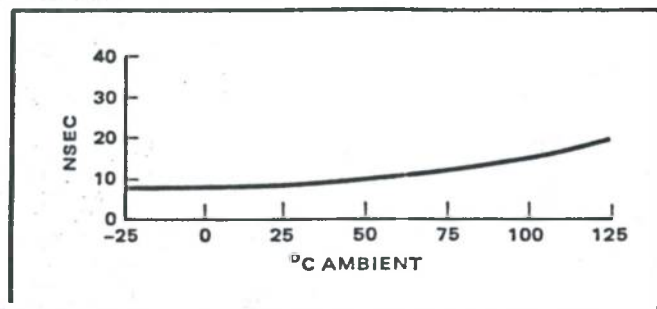


Figure 3. Typical Setup Time

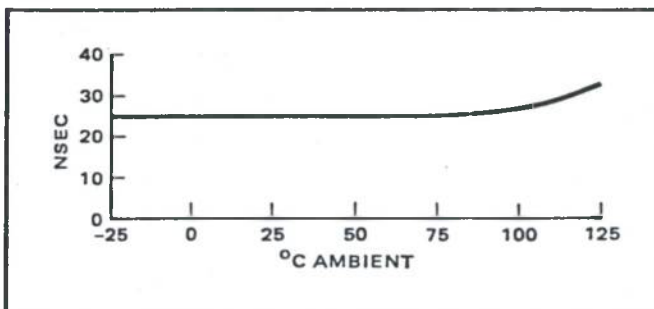


Figure 4. Typical Three-State Delay, Output Delay

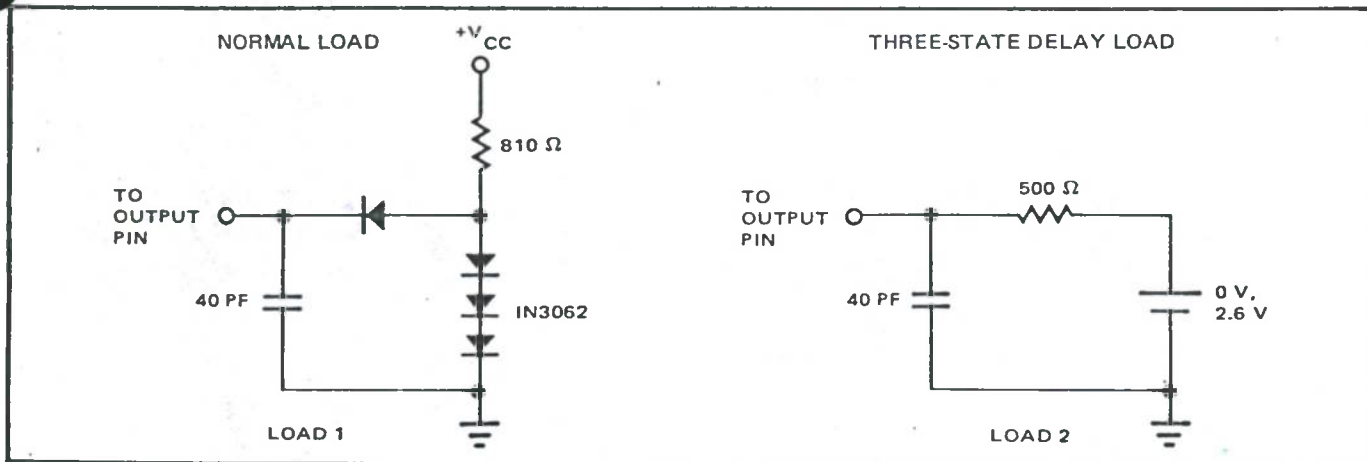


Figure 5. Test Loads for Delay Measurements

SOCKET INFORMATION

TYPE	40 PIN	64 PIN
Wire wrap	Excel 800B-003-40	Excel 800B-003-64
Solder tail-tin plate	Cambion 703-4040-01-04-12	Cambion 703-4064-01-04-12
Solder tail-gold plate	Robinson Nugent ICN-406-S5-G	Robinson Nugent ICN-649-S5-G
Zero insertion force	Textool 240-3346-00-0605	Textool 232-2601-00-0605 (2 Required)

TRI-STATE Octal Buffers

General Description

These devices provide eight, two-input buffers in each package. All employ the newest low power-Schottky TTL technology. One of the two inputs to each buffer is used as a control line to gate the output into the high-impedance state, while the other input passes the data through the buffer. The 95 and 97 present true data at the outputs, while the 96 and 98 are inverting. On the 95 and 96 versions, all eight TRI-STATE enable lines are common, with access through a 2-input NOR gate. On the 97 and 98 versions, four buffers are enabled from one common line, and the other four buffers are enabled from another common line. In all cases the outputs are placed in the TRI-STATE condition by applying a high logic level to the enable pins. These devices represent octal, low power-Schottky versions of the very popular DM70/8095, 96, 97, and 98 TRI-STATE hex buffers.

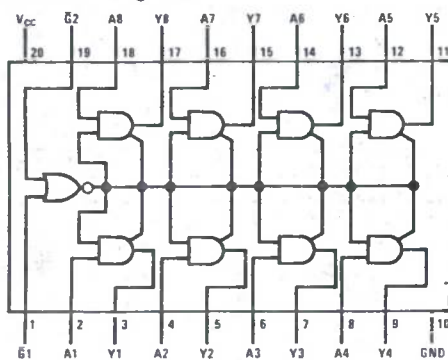
Features

- Octal versions of popular DM8095, 8096, 8097, 8098
- Typical power dissipation

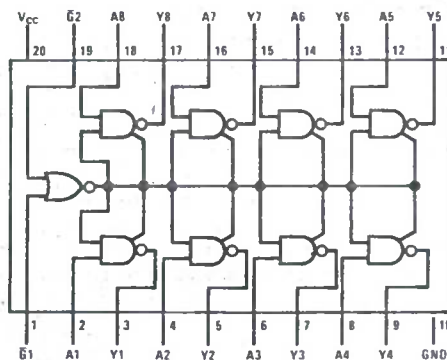
LS95, LS97	80 mW
LS96, LS98	65 mW
- Typical propagation delay

LS95, LS97	13 ns
LS96, LS98	10 ns
- Low power-Schottky, TRI-STATE technology

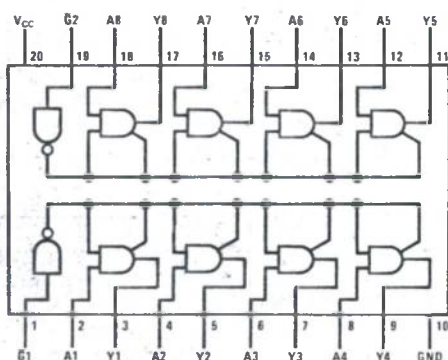
Connection Diagrams



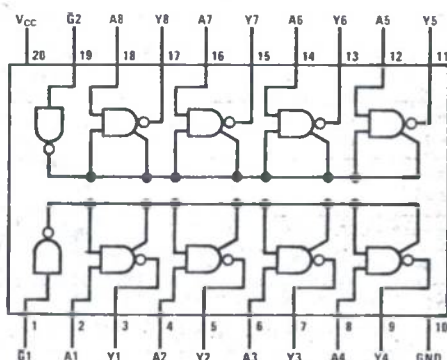
71LS95/81LS95(N)



71LS96/81LS96(N)



71LS97/81LS97(N)



71LS98/81LS98(N)

Truth Tables

LS95			
INPUTS		OUTPUT	
$\bar{G}1$	$\bar{G}2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

LS96			
INPUTS		OUTPUT	
$\bar{G}1$	$\bar{G}2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

LS97		
INPUTS	OUTPUT	
$\bar{G}$	A	Y
H	X	Z
L	H	H
L	L	L

LS98		
INPUTS	OUTPUT	
$\bar{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Notes

(1) All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.

(2) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25^\circ C$

PARAMETER		CONDITIONS	DM71LS/B1LS						UNITS
			LS95, LS97			LS96, LS98			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega$		11	16		6	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			15	22		13	17	ns
t_{ZH}	Output Enable Time to High Level			16	25		17	27	ns
t_{ZL}	Output Enable Time to Low Level			13	20		16	25	ns
t_{HZ}	Output Disable Time from High Level	$C_L = 5 \text{ pF}, R_L = 2 \text{ k}\Omega$		13	20		13	20	ns
t_{LZ}	Output Disable Time from Low Level			19	27		18	27	ns

General

These devices have a word length; and 2) word input over logic level comparison to accomplish DM8200.

Connect

Truth Ta

8279/8279-5

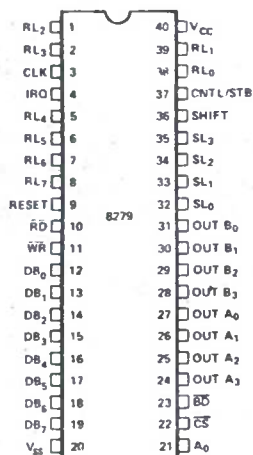
PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

- MCS-85™ Compatible 8279-5
- Simultaneous Keyboard Display Operations
- Scanned Keyboard Mode
- Scanned Sensor Mode
- Strobed Input Entry Mode
- 8-Character Keyboard FIFO
- 2-Key Lockout or N-Key Rollover with Contact Debounce
- Dual 8- or 16-Numerical Display
- Single 16-Character Display
- Right or Left Entry 16-Byte Display RAM
- Mode Programmable from CPU
- Programmable Scan Timing
- Interrupt Output on Key Entry

The Intel® 8279 is a general purpose programmable keyboard and display I/O interface device designed for use with Intel® microprocessors. The keyboard portion can provide a scanned interface to a 64-contact key matrix. The keyboard portion will also interface to an array of sensors or a strobed interface keyboard, such as the hall effect and ferrite variety. Key depressions can be 2-key lockout or N-key rollover. Keyboard entries are debounced and strobed in an 8-character FIFO. If more than 8 characters are entered, overrun status is set. Key entries set the interrupt output line to the CPU.

The display portion provides a scanned display interface for LED, incandescent, and other popular display technologies. Both numeric and alphanumeric segment displays may be used as well as simple indicators. The 8279 has 16X8 display RAM which can be organized into dual 16X4. The RAM can be loaded or interrogated by the CPU. Both right entry, calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto-increment of the display RAM address.

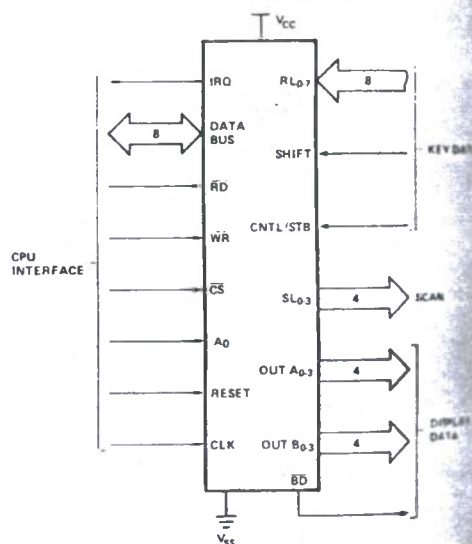
PIN CONFIGURATION



PIN NAMES

Pin	I/O	DATA BUS (BI DIRECTIONAL)
DB ₀₋₇	I/O	DATA BUS (BI DIRECTIONAL)
CLK	I	CLOCK INPUT
RESET	I	RESET INPUT
CS	I	CHIP SELECT
RD	I	READ INPUT
WR	I	WRITE INPUT
A ₀	I	BUFFER ADDRESS
IRQ	O	INTERRUPT REQUEST OUTPUT
SL ₀₋₃	O	SCAN LINES
RL ₀₋₇	I	RETURN LINES
SHIFT	I	SHIFT INPUT
CNTL/STB	I	CONTROL/STROBE INPUT
OUT A ₀₋₃	O	DISPLAY (A) OUTPUTS
OUT B ₀₋₃	O	DISPLAY (B) OUTPUTS
BD	O	BLANK DISPLAY OUTPUT

LOGIC SYMBOL



HARDWARE DESCRIPTION

The 8279 is packaged in a 40 pin DIP. The following is a functional description of each pin.

No. Of Pins	Designation	Function
8	DB0-DB7	Bi-directional data bus. All data and commands between the CPU and the 8279 are transmitted on these lines.
1	CLK	Clock from system used to generate internal timing.
1	RESET	A high signal on this pin resets the 8279. After being reset the 8279 is placed in the following mode: 1) 16 8-bit character display —left entry. 2) Encoded scan keyboard—2 key lockout. Along with this the program clock prescaler is set to 31.
1	$\overline{CS}$	Chip Select. A low on this pin enables the interface functions to receive or transmit.
1	A ₀	Buffer Address. A high on this line indicates the signals in or out are interpreted as a command or status. A low indicates that they are data.
2	$\overline{RD}$, $\overline{WR}$	Input/Output read and write. These signals enable the data buffers to either send data to the external bus or receive it from the external bus.
1	IRQ	Interrupt Request. In a keyboard mode, the interrupt line is high when there is data in the FIFO/Sensor RAM. The interrupt line goes low with each FIFO/Sensor RAM read and returns high if there is still information in the RAM. In a sensor mode, the interrupt line goes high whenever a change in a sensor is detected.
2	V _{SS} , V _{CC}	Ground and power supply pins.
4	SL0-SL3	Scan Lines which are used to scan the key switch or sensor matrix and the display digits. These lines can be either encoded (1 of 16) or decoded (1 of 4).
8	RL0-RL7	Return line inputs which are connected to the scan lines through the keys or sensor switches. They have active internal pullups to keep them high until a switch closure pulls one low. They also serve as an 8-bit input in the Strobed Input mode.

1 SHIFT The shift input status is stored along with the key position on key closure in the Scanned

No. Of Pins	Designation	Function
1	CNTL/STB	Keyboard modes. It has an active internal pullup to keep it high until a switch closure pulls it low. For keyboard modes this line is used as a control input and stored like status on a key closure. The line is also the strobe line that enters the data into the FIFO in the Strobed Input mode. (Rising Edge). It has an active internal pullup to keep it high until a switch closure pulls it low.
4	OUT A ₀ -OUT A ₃	These two ports are the outputs for the 16 x 4 display refresh registers. The data from these outputs is synchronized to the scan lines (SL ₀ -SL ₃) for multiplexed digit displays. The two 4 bit ports may be blanked independently. These two ports may also be considered as one 8 bit port.
4	OUT B ₀ -OUT B ₃	
1	$\overline{BD}$	Blank Display. This output is used to blank the display during digit switching or by a display blanking command.

PRINCIPLES OF OPERATION

The following is a description of the major elements of the 8279 Programmable Keyboard/Display interface device. Refer to the block diagram in Figure 1.

I/O Control and Data Buffers

The I/O control section uses the $\overline{CS}$, A₀, $\overline{RD}$ and $\overline{WR}$ lines to control data flow to and from the various internal registers and buffers. All data flow to and from the 8279 is enabled by $\overline{CS}$. The character of the information, given or desired by the CPU, is identified by A₀. A logic one means the information is a command or status. A logic zero means the information is data. $\overline{RD}$ and $\overline{WR}$ determine the direction of data flow through the Data Buffers. The Data Buffers are bi-directional buffers that connect the internal bus to the external bus. When the chip is not selected ($\overline{CS} = 1$), the devices are in a high impedance state. The drivers input during $\overline{WR} \cdot \overline{CS}$ and output during $\overline{RD} \cdot \overline{CS}$.

Control and Timing Registers and Timing Control

These registers store the keyboard and display modes and other operating conditions programmed by the CPU. The modes are programmed by presenting the proper command on the data lines with A₀ = 1 and then sending a $\overline{WR}$. The command is latched on the rising edge of $\overline{WR}$.

INTERFACE

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-Byte Display

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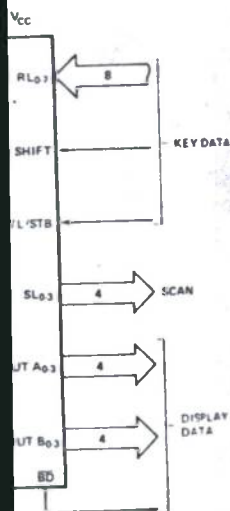
Timing

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e designed for use with contact key matrix. The ch as the hall effect and rebounded and strobed in set the interrupt output

other popular display ple indicators. The 8279 ogated by the CPU. Both write of the display RAM

YMBOL



FUNCTIONAL DESCRIPTION

Since data input and display are an integral part of many microprocessor designs, the system designer needs an interface that can control these functions without placing a large load on the CPU. The 8279 provides this function for 8-bit microprocessors.

The 8279 has two sections: keyboard and display. The keyboard section can interface to regular typewriter style keyboards or random toggle or thumb switches. The display section drives alphanumeric displays or a bank of indicator lights. Thus the CPU is relieved from scanning the keyboard or refreshing the display.

The 8279 is designed to directly connect to the microprocessor bus. The CPU can program all operating modes for the 8279. These modes include:

Input Modes

- Scanned Keyboard — with encoded (8 x 8 key keyboard) or decoded (4 x 8 key keyboard) scan lines. A key depression generates a 6-bit encoding of key position. Position and shift and control status are stored in the FIFO. Keys are automatically debounced with 2-key lockout or N-key rollover.

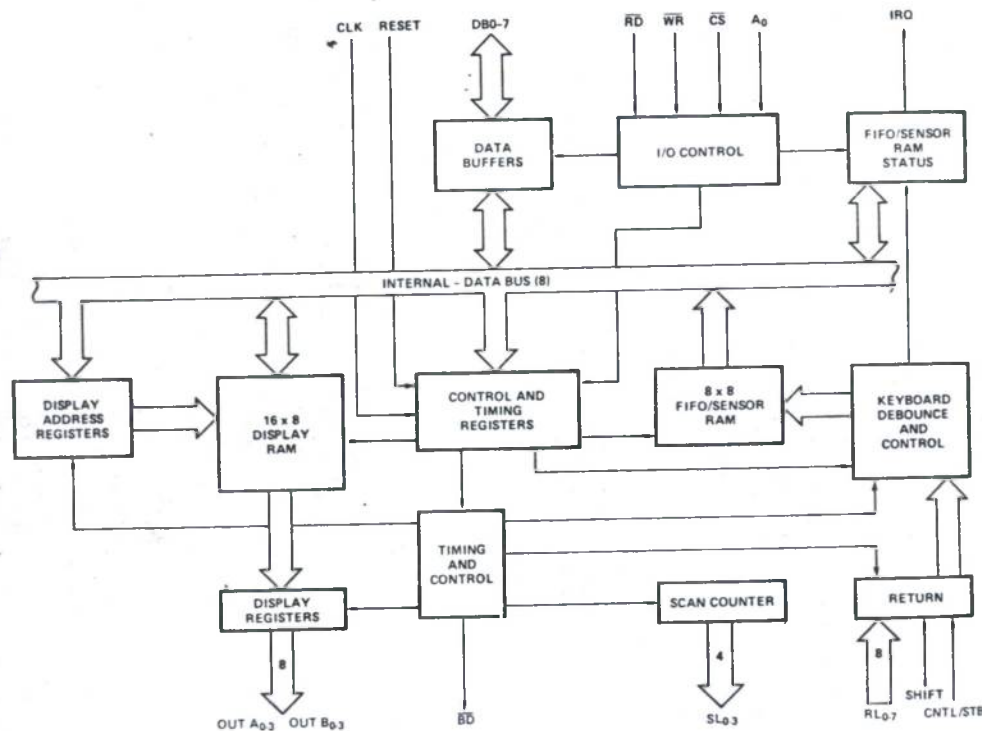
- Scanned Sensor Matrix — with encoded (8 x 8 matrix switches) or decoded (4 x 8 matrix switches) scan lines. Key status (open or closed) stored in RAM addressable by CPU.
- Strobed Input — Data on return lines during control line strobe is transferred to FIFO.

Output Modes

- 8 or 16 character multiplexed displays that can be organized as dual 4-bit or single 8-bit ($B_0 = D_0$, $A_3 = D_7$).
- Right entry or left entry display formats.

Other features of the 8279 include:

- Mode programming from the CPU.
- Clock Prescaler
- Interrupt output to signal CPU when there is keyboard or sensor data available.
- An 8 byte FIFO to store keyboard information.
- 16 byte internal Display RAM for display refresh. This RAM can also be read by the CPU.



The command function is a timing counter that can be programmed at 100 kHz with a 10.3 ms delay down the basic key scan, row scan times.

Scan Counter

The scan counter is the counter programmed externally to decode keyboard and sensor data. The counter decodes 1 of 4 scan lines, the first 4 character in the encoded outputs. In the row outputs.

Return Buffers and Control

The 8 return lines are used for the keyboard and sensor data. In the keyboard, the circuit detects a key depression and checks if the switch is in the correct position. The CONTROL are transferred to the Sensor Matrix mode. The Sensor RAM (FIFO) mode, the content of the FIFO on the return lines.

Display Address Register

The Display Address Register is currently being programmed by the 4-bit nibbles. The addresses are programmed to set the auto increment. The Display RAM can be set to correct mode and address. The 8 nibbles are auto match data entry by the timer. The mode that is set by the timer is set to either left or right. Considerations for display format.

board Mode, the Auto-Increment flag (AI) and the RAM address bits (AAA) are irrelevant. The 8279 will automatically drive the data bus for each subsequent read ($A_0=0$) in the same sequence in which the data first entered the FIFO. All subsequent reads will be from the FIFO until another command is issued.

In the Sensor Matrix Mode, the RAM address bits AAA select one of the 8 rows of the Sensor RAM. If the AI flag is set ($AI=1$), each successive read will be from the subsequent row of the sensor RAM.

Read Display RAM

Code:

0	1	1	AI	A	A	A	A
---	---	---	----	---	---	---	---

The CPU sets up the 8279 for a read of the Display RAM by first writing this command. The address bits AAAA select one of the 16 rows of the Display RAM. If the AI flag is set ($AI=1$), this row address will be incremented after each following read or write to the Display RAM. Since the same counter is used for both reading and writing, this command sets the next read or write address and the sense of the Auto-Increment mode for both operations.

Write Display RAM

Code:

1	0	0	AI	A	A	A	A
---	---	---	----	---	---	---	---

The CPU sets up the 8279 for a write to the Display RAM by first writing this command. After writing the command with $A_0=1$, all subsequent writes with $A_0=0$ will be to the Display RAM. The addressing and Auto-Increment functions are identical to those for the Read Display RAM. However, this command does not affect the source of subsequent Data Reads; the CPU will read from whichever RAM (Display or FIFO/Sensor) which was last specified. If, indeed, the Display RAM was last specified, the Write Display RAM will, nevertheless, change the next Read location.

Display Write Inhibit/Blanking

Code:

				A	B	A	B
1	0	1	X	IW	IW	BL	BL

The IW Bits can be used to mask nibble A and nibble B in applications requiring separate 4-bit display ports. By setting the IW flag ($IW=1$) for one of the ports, the port becomes masked so that entries to the Display RAM from the CPU do not affect that port. Thus, if each nibble is input to a BCD decoder, the CPU may write a digit to the Display RAM without affecting the other digit being displayed. It is important to note that bit B_0 corresponds to bit D_0 on the CPU bus, and that bit A_3 corresponds to bit D_7 .

If the user wishes to blank the display, the BL flags are available for each nibble. The last Clear command issued determines the code to be used as a "blank." This code defaults to all zeros after a reset. Note that both BL flags must be set to blank a display formatted with a single 8-bit port.

Clear

Code:

1	1	0	C_D	C_D	C_D	C_F	C_A
---	---	---	-------	-------	-------	-------	-------

The C_D bits are available in this command to clear all rows of the Display RAM to a selectable blanking code as follows:

C_D	C_D	C_D	
0	X	X	All Zeros (X = Don't Care)
1	0	0	AB = Hex 20 (0010 0000)
1	1	1	All Ones

Enable clear display when = 1 (or by $C_A=1$)

During the time the Display RAM is being cleared ($\sim 160 \mu s$), it may not be written to. The most significant bit of the FIFO status word is set during this time. When the Display RAM becomes available again, it automatically resets.

If the C_F bit is asserted ($C_F=1$), the FIFO status is cleared and the interrupt output line is reset. Also, the Sensor RAM pointer is set to row 0.

C_A , the Clear All bit, has the combined effect of C_D and C_F ; it uses the C_D clearing code on the Display RAM and also clears FIFO status. Furthermore, it resynchronizes the internal timing chain.

End Interrupt/Error Mode Set

Code:

1	1	1	E	X	X	X	X
---	---	---	---	---	---	---	---

 X = Don't care.

For the sensor matrix modes this command lowers the IRQ line and enables further writing into RAM. (The IRQ line would have been raised upon the detection of a change in a sensor value. This would have also inhibited further writing into the RAM until reset).

For the N-key rollover mode — if the E bit is programmed to "1" the chip will operate in the special Error mode. (For further details, see Interface Considerations Section.)

Status Word

The status word contains the FIFO status, error, and display unavailable signals. This word is read by the CPU when A_0 is high and $\overline{CS}$ and $\overline{RD}$ are low. See Interface Considerations for more detail on status word.

Data Read

Data is read when A_0 , $\overline{CS}$ and $\overline{RD}$ are all low. The source of the data is specified by the Read FIFO or Read Display commands. The trailing edge of $\overline{RD}$ will cause the address of the RAM being read to be incremented if the Auto-Increment flag is set. FIFO reads always increment (if no error occurs) independent of AI.

Data Write

Data that is written with A_0 , $\overline{CS}$ and $\overline{WR}$ low is always written to the Display RAM. The address is specified by the latest Read Display or Write Display command. Auto-Incrementing on the rising edge of $\overline{WR}$ occurs if AI set by the latest display command.

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INTERFACE CONSIDERATIONS

Scanned Keyboard Mode, 2-Key Lockout

There are three possible combinations of conditions that can occur during debounce scanning. When a key is depressed, the debounce logic is set. Other depressed keys are looked for during the next two scans. If none are encountered, it is a single key depression and the key position is entered into the FIFO along with the status of CNTL and SHIFT lines. If the FIFO was empty, IRQ will be set to signal the CPU that there is an entry in the FIFO. If the FIFO was full, the key will not be entered and the error flag will be set. If another closed switch is encountered, no entry to the FIFO can occur. If all other keys are released before this one, then it will be entered to the FIFO. If this key is released before any other, it will be entirely ignored. A key is entered to the FIFO only once per depression, no matter how many keys were pressed along with it or in what order they were released. If two keys are depressed within the debounce cycle, it is a simultaneous depression. Neither key will be recognized until one key remains depressed alone. The last key will be treated as a single key depression.

Scanned Keyboard Mode, N-Key Rollover

With N-key Rollover each key depression is treated independently from all others. When a key is depressed, the debounce circuit waits 2 keyboard scans and then checks to see if the key is still down. If it is, the key is entered into the FIFO. Any number of keys can be depressed and another can be recognized and entered into the FIFO. If a simultaneous depression occurs, the keys are recognized and entered according to the order the keyboard scan found them.

Scanned Keyboard — Special Error Modes

For N-key rollover mode the user can program a special error mode. This is done by the "End Interrupt/Error Mode Set" command. The debounce cycle and key-validity check are as in normal N-key mode. If during a single debounce cycle, two keys are found depressed, this is considered a simultaneous multiple depression, and sets an error flag. This flag will prevent any further writing into the FIFO and will set interrupt (if not yet set). The error flag could be read in this mode by reading the FIFO STATUS word. (See "FIFO STATUS" for further details.) The error flag is reset by sending the normal CLEAR command with CF = 1.

Sensor Matrix Mode

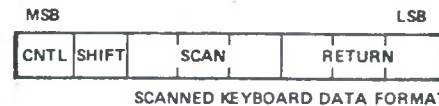
In Sensor Matrix mode, the debounce logic is inhibited. The status of the sensor switch is inputted directly to the Sensor RAM. In this way the Sensor RAM keeps an image of the state of the switches in the sensor matrix. Although debouncing is not provided, this mode has the advantage that the CPU knows how long the sensor was closed and when it was released. A keyboard mode can only indicate a validated closure. To make the software easier, the designer should functionally group the sensors by row since this is the format in which the CPU will read them. The IRQ line goes high if any sensor value change is detected at the end of a sensor matrix scan. The IRQ line is cleared by the first data read operation if the Auto-

Increment flag is set to zero, or by the End Interrupt command if the Auto-Increment flag is set to one.

Note: Multiple changes in the matrix Addressed by (SL₀₋₃ = 0) may cause multiple interrupts. (SL₀ = 0 in the Decoded Mode). Reset may cause the 8279 to see multiple changes.

Data Format

In the Scanned Keyboard mode, the character entered into the FIFO corresponds to the position of the switch in the keyboard plus the status of the CNTL and SHIFT lines (non-inverted). CNTL is the MSB of the character and SHIFT is the next most significant bit. The next three bits are from the scan counter and indicate the row the key was found in. The last three bits are from the column counter and indicate to which return line the key was connected.



In Sensor Matrix mode, the data on the return lines is entered directly in the row of the Sensor RAM that corresponds to the row in the matrix being scanned. Therefore, each switch position maps directly to a Sensor RAM position. The SHIFT and CNTL inputs are ignored in this mode. Note that switches are not necessarily the only thing that can be connected to the return lines in this mode. Any logic that can be triggered by the scan lines can enter data to the return line inputs. Eight multiplexed input ports could be tied to the return lines and scanned by the 8279.



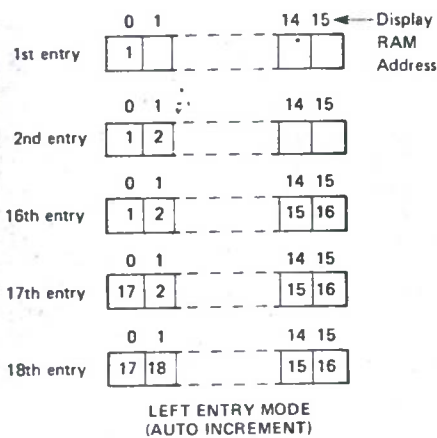
In Strobed Input mode, the data is also entered to the FIFO from the return lines. The data is entered by the rising edge of a CNTL/STB line pulse. Data can come from another encoded keyboard or simple switch matrix. The return lines can also be used as a general purpose strobed input.



Display

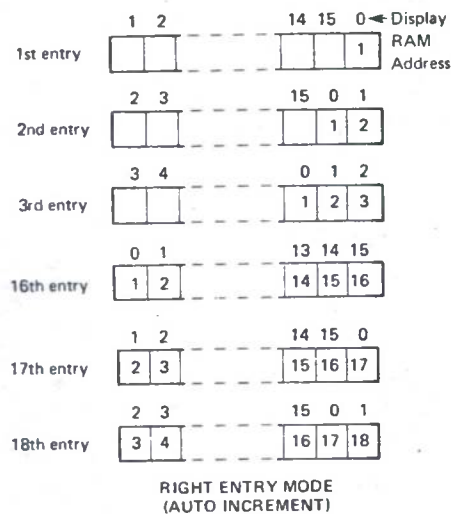
Left Entry

Left Entry mode is the simplest display format in that each display position directly corresponds to a byte (or nibble) in the Display RAM. Address 0 in the RAM is the left-most display character and address 15 (or address 7 in 8 character display) is the right most display character. Entering characters from position zero causes the display to fill from the left. The 17th (9th) character is entered back in the left most position and filling again proceeds from there.



Right Entry

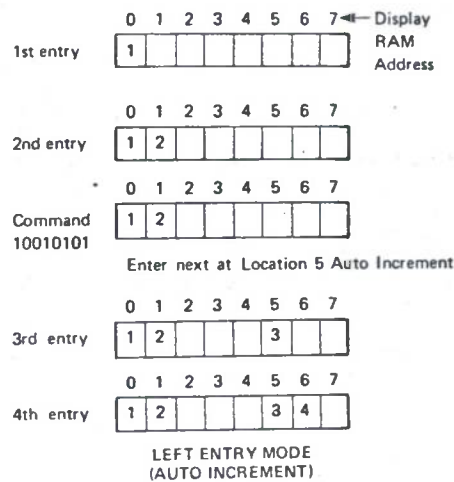
Right entry is the method used by most electronic calculators. The first entry is placed in the right most display character. The next entry is also placed in the right most character after the display is shifted left one character. The left most character is shifted off the end and is lost.



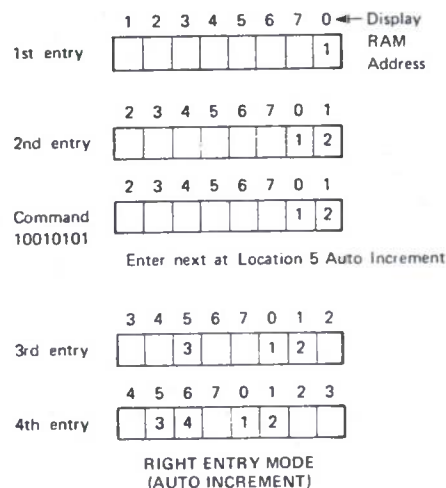
Note that now the display position and register address do not correspond. Consequently, entering a character to an arbitrary position in the Auto Increment mode may have unexpected results. Entry starting at Display RAM address 0 with sequential entry is recommended.

Auto Increment

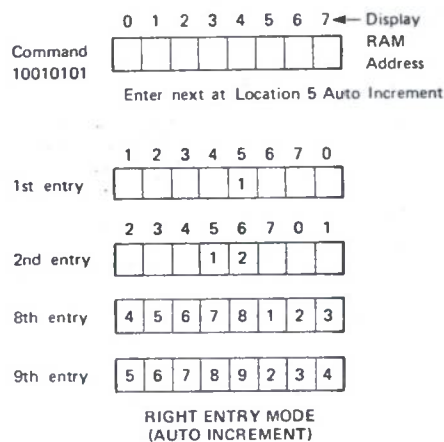
In the Left Entry mode, Auto Incrementing causes the address where the CPU will next write to be incremented by one and the character appears in the next location. With non-Auto Incrementing the entry is both to the same RAM address and display position. Entry to an arbitrary address in the Auto Increment mode has no undesirable side effects and the result is predictable:



In the Right Entry mode, Auto Incrementing and non Incrementing have the same effect as in the Left Entry except if the address sequence is interrupted:



Starting at an arbitrary location operates as shown below:



Entry appears to be from the initial entry point.

8/16 Character Display Formats

If the display mode is set to an 8 character display, the on duty-cycle is double what it would be for a 16 character display (e.g., 5.1 ms scan time for 8 characters vs. 10.3 ms for 16 characters with 100 kHz internal frequency).

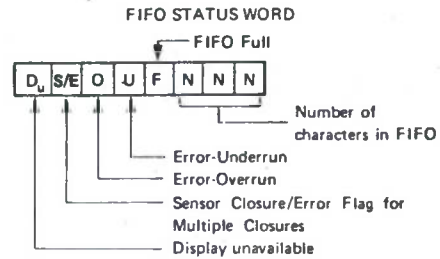
G. FIFO Status

FIFO status is used in the Keyboard and Strobed Input modes to indicate the number of characters in the FIFO and to indicate whether an error has occurred. There are two types of errors possible: overrun and underrun. Overrun occurs when the entry of another character into a full FIFO is attempted. Underrun occurs when the CPU tries to read an empty FIFO.

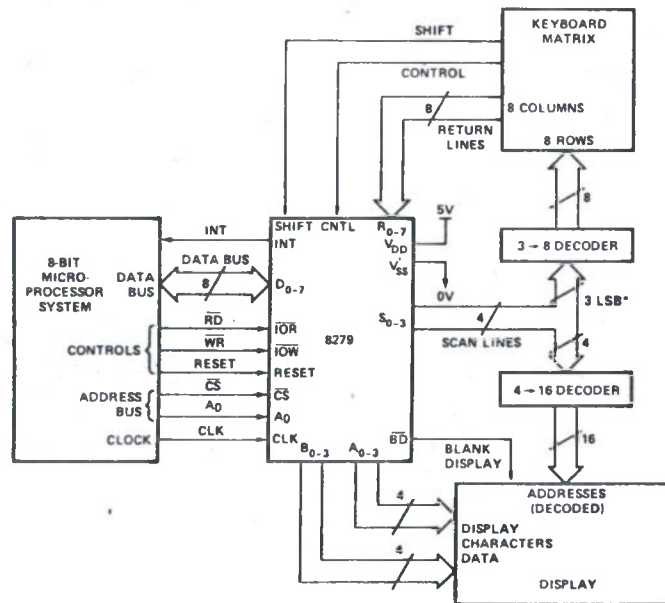
The FIFO status word also has a bit to indicate that the Display RAM was unavailable because a Clear Display or Clear All command had not completed its clearing operation.

In a Sensor Matrix mode, a bit is set in the FIFO status word to indicate that at least one sensor closure indication is contained in the Sensor RAM.

In Special Error Mode the S/E bit is showing the error flag and serves as an indication to whether a simultaneous multiple closure error has occurred.



APPLICATIONS



*Do not drive the keyboard decoder with the MSB of the scan lines.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature 0°C to 70°C
 Storage Temperature -65°C to 125°C
 Voltage on any Pin with :
 Respect to Ground -0.5V to +7V
 Power Dissipation 1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ± 5%, V_{CC} = +5V ± 10% (8279-5)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V _{IL1}	Input Low Voltage for Return Lines	-0.5	1.4	V	
V _{IL2}	Input Low Voltage for All Others	-0.5	0.8	V	
V _{IH1}	Input High Voltage for Return Lines	2.2		V	
V _{IH2}	Input High Voltage for All Others	2.0		V	
V _{OL}	Output Low Voltage		0.45	V	Note 1
V _{OH1}	Output High Voltage on Interrupt Line	3.5		V	Note 2
V _{OH2}	Other Outputs	2.4			
I _{IL1}	Input Current on Shift, Control and Return Lines		+10 -100	μA μA	V _{IN} = V _{CC} V _{IN} = 0V
I _{IL2}	Input Leakage Current on All Others		±10	μA	V _{IN} = V _{CC} to 0V
I _{OFL}	Output Float Leakage		±10	μA	V _{OUT} = V _{CC} to 0V
I _{CC}	Power Supply Current		120	mA	

Notes:

8279, I_{OL} = 1.6mA; 8279-5, I_{OL} = 2.2mA.
 8279, I_{OH} = -100μA; 8279-5, I_{OH} = -400μA.

CAPACITANCE

SYMBOL	TEST	TYP.	MAX.	UNIT	TEST CONDITIONS
C _{in}	Input Capacitance	5	10	pF	V _{in} = V _{CC}
C _{out}	Output Capacitance	10	20	pF	V _{out} = V _{CC}

A.C. CHARACTERISTICS $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{SS} = 0\text{V}$, (Note 1)**Bus Parameters****Read Cycle:**

Symbol	Parameter	8279		8279-5		Unit
		Min.	Max.	Min.	Max.	
t_{AR}	Address Stable Before $\overline{\text{READ}}$	50		0		ns
t_{RA}	Address Hold Time for $\overline{\text{READ}}$	5		0		ns
t_{RR}	$\overline{\text{READ}}$ Pulse Width	420		250		ns
$t_{RD}^{[2]}$	Data Delay from $\overline{\text{READ}}$		300		150	ns
$t_{AD}^{[2]}$	Address to Data Valid		450		250	ns
t_{DF}	$\overline{\text{READ}}$ to Data Floating	10	100	10	100	ns
t_{RCY}	Read Cycle Time	1		1		μs

Write Cycle:

Symbol	Parameter	8279		8279-5		Unit
		Min.	Max.	Min.	Max.	
t_{AW}	Address Stable Before $\overline{\text{WRITE}}$	50		0		ns
t_{WA}	Address Hold Time for $\overline{\text{WRITE}}$	20		0		ns
t_{WW}	$\overline{\text{WRITE}}$ Pulse Width	400		250		ns
t_{DW}	Data Set Up Time for $\overline{\text{WRITE}}$	300		150		ns
t_{WD}	Data Hold Time for $\overline{\text{WRITE}}$	40		0		ns
t_{WCY}	Write Cycle Time	1		1		μs

Notes:

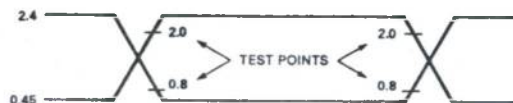
1. 8279, $V_{CC} = +5\text{V} \pm 5\%$; 8279-5, $V_{CC} = +5\text{V} \pm 10\%$.
 2. 8279, $C_L = 100\text{pF}$; 8279-5, $C_L = 150\text{pF}$.

Other Timings:

Symbol	Parameter	8279		8279-5		Unit
		Min.	Max.	Min.	Max.	
$t_{\phi W}$	Clock Pulse Width	230		120		nsec
t_{CY}	Clock Period	500		320		nsec

Keyboard Scan Time: 5.1 msec
 Keyboard Debounce Time: 10.3 msec
 Key Scan Time: 80 μsec
 Display Scan Time: 10.3 msec

Digit-on Time: 480 μsec
 Blanking Time: 160 μsec
 Internal Clock Cycle: 10 μsec

Input Waveforms For A.C. Tests

DS8861 MOS-to-LED 5-segment driver

DS8863 MOS-to-LED 8-digit driver

DS8963 MOS-to-LED 8-digit driver

general description

The DS8861, DS8863 and DS8963 are designed to be used in conjunction with MOS integrated circuits and common-cathode LED's in serially-addressed multi-digit displays.

The DS8861 is a 5-segment driver capable of sinking or sourcing up to 50 mA from each driver.

The DS8863 is an 8-digit driver. Each driver is capable of sinking up to 500 mA.

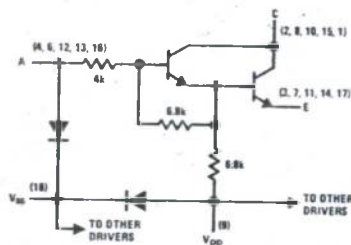
The DS8963 is identical to the DS8863 except it is intended for operation at up to 18V.

features

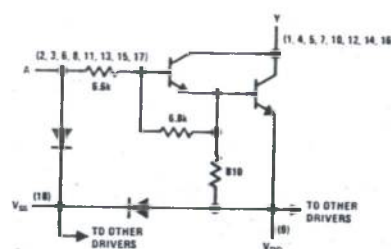
- 50 mA source or sink capability per driver, DS8861
- 500 mA sink capability per driver, DS8863, DS8963
- MOS compatibility (low input current)
- Low standby power
- High gain Darlington circuits

schematic and connection diagrams

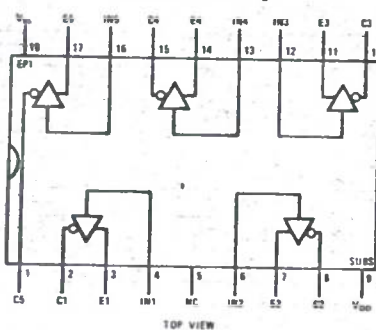
DS8861



DS8863/DS8963

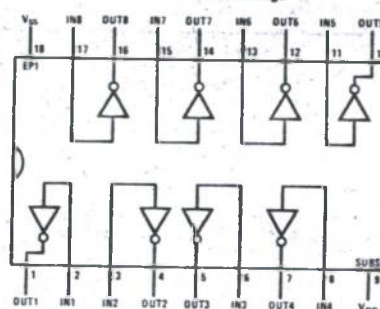


Dual-In-Line Package



TOP VIEW

Dual-In-Line Package



TOP VIEW

Order Numbers DS8861N, DS8863N or DS8963N
See NS Package N18A

absolute maximum ratings

	DS8861	DS8863	DS8963
Input Voltage Range (Note 1)	-5V to V_{SS}	-5V to V_{SS}	-5V to V_{SS}
Collector (Output) Voltage (Note 2)	10V	10V	18V
Collector (Output)-to-Input Voltage	10V	10V	18V
Emitter-to-Ground Voltage ($V_I \geq 5V$)	10V		
Emitter-to-Input Voltage	5V		
Voltage at V_{SS} Terminal With Respect to Any Other Device Terminal	10V	10V	18V
Collector (Output) Current			
Each Collector (Output)	50 mA	500 mA	500 mA
All Collectors (Output)	200 mA	600 mA	600 mA
Continuous Total Dissipation	800 mW	800 mW	800 mW
Operating Temperature Range	0°C to +70°C	0°C to +70°C	0°C to +70°C
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C	300°C	300°C

electrical characteristics

DS8861 ($V_{SS} = 10V$, $T_A = 0^\circ C$ to +70°C unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CEON} "ON" State Collector Emitter Voltage	Input = 8V through 1 k Ω , $V_E = 5V$, $T_A = 25^\circ C$ $I_C = 50$ mA		0.9	1.2	V
I_{COFF} "OFF" State Collector Current	$V_C = 10V$, $V_E = 0$ $I_{IN} = 40\mu A$ $V_{IN} = 0.7V$			100	μA
I_I Input Current at Maximum Input Voltage	$V_{IN} = 10V$, $V_E = 0$, $I_C = 20$ mA		2.2	3.3	mA
I_E Emitter Reverse Current	$V_{IN} = 0$, $V_E = 5V$, $I_C = 0$			100	μA
I_{SS} Current Into V_{SS} Terminal				1	mA

DS8863/DS8963 ($V_{SS} = 10V$, $T_A = 0^\circ C$ to +70°C unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OL} Low Level Output Voltage	$V_{IN} = 7V$, $I_{OUT} = 500$ mA $T_A = 25^\circ C$			1.5	V
I_{OH} High Level Output Current	$V_{OH} = 10V^*$ $I_{IN} = 40\mu A$ $V_{IN} = 0.5V$			250	μA
I_I Input Current at Maximum Input Voltage	$V_{IN} = 10V$, $I_{OL} = 20$ mA			2	mA
I_{SS} Current Into V_{SS} Terminal				1	mA

*18V for the DS8963

switching characteristics

DS8861 ($V_{SS} = 7.5V$, $T_A = 25^\circ C$)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH} Propagation Delay Time, Low-to-High Level Output (Collector)	$V_{IH} = 4.5V$, $V_E = 0$		100		ns
t_{PHL} Propagation Delay Time, High-to-Low Level Output (Collector)	$R_L = 200\Omega$, $C_L = 15$ pF		20		ns

DS8863/DS8963 ($V_{SS} = 7.5V$, $T_A = 25^\circ C$)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH} Propagation Delay Time, Low-to-High Level Output	$V_{IH} = 8V$, $R_L = 21\Omega$,		300		ns
t_{PHL} Propagation Delay Time, High-to-Low Level Output	$C_L = 15$ pF		30		ns

Note 1: The input is the only device terminal which may be negative with respect to ground.

Note 2: Voltage values are with respect to network ground terminal unless otherwise noted.

8T38-B,F

DIGITAL 8T SERIES INTERFACE TTL/MSI

DESCRIPTION

The 8T38 is a quad bus transceiver with a common two input disable control for the drivers. Open collector driver outputs together with low input requirements for the receivers offer extreme versatility in low cost bus organized systems.

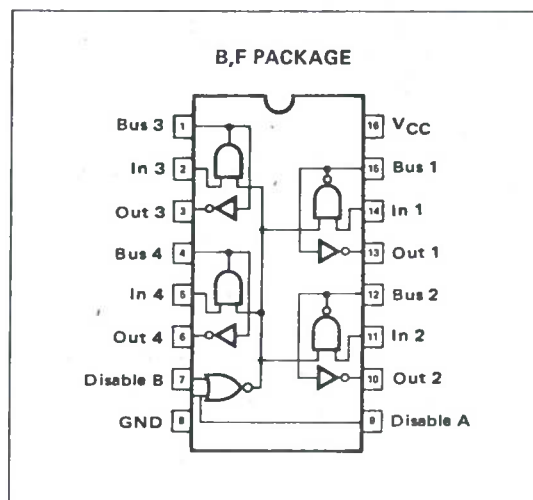
Busses may be terminated at both ends such that up to 100 driver/receiver pairs can utilize a common data bus. The receiver incorporates hysteresis to provide maximum noise immunity. In addition the receiver does not load the bus when $V_{CC} = 0$.

In those applications where only bus receivers are required the 8T380 quad bus receiver or the 8T37 hex bus receiver should be considered.

FEATURES

- RECEIVER HYSTERESIS – 1V TYPICAL
- RECEIVER NOISE IMMUNITY – 2V
- RECEIVER INPUT CURRENT – $20\mu A$ TYPICAL (FOR NORMAL V_{CC} AND $V_{CC} = 0V$)
- RECEIVER
 - SINK – 16mA AT 0.4V
 - SOURCE – 5.2mA AT 2.4V
- DRIVER
 - SINK – 50mA AT 0.7V
- DRIVERS HAVE OPEN COLLECTOR OUTPUTS
- DRIVES 100Ω TERMINATED BUSES
- 7400 SERIES COMPATIBLE
- PIN COMPATIBLE WITH DM8838

PIN CONFIGURATION (Top View)



TRUTH TABLE

MODE	DISABLE A	DISABLE B	DRIVER IN	BUS	RECEIVER OUT
RECEIVE	1	X	X	1	0
RECEIVE	X	1	X	0	1
DRIVE	0	0	1	0	1
DRIVE	0	0	0	1	0

AC ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ C$, $V_{CC} = 5.0V$)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Disable to Bus	11	19	30	ns
t_{PLH}	Disable to Bus	15	23	35	ns
t_{PHL}	Driver to Bus	5	12	20	ns
t_{PLH}	Driver to Bus	5	12	25	ns
t_{PHL}	Bus to Receiver	5	14	25	ns
t_{PLH}	Bus to Receiver	12	27	40	ns

DC ELECTRICAL CHARACTERISTICS (Over Recommended Voltage and Temperature Range)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOH "1" Output Voltage Receiver	$I_{out} = -400\mu A$ $V_{CC} = \text{Min.}$	2.4			V
VOL "0" Output Voltage Bus Driver	$I_{out} = 50\text{mA}$ $V_{CC} = \text{Min.}$		0.25	0.7	V
	$I_{out} = 16\text{mA}$ $V_{CC} = \text{Min.}$			0.4	V
VIH "1" Input Voltage Disable	$V_{CC} = \text{Min.}$	2.0			V
	$V_{CC} = \text{Min.}$	2.0			V
VIL "0" Input Voltage Disable	$V_{CC} = \text{Min.}$			0.8	V
	$V_{CC} = \text{Min.}$			0.8	V
IIH "1" Input Current Disable & Driver	$V_{in} = 2.4\text{V}$ $V_{CC} = \text{Max.}$			50	μA
	$V_{in} = 4.0\text{V}$ $V_{CC} = \text{Max.}$		20	100	μA
Bus Power ON	$V_{in} = 4.0\text{V}$ $V_{CC} = 0$		2	100	μA
	$V_{in} = 4.0\text{V}$ $V_{CC} = 0$			100	μA
IIH "0" Input Current Driver	$V_{in} = 0.4\text{V}$ $V_{CC} = \text{Max.}$			-1.6	mA
VT+ High Receiver Threshold	$V_{CC} = \text{Min.}$	1.80	2.25	2.50	V
VT- Low Receiver Threshold	$V_{CC} = \text{Max.}$	1.05	1.30	1.55	V
VImax Max Input Voltage All Inputs	$I_{in} \leq 1\text{mA}$			5.5	V
VICL Input Clamp Voltage All Inputs	$I_{in} = -12\text{mA}$ $V_{CC} = \text{Min.}$		-1.0	-1.5	V
IOS Output Short Circuit Current; Receiver	$V_{out} = 0$ $V_{CC} = \text{Max.}$	-18	-33	-55	mA
ICC Power Dissipation/Supply Current	Disable = 0V, $V_{CC} = \text{Max.}$ Driver = 2.0V		210 40	315 60	mW mA

DESCRIPTION

The 8T363 Dual circuit incorporating gate output. The and employs thresholds. The compatible with DTL

APPLICATION

ZERO-CROSSING
HIGH STABILITY
BI-DIRECTIONAL
FREQUENCY DO
STABLE-LOW FR
LINEAR AMPLIF
FREQUENCY TO

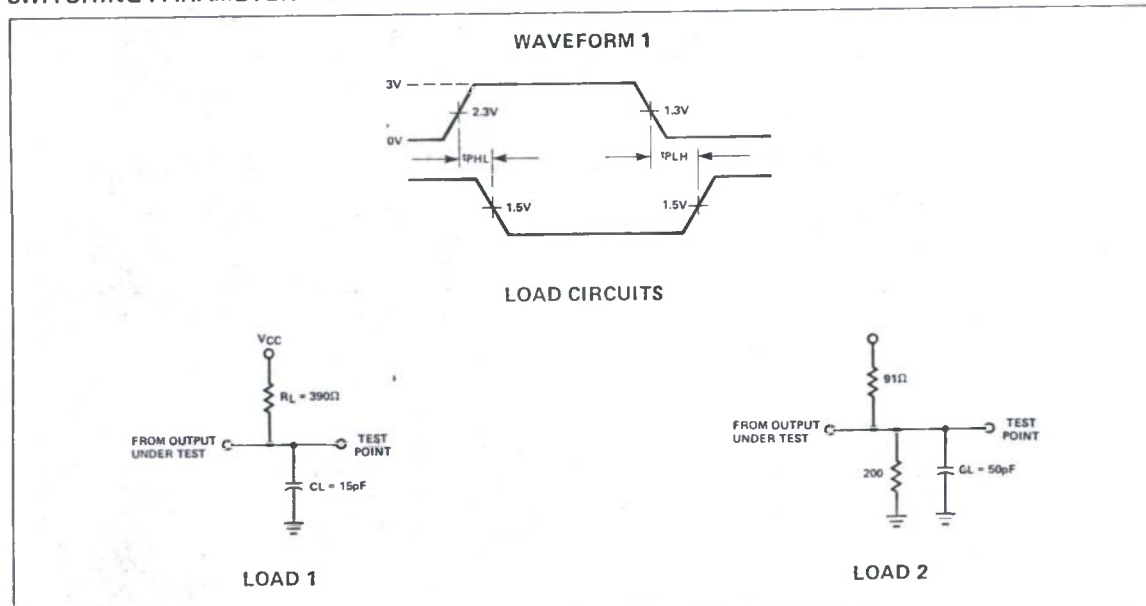
ABSOLUTE MA

Input Voltage
Output Voltage
 V_{CC}
Input Current
Output Current
Storage Temperatu
Operating Tempera
V-

Maximum ratings are
be impaired.

CIRCUIT SCHE

SWITCHING PARAMETER MEASUREMENT INFORMATION



96S02 96LS02

DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION — The 96S02 and 96LS02 are dual retriggerable and resettable monostable multivibrators. These one-shots provide exceptionally wide delay range, pulse width stability, predictable accuracy and immunity to noise. The pulse width is set by an external resistor and capacitor. Resistor values up to 1.0 M Ω for the 96LS02 and 2.0 M Ω for the 96S02 reduce required capacitor values. Hysteresis is provided on both trigger inputs of the 96LS02 and on the positive trigger input of the 96S02 for increased noise immunity.

- **REQUIRED TIMING CAPACITANCE REDUCED BY FACTORS OF 10 TO 100 OVER CONVENTIONAL DESIGNS**
- **BROAD TIMING RESISTOR RANGE — 1.0 k Ω to 2.0 M Ω**
- **OUTPUT PULSE WIDTH IS VARIABLE OVER A 2000:1 RANGE BY RESISTOR CONTROL**
- **PROPAGATION DELAY OF 35 ns 96LS02, 12 ns 96S02**
- **0.3 V HYSTERESIS ON TRIGGER INPUTS**
- **OUTPUT PULSE WIDTH INDEPENDENT OF DUTY CYCLE**
- **35 ns TO ∞ OUTPUT PULSE WIDTH RANGE**

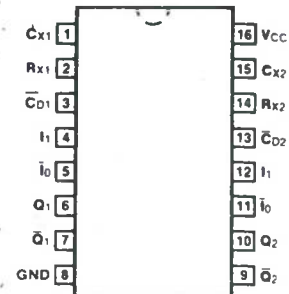
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0 \text{ V} \pm 10\%$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	96S02PC, 96LS02PC		9B
Ceramic DIP (D)	A	96S02DC, 96LS02DC	96S02DM, 96LS02DM	6B
Flatpak (F)	A	96S02FC, 96LS02FC	96S02FM, 96LS02FM	4L

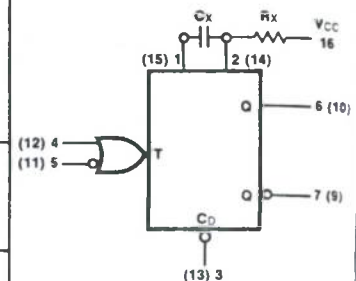
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	96S (U.L.) HIGH/LOW	96LS (U.L.) HIGH/LOW
$\bar{I}_0$	Trigger Input (Active Falling Edge)	0.5/0.625	
I_0	Schmitt Trigger Input (Active Falling Edge)		0.5/0.25
I_1	Schmitt Trigger Input (Active Rising Edge)	0.5/0.625	0.5/0.25
$\bar{C}_D$	Direct Clear Input (Active LOW)	0.5/0.625	0.5/0.25
Q	True Pulse Output	25/12.5	10/5.0 (2.5)
$\bar{Q}$	Complementary Pulse Output	25/12.5	10/5.0 (2.5)

CONNECTION DIAGRAM PINOUT A



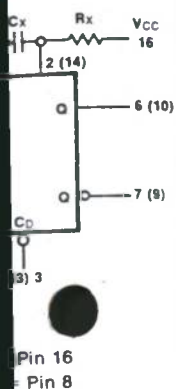
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

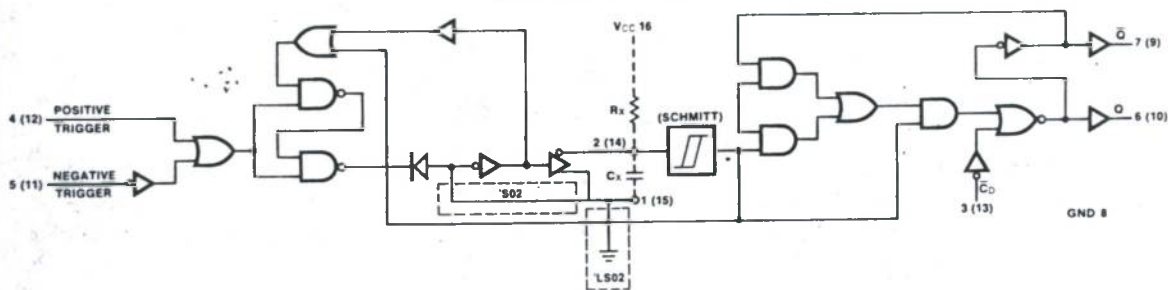
DIAGRAM
OUT A

SYMBOL

LS (U.L.)
HIGH/LOW

0.5/0.25
0.5/0.25
0.5/0.25
10/5.0
(2.5)
10/5.0
(2.5)

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The 96S02 and 96LS02 dual retriggerable resettable monostable multivibrators have two dc coupled trigger inputs per function, one active LOW ($\bar{I}_0$) and one active HIGH (I_1). The I_1 input of both circuit types and the $\bar{I}_0$ input of the 96LS02 utilize an internal Schmitt trigger with hysteresis of 0.3 V to provide increased noise immunity. The use of active HIGH and LOW inputs allows either rising or falling edge triggering and optional non-retriggerable operation. The inputs are dc coupled making triggering independent of input transition times. When input conditions for triggering are met the Q output goes HIGH and the external capacitor is rapidly discharged and then allowed to recharge. An input trigger which occurs during the timing cycle will retrigger the circuit and result in Q remaining HIGH. The output pulse may be terminated (Q to the LOW state) at any time by setting the Direct Clear input LOW. Retriggering may be inhibited by tying the $\bar{Q}$ output to $\bar{I}_0$ or the Q output to I_1 . Differential sensing techniques are used to obtain excellent stability over temperature and power supply variations and a feedback Darlington capacitor discharge circuit minimizes pulse width variation from unit to unit. Schottky TTL output stages provide high switching speeds and output compatibility with all TTL logic families.

Operation Notes

TIMING

1. An external resistor (R_x) and an external capacitor (C_x) are required as shown in the Logic Diagram. The value of R_x may vary from 1.0 k Ω to 1.0 M Ω (96LS02) or 2.0 M Ω (96S02).
2. The value of C_x may vary from 0 to any necessary value available. If, however, the capacitor has significant leakage relative to V_{CC}/R_x the timing equations may not represent the pulse width obtained.
3. Polarized capacitors may be used directly. The (+) terminal of a polarized capacitor is connected to pin 1 (15), the (-) terminal to pin 2 (14) and R_x . Pin 1 (15) will remain positive with respect to pin 2 (14) during the timing cycle. In the 96S02, however, during quiescent (non-triggered) conditions, pin 1 (15) may go negative with respect to pin 2 (14) depending on values of R_x and V_{CC} . For values of $R_x \geq 10$ k Ω the maximum amount of capacitor reverse polarity, pin 1 (15) negative with respect to pin 2 (14) is 500 mV. Most tantalum electrolytic capacitors are rated for safe reverse bias operation up to 5% of their working forward voltage rating; therefore, capacitors having a rating of 10 WVdc or higher should be used with the 96S02 when $R_x \geq 10$ k Ω .
4. The output pulse width t_w for $R_x \geq 10$ k Ω and $C_x \geq 1000$ pF is determined as follows:
 (96S02) $t_w = 0.55 R_x C_x$
 (96LS02) $t_w = 0.43 R_x C_x$
 Where R_x is in k Ω , C_x is in pF, t is in ns or R_x is in k Ω , C_x is in μ F, t is in ms.
5. The output pulse width for $R_x < 10$ k Ω or $C_x < 1000$ pF should be determined from pulse width versus C_x or R_x graphs.
6. To obtain variable pulse width by remote trimming, the following circuit is recommended:

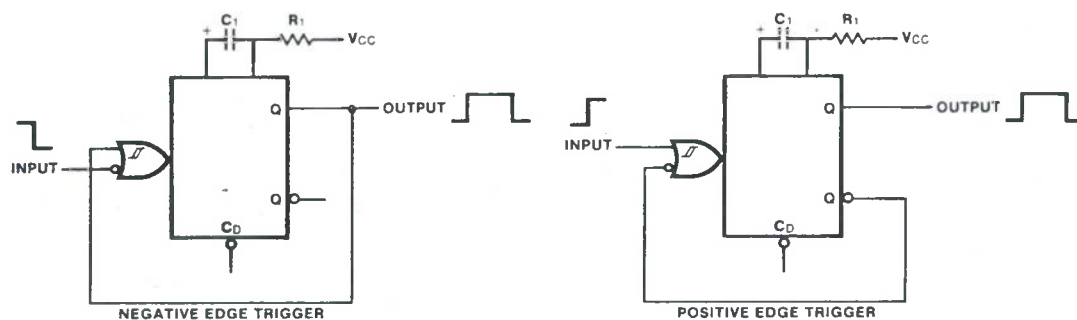


Operation Notes (Cont'd)

7. Under any operating condition, C_X and R_X (Min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
8. V_{CC} and ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and ground leads do not cause interaction between one shots. Use of a $0.01\ \mu\text{F}$ to $0.1\ \mu\text{F}$ bypass capacitor between V_{CC} and ground located near the circuit is recommended.

TRIGGERING

1. The minimum negative pulse width into $\bar{I}_0$ is 8.0 ns; the minimum positive pulse width into I_1 is 12 ns.
2. Input signals to the 96S02 exhibiting slow or noisy transitions should use the positive trigger input I_1 which contains a Schmitt trigger. Input signals to the 96LS02 exhibiting slow or noisy transitions can use either trigger as both are Schmitt triggers.
3. When non-retriggerable operation is required, i.e., when input triggers are to be ignored during quasi-stable state, input latching is used to inhibit retriggering.



4. An overriding active LOW level direct clear is provided on each multivibrator. By applying a LOW to the clear, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW. A LOW-to-HIGH transition on $\bar{C}_D$ will not trigger the 96S02 or 96LS02. If the $\bar{C}_D$ input goes HIGH coincident with a trigger transition, the circuit will respond to the trigger.

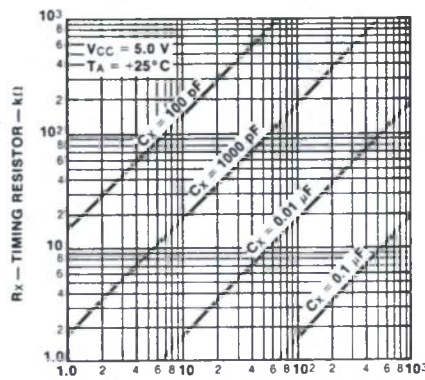
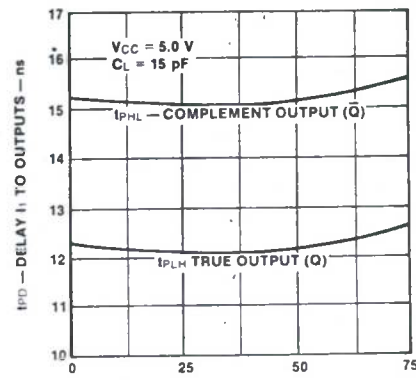
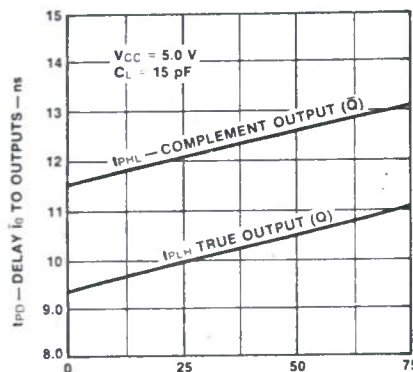
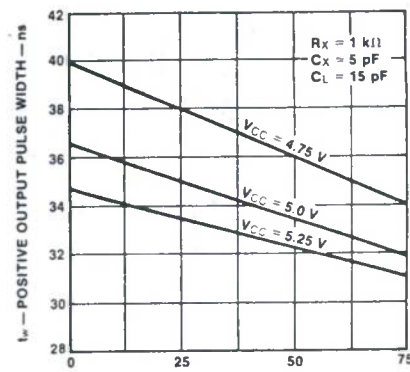
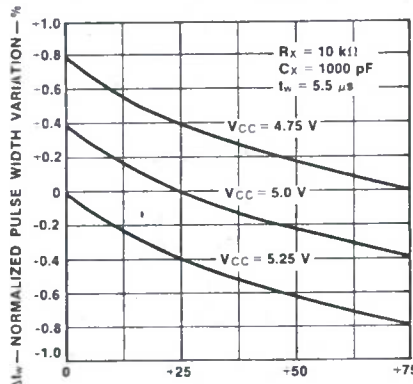
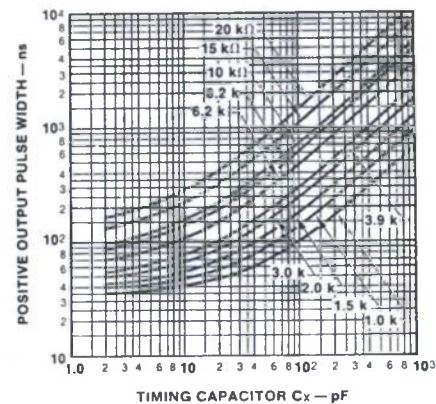
TRIGGERING TRUTH TABLE

PIN NO'S.			OPERATION
5 (11)	4 (12)	3 (13)	
H $\rightarrow$ L	L	H	Trigger
H	L $\rightarrow$ H	H	Trigger
X	X	L	Reset

H = HIGH Voltage Level $\geq V_{IH}$ L = LOW Voltage Level $\leq V_{IL}$

X = Immaterial (either H or L)

H $\rightarrow$ L = HIGH to LOW Voltage Level transitionL $\rightarrow$ H = LOW to HIGH Voltage Level transition

TYPICAL CHARACTERISTICS
96S02OUTPUT t_w vs R_X and C_X  t_w - OUTPUT PULSE WIDTH - μ s I_1 DELAY TIME vs T_A  T_A - AMBIENT TEMPERATURE - $^{\circ}$ C $\bar{t}_0$ DELAY TIME vs T_A  T_A - AMBIENT TEMPERATURE - $^{\circ}$ COUTPUT t_w vs T_A  T_A - AMBIENT TEMPERATURE - $^{\circ}$ CNORMALIZED Δt_w vs T_A  T_A - AMBIENT TEMPERATURE - $^{\circ}$ CPULSE WIDTH vs $R_X C_X$ 

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	96S		96LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
V_{T+}	Positive-going Threshold Voltage, $\bar{I}_0$, I_1 (96LS02) I_1 (96S02)	2.0		2.0		V	$V_{CC} = 5.0$ V
V_{T-}	Negative-going Threshold Voltage $\bar{I}_0$, I_1 (96LS02) I_1 (96S02)	XM	0.8	0.7		V	$V_{CC} = 5.0$ V
		XC	0.8	0.8			
V_{OH}	Output HIGH Voltage	XM	2.7	2.5		V	$V_{CC} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -400 \mu\text{A}$ ('LS02) $I_{OH} = -1.0$ mA ('S02)
		XC	2.7	2.7			
V_{OL}	Output LOW Voltage	XM	0.5	0.5		V	$V_{CC} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL}
		XC	0.5	0.4			
V_{CX}	Capacitor Voltage Pin 1 (15) Referenced to Pin 2 (14)	-0.85	3.0	0	3.0	V	$R_X = 1.0$ k Ω $V_{CC} = 4.75$ V $R_X = > 10$ k Ω to 5.25 V $R_X > 1.0$ M Ω
		-0.5	3.0	0	3.0		
		-0.4	3.0	0	3.0		
I_{IH}	Input HIGH Current	20		20		μA	$V_{IN} = 2.7$ V $V_{IN} = 5.5$ V ('S02) $V_{CC} = \text{Max}$ $V_{IN} = 10$ V ('LS02)
		0.1		0.1		mA	
I_{IL}	Input LOW Current	-1.0		-0.4		mA	$V_{IN} = 0.4$ V, $V_{CC} = \text{Max}$
I_{OS}	Output Short Circuit Current	-40	-100	-20	-100	mA	$V_{CC} = \text{Max}$, $V_{OUT} = 0$ V
I_{CC}	Power Supply Current	75		36		mA	$V_{IN} = \text{Open}$, $V_{CC} = \text{Max}$

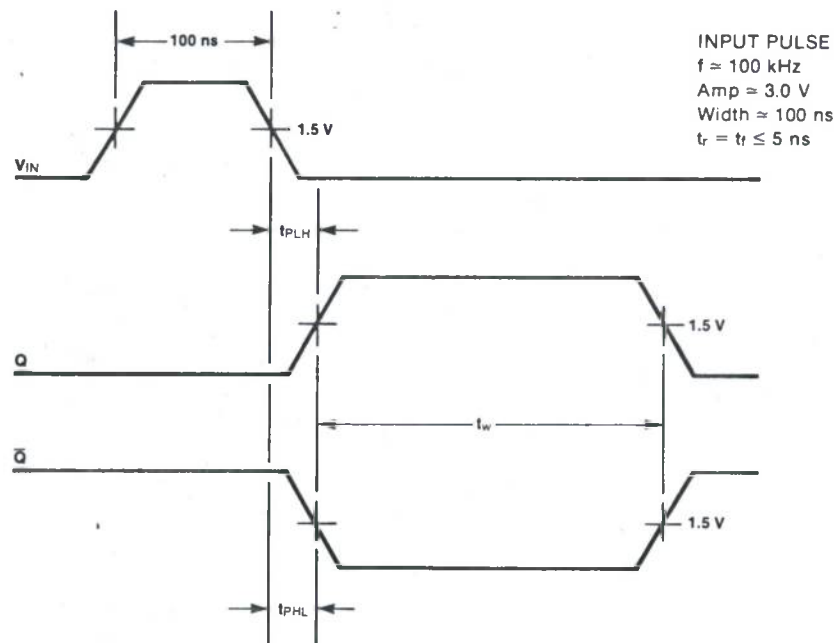


Fig. a

AC CHARACTERISTICS: $V_{CC} = +5.0\text{ V}$, $T_A = +25^\circ\text{C}$ (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER		96S		96LS		UNITS	CONDITIONS
			C _L = 15 pF		C _L = 15 pF			
			Min	Max	Min	Max		
t _{PLH}	Propagation Delay I ₀ to Q		15		55		ns	Fig. a
t _{PHL}	Propagation Delay I ₀ to Q̄		19		50		ns	
t _{PLH}	Propagation Delay I ₁ to Q		19		60		ns	
t _{PHL}	Propagation Delay I ₁ to Q̄		20		55		ns	
t _{PHL}	Propagation Delay C _D to Q		20		30		ns	
t _{PLH}	Propagation Delay C _D to Q̄		14		35		ns	
t _w (L)	I ₀ Pulse Width LOW		8.0		15		ns	
t _w (H)	I ₁ Pulse Width HIGH		12		30		ns	
t _w (L)	C _D Pulse Width LOW		7.0		22		ns	
t _w (H)	Minimum Q Pulse Width HIGH		30	45	25	55	ns	R _x = 1.0 kΩ, C _x = 10 pF including jig and stray
t _w	Q Pulse Width		5.2	5.8	4.1	4.5	μs	R _x = 10 kΩ, C _x = 1000 pF
R _x	Timing Resistor Range*		1.0	2000	1.0	1000	kΩ	T _A = -55°C to +125°C, V _{CC} = 4.5 V to 5.5 V
t	Change in Q Pulse Width over Temperature	XM XC	1.0		3.0 1.0		%	R _x = 10 kΩ, C _x = 1000 pF
t	Change in Q Pulse Width over V _{CC} Range		1.0		0.8 1.5		%	T _A = 25°C, V _{CC} = 4.75 V to 5.25 V, R _x = 10 kΩ, C _x = 1000 pF T _A = 25°C, V _{CC} = 4.5 V to 5.5 V, R _x = 10 kΩ, C _x = 1000 pF

*Applies only over commercial V_{CC} and T_A range for 96S02.

ADDRESS

DESCRIPTION
for multiplexed
addresses (or
applied address
refresh counter)
refresh may be
suitable for use
operates from
a 0°C to $+75^\circ\text{C}$

- SIMPLIFIES
- REDUCES P
- DRIVES HIGH
- USE FOR DI
- STANDARD
- LOW POWER

ORDERING CO

PKGS	PIN OUT
Plastic DIP (P)	A
Ceramic DIP (D)	A
Flatpak (F)	A

INPUT LOADING

PIN NAMES

$A_0 - A_5$
 $A_6 - A_{11}$
 $\bar{C}_P$
 $\bar{R}_E$
 $\bar{R}_S$
 $\bar{Z}_D$
 $\bar{O}_0 - \bar{O}_5$

Performance Curves NZF

See Page 4-49

N-CHANNEL SILICON JUNCTION FIELD-EFFECT TRANSISTORS



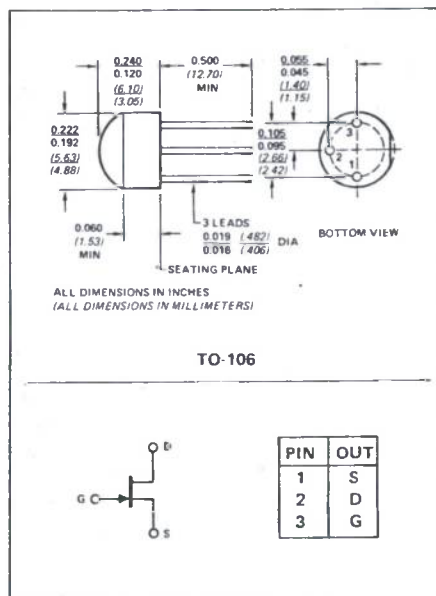
FOR GENERAL-PURPOSE AMPLIFIER APPLICATIONS

This series of epoxy-encapsulated FETs is characterized for low and medium frequency small-signal amplifier applications which require high transconductance and low input capacitance.

- Typical transconductance $g_{fs} = 10,000 \mu\text{mho}$ (E211 and E212)
- Typical input capacitance $C_{iss} = 5 \text{ pF}$

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-25 V
Gate Current	10 mA
Total Device Dissipation (25°C Free-Air Temperature)	350 mW
Power Derating (to +125°C)	3.5 mW/°C
Storage Temperature Range	-55 to +125°C
Operating Temperature Range	-55 to +125°C
Lead Temperature (1/16" from case for 10 seconds)	300°C



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic			E210			E211			E212			Unit	Test Conditions	
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	S	I_{GSS}			-100			-100			-100	pA	$V_{DS} = 0, V_{GS} = -15 \text{ V}$	
2	T	$V_{GS(off)}$			-3	-2.5		-4.5	-4		-6	V	$V_{DS} = 15 \text{ V}, I_D = 1 \text{ nA}$	
3	A	BV_{GSS}			-25			-25			-25		$V_{DS} = 0, I_G = -1 \mu\text{A}$	
4	I	I_{DSS}			15	7		20	15		40	mA	$V_{DS} = 15 \text{ V}, V_{GS} = 0$	
5	C	I_G			-10			-10			-10	pA	$V_{DG} = 10 \text{ V}, I_D = 1 \text{ mA}$	
6		g_{fs}			12,000	7,000		12,000	7,000		12,000	μmho	$V_{DS} = 15 \text{ V}, V_{GS} = 0$	$f = 1 \text{ kHz}$
7	D	g_{os}			150			200			200			
8	N	C_{iss}			5.0			5.0			5.0	pF		$f = 1 \text{ MHz}$
9	A	C_{rss}			1.5			1.5			1.5			
10	M	$\bar{e}_n$			10			10			10	$\frac{nV}{\sqrt{Hz}}$		$f = 1 \text{ kHz}$

NOTES:

1. Approximately doubles for every 10°C increase in T_A .
2. Pulse test duration = 2 ms.

NZF



MOTOROLA

MC3459

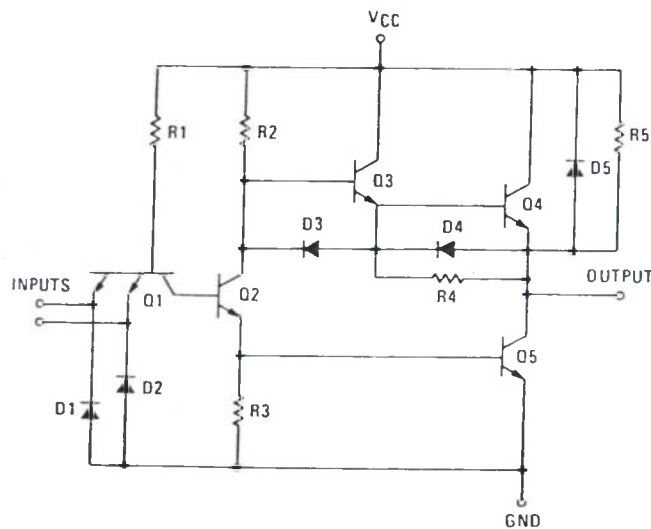
Specifications and Applications Information

QUAD NMOS MEMORY ADDRESS DRIVER

The MC3459 is designed for high-speed driving of the highly capacitive Address select inputs for NMOS Memories. It is also useful in numerous applications requiring a high-current MTTL NAND gate. It is pin-compatible with the popular MC7400 Quad NAND gate.

- Fast Propagation Delay Time —
20 ns Typical with 360 pF Load
- Output Voltages Compatible with NMOS Memories
- Inputs Compatible in MTTL and MDTL Logic Families
- Output Loading Factor — 50

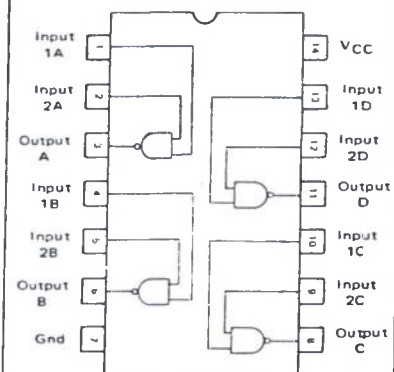
REPRESENTATIVE CIRCUIT SCHEMATIC
(1/4 of Circuit Shown)



QUAD NMOS ADDRESS LINE DRIVER

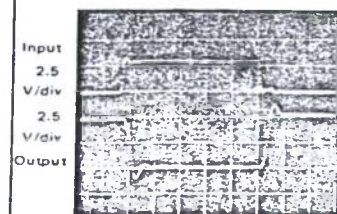
SILICON MONOLITHIC
INTEGRATED CIRCUIT

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO 116



P SUFFIX
PLASTIC PACKAGE
CASE 646

TYPICAL OPERATION



$V_{CC} = 5.0 \text{ V}$
 $T_A = 25^\circ \text{C}$
 $C_L = 360 \text{ pF}$
 $R_S = 0 \Omega$

MC3459

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.5	Vdc
Input Voltage	V_I	5.5	Vdc
Power Dissipation (Package Limitation)			
Ceramic Package @ $T_A = 25^\circ\text{C}$	P_D	1000	mW
Derate above $T_A = 25^\circ\text{C}$	$1/R_{\theta JA}$	6.6	mW/ $^\circ\text{C}$
Plastic Package @ $T_A = 25^\circ\text{C}$	P_D	830	mW
Derate above $T_A = 25^\circ\text{C}$	$1/R_{\theta JA}$	6.6	mW/ $^\circ\text{C}$
Ceramic Package @ $T_C = 25^\circ\text{C}$	P_D	3.0	Watts
Derate above $T_C = 25^\circ\text{C}$	$1/R_{\theta JC}$	20	mW/ $^\circ\text{C}$
Plastic Package @ $T_C = 25^\circ\text{C}$	P_D	1.8	Watts
Derate above $T_C = 25^\circ\text{C}$	$1/R_{\theta JC}$	14	mW/ $^\circ\text{C}$
Operating Ambient Temperature Range	T_A	0 to 70	$^\circ\text{C}$
Junction Temperature	T_J		$^\circ\text{C}$
Ceramic Package		175	
Plastic Package		150	
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $4.75\text{ V} < V_{CC} \leq 5.25\text{ V}$ and $0 < T_A \leq 70^\circ\text{C}$)

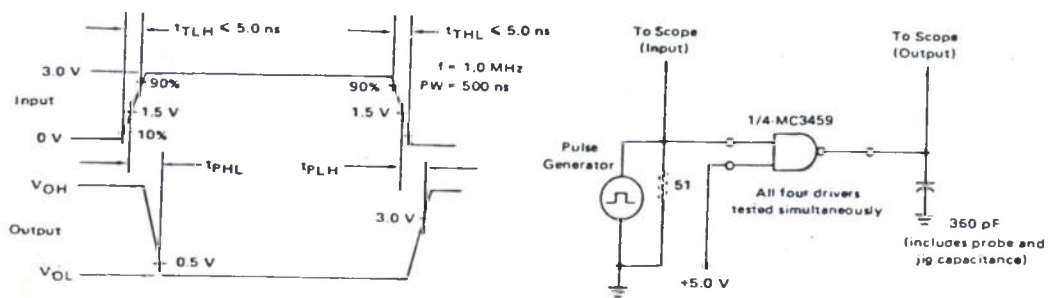
Characteristic	Symbol	Min	Typ(1)	Max	Unit
Input Voltage — High Logic State	V_{IH}	2.0	—	—	V
Input Voltage — Low Logic State	V_{IL}	—	—	0.8	V
Input Current — High Logic State ($V_{CC} = 5.25\text{ V}$, $V_{IH} = 2.4\text{ V}$) ($V_{CC} = 5.25\text{ V}$, $V_{IH} = 5.5\text{ V}$)	I_{IH1} I_{IH2}	—	—	80 2.0	μA mA
Input Current — Low Logic State ($V_{CC} = 5.25\text{ V}$, $V_{IL} = 0.4\text{ V}$)	I_{IL}	—	—	-3.6	mA
Input Clamp Voltage ($I_{IC} = -12\text{ mA}$)	V_{IC}	—	—	-1.5	V
Output Voltage — High Logic State ($V_{CC} = 4.75\text{ V}$, $V_{IL} = 0.8\text{ V}$, $I_{OH} = -640\text{ }\mu\text{A}$) ($V_{CC} = 4.75\text{ V}$, $V_{IL} = 0.8\text{ V}$, $I_{OH} = -2.0\text{ mA}$)	V_{OH1} V_{OH2}	3.2 2.4	—	—	V
Output Clamp Voltage ($V_{CC} = 5.25\text{ V}$, $V_{IL} = 0\text{ V}$, $I_{OC} = 5.0\text{ mA}$)	V_{OC}	—	5.8	6.75	V
Output Voltage — Low Logic State ($V_{CC} = 4.75\text{ V}$, $V_{IH} = 2.0\text{ V}$, $I_{OL} = 640\text{ }\mu\text{A}$) ($V_{CC} = 4.75\text{ V}$, $V_{IH} = 2.0\text{ V}$, $I_{OL} = 80\text{ mA}$)	V_{OL1} V_{OL2}	— —	— —	0.3 0.7	V
Power Supply Current — Outputs High Logic State ($V_{CC} = 5.25\text{ V}$, $V_{IL} = 0\text{ V}$)	I_{CCH}	—	12	18	mA
Power Supply Current — Outputs Low Logic State ($V_{CC} = 5.25\text{ V}$, $V_{IH} = 5.0\text{ V}$)	I_{CCL}	—	85	122	mA

SWITCHING CHARACTERISTICS (Unless otherwise noted, $V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 360\text{ pF}$)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — High to Low Logic State	t_{PHL}	—	21	32	ns
Propagation Delay Time — Low to High Logic State	t_{PLH}	—	16	26	ns

(1) Typical values measured at $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$.

FIGURE 1 - TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES



TYPICAL PERFORMANCE CURVES

FIGURE 2 - POWER CONSUMPTION versus OPERATING FREQUENCY

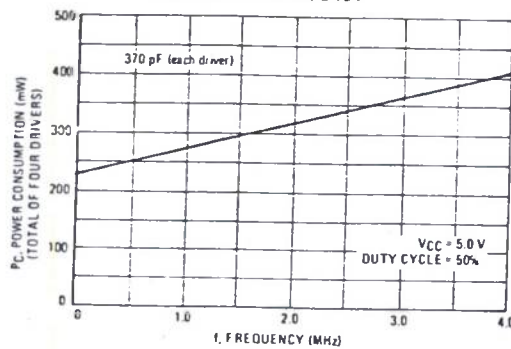


FIGURE 3 - OUTPUT VOLTAGE - HIGH LOGIC STATE versus OUTPUT CURRENT

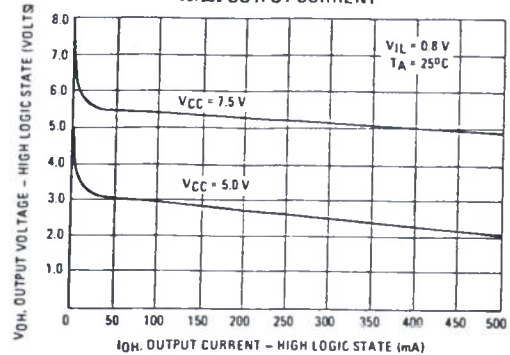


FIGURE 4 - OUTPUT VOLTAGE - HIGH LOGIC STATE versus OUTPUT CURRENT (Expanded Scale)

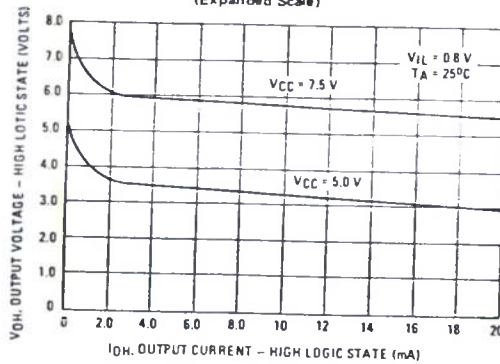
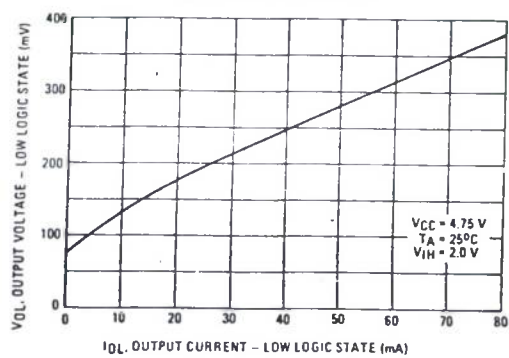


FIGURE 5 - OUTPUT VOLTAGE - LOW LOGIC STATE versus OUTPUT CURRENT



MC3459

APPLICATIONS SUGGESTIONS

A majority of the new N-Channel MOS memories have TTL logic compatible inputs that exhibit extremely low input current and capacitance (typically 5 pF to 10 pF). However, in a typical memory system (Figure 6) where some of the inputs such as Address lines have to be common, the total parallel input capacitance can be over 300 pF. Standard TTL logic gates have insufficient current drive capability to rapidly switch a high capacitive load; a high speed buffer, such as the MC3459, is required.

A considerable amount of noise can be generated during switching due to the high speed and high current drive capability of the MC3459. The high capacitive discharge current during the high to low transition, plus current spikes can result in a considerable amount of noise being generated on the ground lead. Current spikes are due to both the upper and lower output drive transistors being on for a short period of time during switching. This causes a very low impedance path between V_{CC} and ground.

In order to minimize the effects of these currents, the following layout rules should be followed:

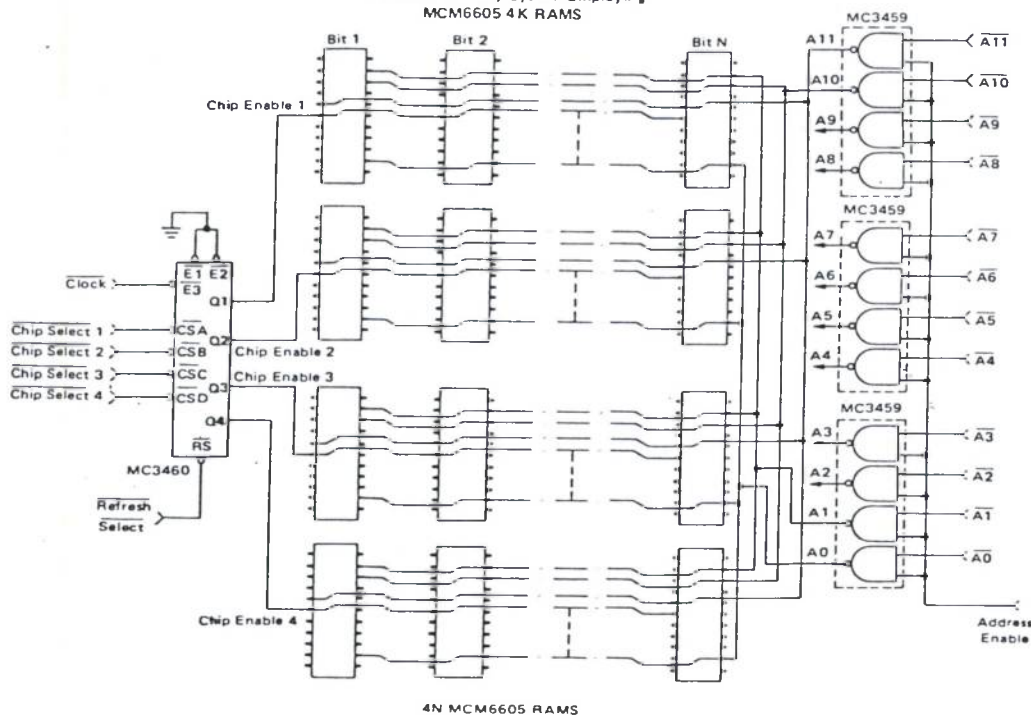
1. The V_{CC} supply pin of each package should be bypassed with a low inductance 0.01 μ F capacitor. The 0.01 μ F capacitor will sustain the high surge currents required during switching.
2. There is a large amount of current out of the ground node during switching — the noise seen at this node

will be proportional to the ground impedance. The impedance of the ground bus can be reduced by increasing its width. At least a 50 mil ground width is recommended.

Some of the NMOS memories with TTL logic compatible inputs do not actually meet the TTL logic level requirements in the input high state voltage (V_{IH}). There are N-Channel MOS memories with a V_{IH} minimum ranging from 2.4 V to 4.0 V. The MC3459 can directly interface with those N-Channel memories having a V_{IH} minimum of 3.0 V. The higher driver output levels can be accomplished by adding a pull-up resistor to V_{CC} or by increasing the V_{CC} voltage. There are some N-Channel MOS memories, such as the MCM7001, that have a supply requirement of 7.5 V. The high maximum supply voltage rating of the MC3459 can accommodate a 7.5 V V_{CC} supply without affecting its input TTL logic compatibility. Figure 4 gives the typical V_{OH} versus I_{OH} characteristics for both $V_{CC} = 5.0$ V and $V_{CC} = 7.5$ V. An expanded output characteristic curve of Figure 4 is illustrated in Figure 5.

The MC3459 can be used in a variety of applications including, high fan-out buffer (drives 50 standard TTL loads) and low impedance transmission line driver.

FIGURE 6 — TYPICAL APPLICATION
16 K X N Memory System Employing
MCM6605 4K RAMS



2N3563**NPN LOW LEVEL RF AMPLIFIER**

DIFFUSED SILICON PLANAR EPITAXIAL TRANSISTOR

The 2N3563 is an NPN silicon PLANAR epitaxial transistor designed for low-level RF applications. It features high power gain, low noise and low leakage in a new solid package designed to give maximum mechanical support to the transistor chip.

ABSOLUTE MAXIMUM RATINGS [Note 1]**Maximum Temperatures**

Operating Junction Temperature

Storage Temperature

Soldering Temperature (10 sec. time limit)

+125°C Maximum

-55°C to +125°C

+260°C Maximum

Maximum Power Dissipation

Total Dissipation at 25°C Case Temperature

at 65°C Case Temperature

at 25°C Ambient Temperature

(Note 2)

(Note 2)

(Note 2)

0.5 Watt

0.3 Watt

0.2 Watt

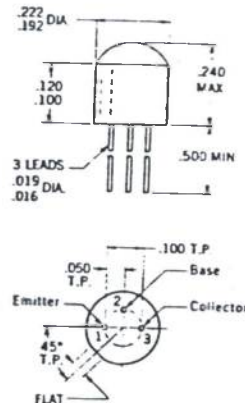
Maximum Voltages V_{CBO} Collector to Base Voltage V_{CEO} Collector to Emitter Voltage V_{EBO} Emitter to Base Voltage

(Note 3)

30 Volts

12 Volts

2.0 Volts

PHYSICAL DIMENSIONS
Epoxy package
TO-106

NOTES: All dimensions in inches.
All leads electrically isolated from case.
Package weight is 0.31 gram. Package
is electrically non-conductive material.

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

Symbol	Characteristics	Min.	Typ.	Max.	Units	Test Conditions
h_{FE}	DC Pulse Current Gain (Note 4)	20	50	200		$I_C = 8.0 \text{ mA}$ $V_{CE} = 10 \text{ V}$
$V_{CE(sat)}$	Collector Saturation Voltage		0.1		Volts	$I_C = 10 \text{ mA}$ $I_B = 1.0 \text{ mA}$
C_{obo}	Open Circuit Output Capacitance		1.3	1.7	pf	$I_E = 0$ $V_{CB} = 10 \text{ V}$
C_{cb}	Collector-base Transfer (Note 7)		0.8		pf	$I_E = 0$ $V_{CB} = 10 \text{ V}$
I_{CBO}	Collector Cutoff Current			50	nA	$I_E = 0$ $V_{CB} = 15 \text{ V}$
$I_{CBO(65^\circ C)}$	Collector Cutoff Current			5.0	μA	$I_E = 0$ $V_{CB} = 15 \text{ V}$
h_{fe}	High Frequency Current Gain ($f = 100 \text{ mc}$)	6.0	9.0			$I_C = 8.0 \text{ mA}$ $V_{CE} = 10 \text{ V}$
G_{pe}	Available Power Gain (neutralized) (Note 5) ($f = 200 \text{ mc}$)	14	17		db	$I_C = 8.0 \text{ mA}$ $V_{CE} = 10 \text{ V}$
NF	Noise Figure (Note 6)		4.0		db	$I_C = 1.0 \text{ mA}$ $V_{CE} = 6.0 \text{ V}$
$r_b' C_c$	Collector-Base Time Constant ($f = 79.8 \text{ mc}$)	8.0	15	25	psec	$I_C = 8.0 \text{ mA}$ $V_{CB} = 10 \text{ V}$
h_{fe}	Small Signal Current Gain ($f = 1.0 \text{ Kc}$)	20		250		$I_C = 8.0 \text{ mA}$ $V_{CE} = 10 \text{ V}$
BV_{CBO}	Collector to Base Breakdown Voltage	30			Volts	$I_E = 0$ $I_C = 100 \mu A$
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage (Notes 3 and 4)	12			Volts	$I_C = 3.0 \text{ mA}$ (pulsed) $I_B = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	2.0			Volts	$I_C = 0$ $I_E = 10 \mu A$

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313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910 379 6435

2N3567 • 2N3568

NPN GENERAL PURPOSE TYPES

DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTORS

The 2N3567 and 2N3568 are NPN silicon PLANAR* epitaxial transistors designed primarily for amplifier and switching applications over a wide range of voltage and current. These devices feature a useful beta range to 500 mA and low saturation voltage. High collector-to-emitter voltage allows operation to 60 volts for the 2N3568 and 40 volts for the 2N3567.

ABSOLUTE MAXIMUM RATINGS [Note 1]

Maximum Temperatures

Storage Temperature

-55°C to +125°C

Operating Junction Temperature

+125°C Maximum

Lead Temperature (Soldering, 10 sec. time limit)

+260°C Maximum

Maximum Power Dissipation

Total Dissipation at 25°C Case Temperature (Notes 2 & 3)

0.8 Watt

at 25°C Ambient Temperature (Notes 2 & 3)

0.3 Watt

Maximum Voltages

2N3567

2N3568

V_{CBO} Collector to Base Voltage

80 Volts

80 Volts

V_{CEO} Collector to Emitter Voltage (Note 4)

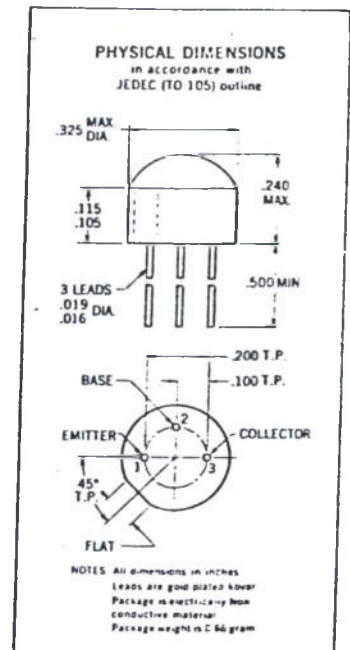
40 Volts

60 Volts

V_{EBO} Emitter to Base Voltage

5.0 Volts

5.0 Volts

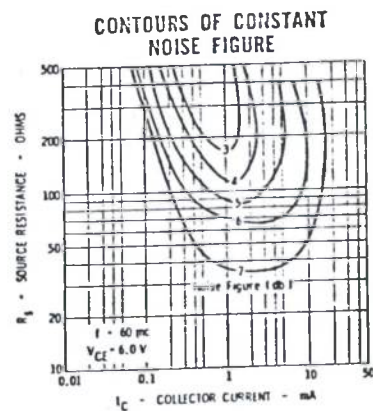
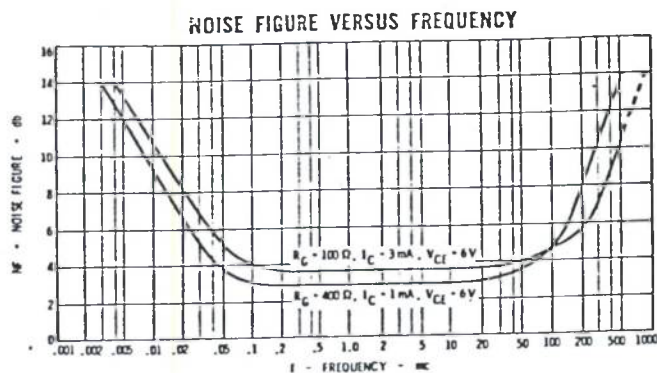
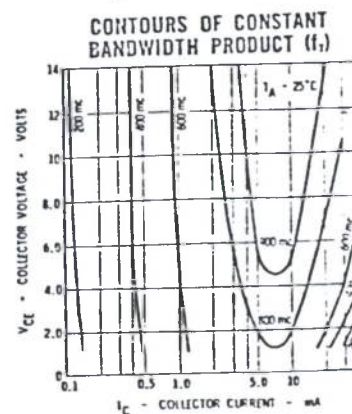
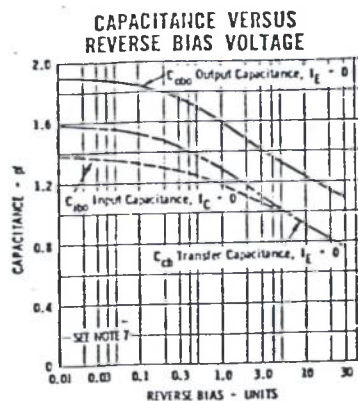
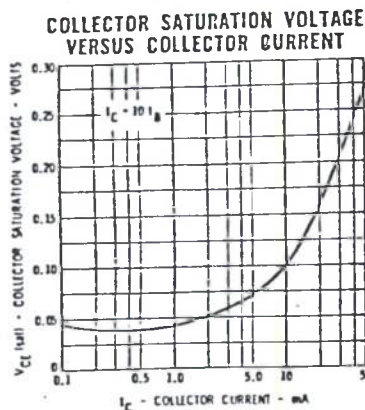
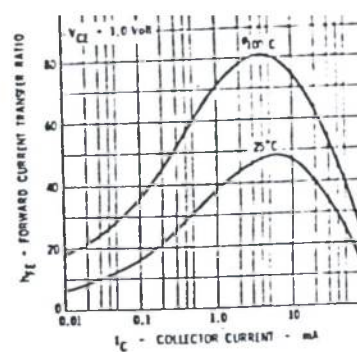
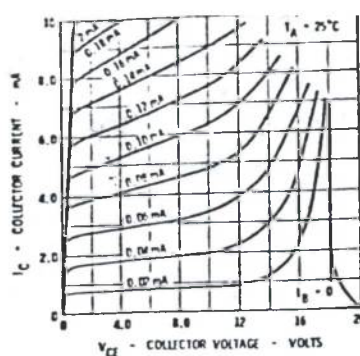
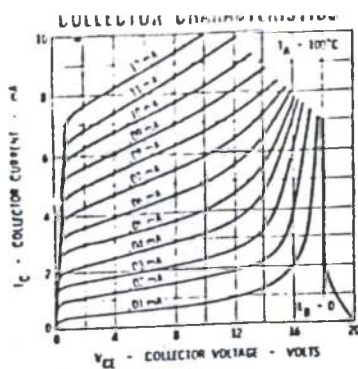


ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

Symbol	Characteristic	2N3567			2N3568			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
h_{FE}	DC Pulse Current Gain (Note 5)	40	80	120	40	80	120		$I_C = 150 \text{ mA}$ $V_{CE} = 1.0 \text{ V}$
h_{FE}	DC Pulse Current Gain (Note 5)	40			40				$I_C = 30 \text{ mA}$ $V_{CE} = 1.0 \text{ V}$
$V_{CE(sat)}$	Collector Saturation Voltage (pulsed, see note 5)	0.15	0.25		0.15	0.25		Volts	$I_C = 150 \text{ mA}$ $I_B = 15 \text{ mA}$
$V_{BE(sat)}$	Base Saturation Voltage (pulsed, see note 5)	0.9	1.1		0.9	1.1		Volts	$I_C = 150 \text{ mA}$ $I_B = 15 \text{ mA}$
h_{fe}	High Frequency Current Gain ($f = 20 \text{ MHz}$)	3.0			3.0				$I_C = 50 \text{ mA}$ $V_{CE} = 10 \text{ V}$
C_{obo}	Open Circuit Output Capacitance	13	20		13	20		pF	$I_E = 0$ $V_{CB} = 10 \text{ V}$
C_{ibo}	Open Circuit Input Capacitance	63	80		63	80		pF	$I_C = 0$ $V_{EB} = 0.5 \text{ V}$
I_{CBO}	Collector Cutoff Current		50			50		nA	$I_E = 0$ $V_{CB} = 40 \text{ V}$
$I_{CBO(75^\circ C)}$	Collector Cutoff Current		5.0			5.0		μA	$I_E = 0$ $V_{CB} = 40 \text{ V}$
I_{EBO}	Emitter Cutoff Current		25			25		nA	$I_C = 0$ $V_{EB} = 4.0 \text{ V}$
BV_{CBO}	Collector to Base Breakdown Voltage	80		80				Volts	$I_E = 0$ $I_C = 100 \mu A$
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage (Notes 4 and 5)	40		60				Volts	$I_C = 30 \text{ mA}$ (pulsed) $I_B = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	5.0		5.0				Volts	$I_C = 0$ $I_E = 10 \mu A$

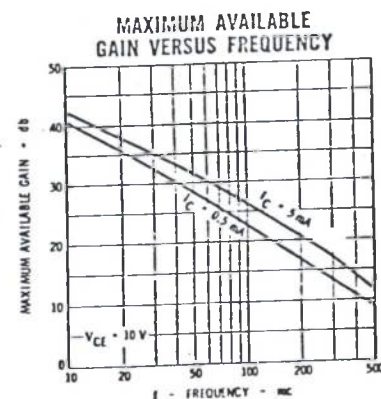
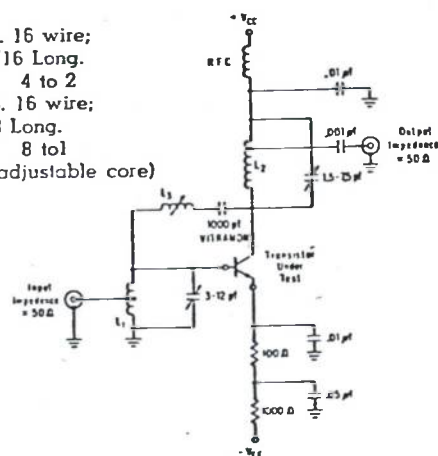
* Planar is a patented Fairchild process.

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NEUTRALIZED 200 MC POWER GAIN AMPLIFIER TEST CIRCUIT

- L₁—3.5 Turns No. 16 wire;
5/16 Dia; 7/16 Long.
Turns Ratio 4 to 2
L₂—8.0 Turns No. 16 wire;
1/8 Dia; 7/8 Long.
Turns Ratio 8 to 1
L₃—0.4-0.65 μ h (adjustable core)



- Single family characteristics on Transistor Curve 1

NOTES:

- NOTES:
- (1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
 - (2) These ratings give a maximum junction temperature of 125°C and junction-to-case thermal resistance of 200°C/Watt (derating factor of $5.0\text{mW}/^{\circ}\text{C}$); junction-to-ambient thermal resistance of 500°C/Watt (derating factor of $2.0\text{mW}/^{\circ}\text{C}$).
 - (3) Rating refers to a high-current point where collector-to-emitter voltage is lowest.
 - (4) Pulse Conditions: length = $300\text{ }\mu\text{sec}$; duty cycle $\leq 1\%$.
 - (5) Forward gain (db) + reverse gain (db) $< (-20\text{ db})$. See test circuit.
 - (6) $f = 60\text{ mc}$; $R_S = 400\text{ }\Omega$.
 - (7) C_{cb} is measured using a three-terminal measurement technique with case and emitter guarded. C_{cb} is equivalent to C_{re} .

MPS3640 (SILICON)



PNP silicon annular transistors designed for general-purpose low-level switching applications.

CASE 29(1)
(TO-92)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	12	Vdc
Collector-Base Voltage	V_{CB}	12	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current - Continuous	I_C	80	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	310 2.81	mW mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +135	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage* ($I_C = 10 \text{ mAdc}$, $I_B = 0$)	$BV_{CEO(sus)}$ *	12	-	Vdc
Collector-Emitter Breakdown Voltage ($I_C = 100 \mu\text{Adc}$, $V_{BE} = 0$)	BV_{CES}	12	-	Vdc
Collector-Base Breakdown Voltage ($I_C = 100 \mu\text{Adc}$, $I_E = 0$)	BV_{CBO}	12	-	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100 \mu\text{Adc}$, $I_C = 0$)	BV_{EBO}	4.0	-	Vdc
Collector Cutoff Current ($V_{CE} = 6.0 \text{ Vdc}$, $V_{BE} = 0$) ($V_{CE} = 6.0 \text{ Vdc}$, $V_{BE} = 0$, $T_A = 65^\circ\text{C}$)	I_{CES}	- -	0.01 1.0	μAdc

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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ON CHARACTERISTICS

DC Current Gain* ($I_C = 10\text{ mA}$, $V_{CE} = 0.3\text{ Vdc}$) ($I_C = 50\text{ mA}$, $V_{CE} = 1.0\text{ Vdc}$)	h_{FE}^*	30 20	120 -	-
Collector-Emitter Saturation Voltage ($I_C = 10\text{ mA}$, $I_B = 1.0\text{ mA}$) ($I_C = 50\text{ mA}$, $I_B = 5.0\text{ mA}$)* ($I_C = 10\text{ mA}$, $I_B = 1.0\text{ mA}$, $T_A = 65^\circ\text{C}$)	$V_{CE(sat)}$	- - -	0.2 0.6 0.25	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ mA}$, $I_B = 0.5\text{ mA}$) ($I_C = 10\text{ mA}$, $I_B = 1.0\text{ mA}$) ($I_C = 50\text{ mA}$, $I_B = 5.0\text{ mA}$)*	$V_{BE(sat)}$	0.75 0.8 -	0.95 1.0 1.5	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product ($I_C = 10\text{ mA}$, $V_{CE} = 5.0\text{ Vdc}$, $f = 100\text{ MHz}$)	f_T	500	-	MHz
Output Capacitance ($V_{CB} = 5.0\text{ Vdc}$, $I_E = 0$, $f = 140\text{ kHz}$)	C_{ob}	-	3.5	pF
Input Capacitance ($V_{BE} = 0.5\text{ Vdc}$, $I_C = 0$, $f = 140\text{ kHz}$)	C_{ib}	-	3.5	pF

SWITCHING CHARACTERISTICS

Turn-On Time ($V_{BE(off)} = 1.9\text{ Vdc}$, $V_{CC} = 6.0\text{ Vdc}$, $I_C = 50\text{ mA}$, $I_{B1} = 5.0\text{ mA}$)(See Figure 1) ($I_C = 10\text{ mA}$, $V_{CC} = 1.5\text{ Vdc}$, $I_{B1} = 0.5\text{ mA}$)(See Figure 2)	t_{on}	- -	25 60	ns
Delay Time ($V_{CC} = 6.0\text{ Vdc}$, $V_{BE(off)} = 1.9\text{ Vdc}$,	t_d	-	10	ns
Rise Time $I_C = 50\text{ mA}$, $I_{B1} = 5.0\text{ mA}$)(See Figure 1)	t_r	-	30	ns
Turn-Off Time ($V_{BE(off)} = 1.9\text{ Vdc}$, $V_{CC} = 6.0\text{ Vdc}$, $I_C = 50\text{ mA}$, $I_{B1} = I_{B2} = 5.0\text{ mA}$)(See Figure 1) ($I_C = 10\text{ mA}$, $V_{CC} = 1.5\text{ Vdc}$, $I_{B1} = I_{B2} = 0.5\text{ mA}$)(See Figure 2)	t_{off}	- -	35 75	ns
Storage Time ($V_{CC} = 6.0\text{ Vdc}$, $I_C = 50\text{ mA}$,	t_s	-	20	ns
Fall Time $I_{B1} = I_{B2} = 5.0\text{ mA}$)(See Figure 1)	t_f	-	12	ns

*Pulse Test: Pulse Width = 300 μs , Duty Cycle = 1.0%.

FIGURE 1 - SWITCHING TIME TEST CIRCUIT

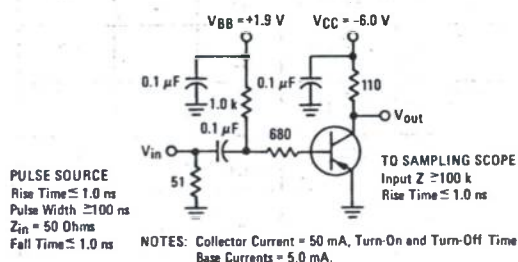
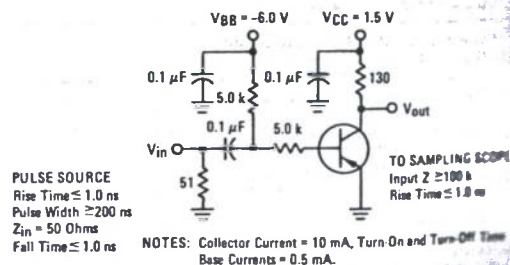


FIGURE 2 - SWITCHING TIME TEST CIRCUIT



2N3644 • 2N3645

PNP HIGH CURRENT SWITCHES

DIFFUSED SILICON PLANAR EPITAXIAL TRANSISTORS

These PNP silicon PLANAR epitaxial transistors are designed for digital and analog applications at current levels up to 500 milliamperes. Their high beta, high I_T at high current and high V_{CEO} , make them ideal for use as line drivers and memory applications.

ABSOLUTE MAXIMUM RATINGS [Note 1]

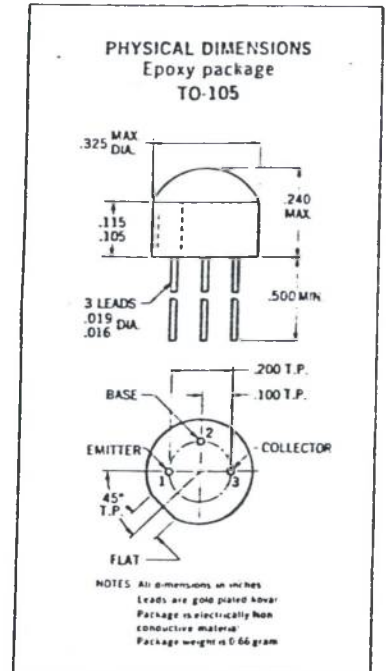
Maximum Temperatures

Storage Temperature	-55°C to +125°C
Operating Junction Temperature	+125°C Maximum
Lead Temperature (soldering, 10 sec time limit)	+260°C Maximum

Maximum Power Dissipation	2N3645	2N3644
Total Dissipation at 25°C Case Temperature (Notes 2 & 3)	0.7 Watt	0.7 Watt
at 25°C Free Air Temperature (Notes 2 & 3)	0.3 Watt	0.3 Watt

Maximum Voltages

V_{CBO}	Collector to base Voltage	-60 Volts	-45 Volts
V_{CEO}	Collector to Emitter Voltage (Note 4)	-60 Volts	-45 Volts
V_{EBO}	Emitter to Base Voltage	-5.0 Volts	-5.0 Volts



ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
h_{FE}	DC Current Gain	40	170			$I_C = 100 \mu A$ $V_{CE} = -10 V$
h_{FE}	DC Current Gain	80	200			$I_C = 1.0 mA$ $V_{CE} = -10 V$
h_{FE}	DC Pulse Current Gain (Note 5)	100	270			$I_C = 10 mA$ $V_{CE} = -10 V$
h_{FE}	DC Pulse Current Gain (Note 5)	115	160	300		$I_C = 50 mA$ $V_{CE} = -1.0 V$
h_{FE}	DC Pulse Current Gain (Note 5)	100	150	300		$I_C = 150 mA$ $V_{CE} = -10 V$
h_{FE}	DC Pulse Current Gain (Note 5)	20	50			$I_C = 300 mA$ $V_{CE} = -2.0 V$
h_{fe}	High Frequency Current Gain ($f = 100 Mc$)	2.0	2.50			$I_C = 20 mA$ $V_{CE} = -20 V$
C_{obo}	Common Base Output Capacitance		4.5	8.0	pf.	$I_E = 0$ $V_{CB} = -10 V$
C_{ibo}	Common Base Input Capacitance		15	25	pf	$I_C = 0$ $V_{EB} = -0.5 V$

Additional Electrical Characteristics on page 2

NOTES:

- These ratings are limiting values above which the serviceability of any individual semiconductor may be impaired.
- These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.
- These ratings give a maximum junction temperature of 125°C and junction-to-case thermal resistance of 143°C/Watt (derating factor of 7.0 mW/°C); junction-to-ambient thermal resistance of 333°C/Watt (derating factor of 3.0 mW/°C).
- Rating refers to a high-current point where collector-to-emitter voltage is lowest.
- Pulse Conditions: length = 300 μsec ; duty cycle = 1%.
- See switching circuit for exact values of I_C , I_{B1} , and I_{B2} .

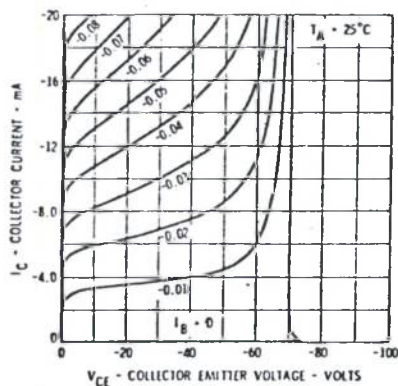
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ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

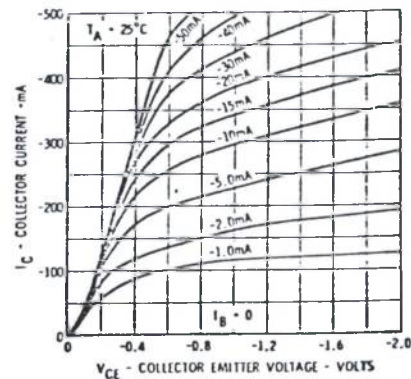
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
$V_{CE(sat)}$	Collector Saturation Voltage (Pulsed, see Note 5)	-0.08	-0.25		Volts	$I_C = 50 \text{ mA}$ $I_B = 2.5 \text{ mA}$
$V_{CE(sat)}$	Collector Saturation Voltage (Pulsed, see Note 5)	-0.18	-0.4		Volts	$I_C = 150 \text{ mA}$ $I_B = 15 \text{ mA}$
$V_{CE(sat)}$	Collector Saturation Voltage (Pulsed, see Note 5)	-0.5	-1.0		Volts	$I_C = 300 \text{ mA}$ $I_B = 30 \text{ mA}$
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage (Notes 4 & 5)	2N3645 -60 2N3644 -45			Volts Volts	$I_C = 10 \text{ mA}$ $I_B = 0$ (pulsed)
$V_{BE(sat)}$	Base Saturation Voltage (Pulsed, see Note 5)	-0.9	-1.0		Volts	$I_C = 50 \text{ mA}$ $I_B = 2.5 \text{ mA}$
$V_{BE(sat)}$	Base Saturation Voltage (Pulsed, see Note 5)	-1.0	-1.3		Volts	$I_C = 150 \text{ mA}$ $I_B = 15 \text{ mA}$
$V_{BE(sat)}$	Base Saturation Voltage (Pulsed, see Note 5)	-0.8	-2.0		Volts	$I_C = 300 \text{ mA}$ $I_B = 30 \text{ mA}$
BV_{EBO}	Emitter to Base Breakdown Voltage	-5.0			Volts	$I_C = 0$ $I_E = 10 \text{ } \mu\text{A}$
BV_{CBO}	Collector to Base Breakdown Voltage	2N3645 -60 2N3644 -45			Volts Volts	$I_C = 100 \text{ } \mu\text{A}$ $I_E = 0$
t_{on}	Turn On Time (Note 6)		30	40	nsec	$I_C \approx 300 \text{ mA}$ $I_{B1} \approx 30 \text{ mA}$
t_{off}	Turn Off Time (Note 6)		65	100	nsec	$I_C \approx 300 \text{ mA}$, $I_{B1} \approx 30 \text{ mA}$, $I_{B2} \approx -30 \text{ mA}$
I_{CES}	Collector Reverse Current	2N3645 2N3644		35	nA	$V_{CE} = -50 \text{ V}$ $V_{BE} = 0$
				35	nA	$V_{CE} = -30 \text{ V}$ $V_{BE} = 0$
I_{CES}	Collector Reverse Current (+65°C)	2N3645 2N3644		2.0	μA	$V_{CE} = -50 \text{ V}$ $V_{BE} = 0$
				2.0	μA	$V_{CE} = -30 \text{ V}$ $V_{BE} = 0$

TYPICAL ELECTRICAL CHARACTERISTICS

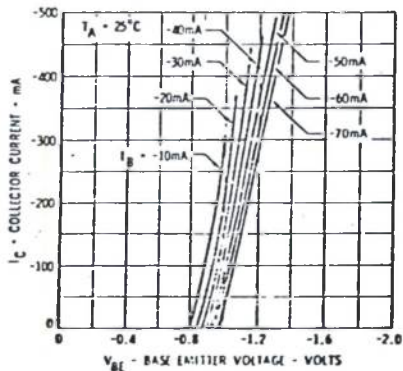
COLLECTOR CHARACTERISTICS*



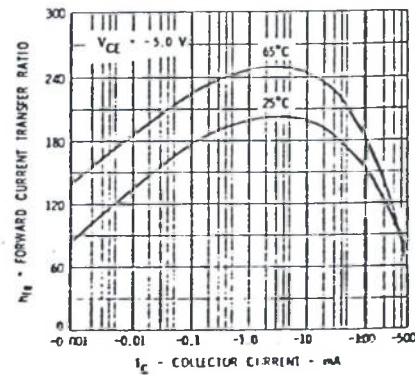
COLLECTOR CHARACTERISTICS*



BASE CHARACTERISTICS*



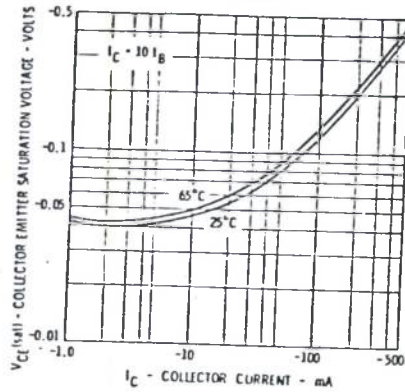
DC PULSED CURRENT GAIN
VERSUS COLLECTOR CURRENT



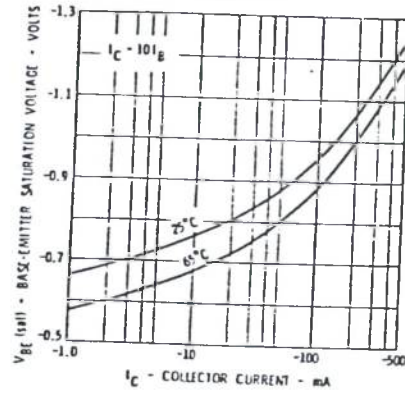
* Single family characteristics on Transistor Curve Tracer.

TYPICAL ELECTRICAL CHARACTERISTICS

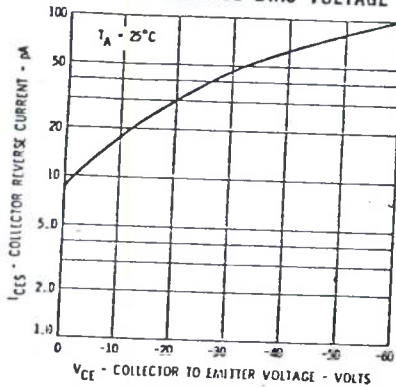
PULSED COLLECTOR SATURATION
 VOLTAGE VERSUS COLLECTOR
 CURRENT



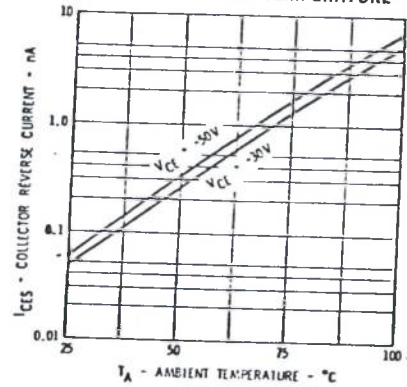
PULSED BASE SATURATION
 VOLTAGE VERSUS COLLECTOR
 CURRENT



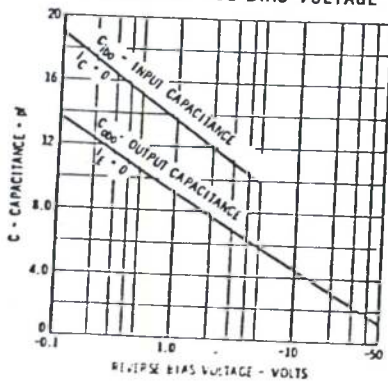
COLLECTOR REVERSE CURRENT
 VERSUS REVERSE BIAS VOLTAGE



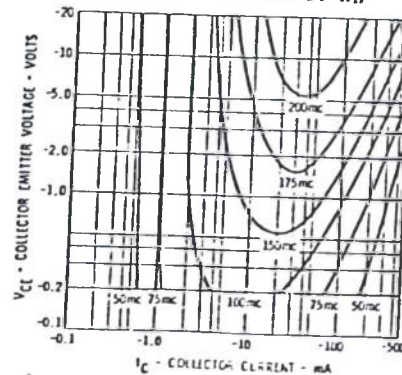
COLLECTOR REVERSE CURRENT
 VERSUS AMBIENT TEMPERATURE



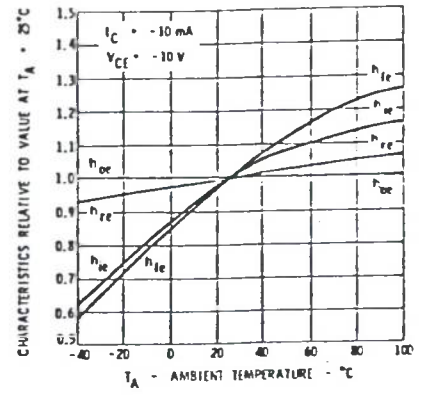
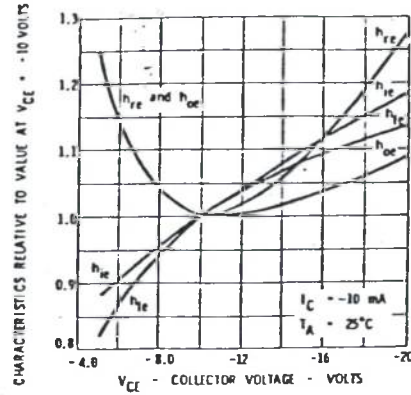
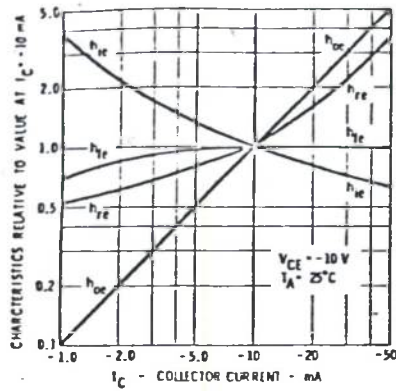
INPUT AND OUTPUT CAPACITANCES
 VERSUS REVERSE BIAS VOLTAGE



CONTOURS OF CONSTANT GAIN
 BANDWIDTH PRODUCT (f_t)



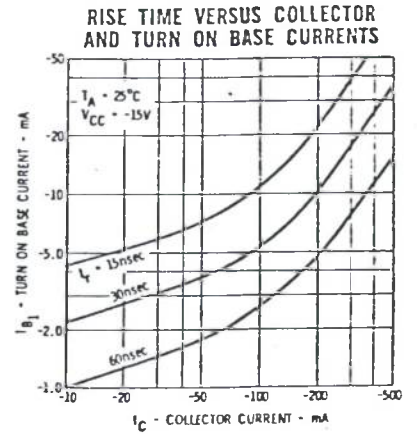
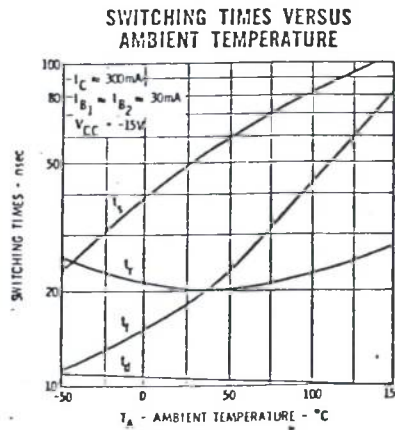
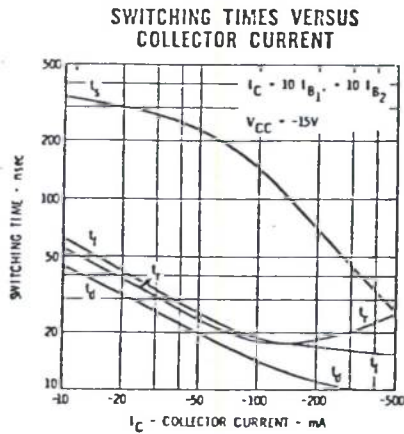
SMALL SIGNAL CHARACTERISTICS



h PARAMETERS (f = 1 kc)

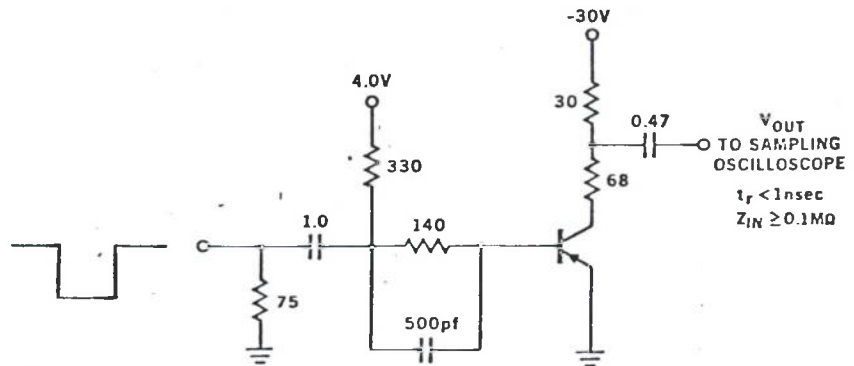
Symbol		Min.	Typ.	Max.	Units	Test Conditions
h_{ie}	Input Resistance		480	2000	ohms	$I_C = 10 \text{ mA}$ $V_{CE} = -10 \text{ V}$
h_{oe}	Output Conductance		80	1200	μmhos	$I_C = 10 \text{ mA}$ $V_{CE} = -10 \text{ V}$
h_{re}	Voltage Feedback Ratio		162	1500	$\times 10^{-6}$	$I_C = 10 \text{ mA}$ $V_{CE} = -10 \text{ V}$
h_{fe}	Small Signal Current Gain	100				$I_C = 10 \text{ mA}$ $V_{CE} = -10 \text{ V}$

TYPICAL ELECTRICAL CHARACTERISTICS



T_{ON} AND T_{OFF} TEST CIRCUIT

PULSE GENERATOR
 $V_{IN} = -9 \text{ V}$
 $t_r, t_f \leq 6 \text{ nsec}$
 $P.W. = 0.5 \mu\text{sec}$
 $Z_{IN} = 50 \Omega$



Fairchild cannot assume responsibility for use of any circuitry described. No circuit patent licenses are implied.

2N3903 (SILICON)

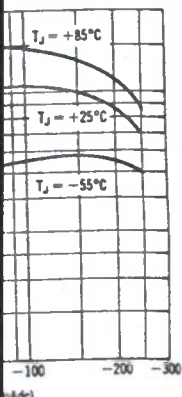
2N3904



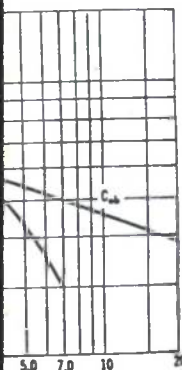
CASE 29(1)
(TO-92)

NPN silicon annular transistors, designed for general-purpose switching and amplifier applications, features one-piece, injection-molded plastic package for high reliability. The 2N3903 and 2N3904 are complementary with PNP types 2N3905 and 2N3906, respectively.

CHARACTERISTICS



REVERSE VOLTAGE



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current	I_C	200	mA dc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ $T_A = 60^\circ\text{C}$ Derate above 25°C	P_D	310 210 2.81	mW mW mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +135	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.357	$^\circ\text{C}/\text{mW}$

2N3903, 2N3904 (continued)

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)*

Characteristic	Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Breakdown Voltage ($I_C = 10\text{ }\mu\text{A}$, $I_E = 0$)		BV_{CBO}	60	-	Vdc
Collector-Emitter Breakdown Voltage* ($I_C = 1.0\text{ mA}$, $I_B = 0$)		BV_{CEO}^*	40	-	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10\text{ }\mu\text{A}$, $I_C = 0$)		BV_{EBO}	6.0	-	Vdc
Collector Cutoff Current ($V_{CE} = 30\text{ Vdc}$, $V_{EB}(\text{off}) = 3.0\text{ Vdc}$)		I_{CEX}	-	50	nAdc
Base Cutoff Current ($V_{CE} = 30\text{ Vdc}$, $V_{EB}(\text{off}) = 3.0\text{ Vdc}$)		I_{BL}	-	50	nAdc

ON CHARACTERISTICS

DC Current Gain* ($I_C = 0.1\text{ mA}$, $V_{CE} = 1.0\text{ Vdc}$)	2N3903 2N3904	15	h_{FE}^*	20 40	-	-
($I_C = 1.0\text{ mA}$, $V_{CE} = 1.0\text{ Vdc}$)	2N3903 2N3904			35 70	-	-
($I_C = 10\text{ mA}$, $V_{CE} = 1.0\text{ Vdc}$)	2N3903 2N3904			50 100	150 300	-
($I_C = 50\text{ mA}$, $V_{CE} = 1.0\text{ Vdc}$)	2N3903 2N3904			30 60	-	-
($I_C = 100\text{ mA}$, $V_{CE} = 1.0\text{ Vdc}$)	2N3903 2N3904			15 30	-	-
Collector-Emitter Saturation Voltage* ($I_C = 10\text{ mA}$, $I_B = 1.0\text{ mA}$) ($I_C = 50\text{ mA}$, $I_B = 5.0\text{ mA}$)		16, 17	$V_{CE}(\text{sat})^*$	- -	0.2 0.3	Vdc
Base-Emitter Saturation Voltage* ($I_C = 10\text{ mA}$, $I_B = 1.0\text{ mA}$) ($I_C = 50\text{ mA}$, $I_B = 5.0\text{ mA}$)		17	$V_{BE}(\text{sat})^*$	0.65 -	0.85 0.95	Vdc

SMALL-SIGNAL CHARACTERISTICS

Current-Gain-Bandwidth Product ($I_C = 10\text{ mA}$, $V_{CE} = 20\text{ Vdc}$, $f = 100\text{ MHz}$)	2N3903 2N3904		f_T	250 300	-	MHz
Output Capacitance ($V_{CB} = 5.0\text{ Vdc}$, $I_E = 0$, $f = 100\text{ kHz}$)		3	C_{ob}	-	4.0	pF
Input Capacitance ($V_{BE} = 0.5\text{ Vdc}$, $I_C = 0$, $f = 100\text{ kHz}$)		3	C_{ib}	-	8.0	pF
Input Impedance ($I_C = 1.0\text{ mA}$, $V_{CE} = 10\text{ Vdc}$, $f = 1.0\text{ kHz}$)	2N3903 2N3904	13	h_{ie}	0.5 1.0	8.0 10	k ohms
Voltage Feedback Ratio ($I_C = 1.0\text{ mA}$, $V_{CE} = 10\text{ Vdc}$, $f = 1.0\text{ kHz}$)	2N3903 2N3904	14	h_{re}	0.1 0.5	5.0 8.0	$\times 10^{-4}$
Small-Signal Current Gain ($I_C = 1.0\text{ mA}$, $V_{CE} = 10\text{ Vdc}$, $f = 1.0\text{ kHz}$)	2N3903 2N3904	11	h_{fe}	50 100	200 400	-
Output Admittance ($I_C = 1.0\text{ mA}$, $V_{CE} = 10\text{ Vdc}$, $f = 1.0\text{ kHz}$)		12	h_{oe}	1.0	40	μmhos
Noise Figure ($I_C = 100\text{ }\mu\text{A}$, $V_{CE} = 5.0\text{ Vdc}$, $R_S = 1.0\text{ k ohms}$, $f = 10\text{ Hz}$ to 15.7 kHz)	2N3903 2N3904	9, 10	NF	- -	6.0 5.0	dB

SWITCHING CHARACTERISTICS

Delay Time	($V_{CC} = 3.0\text{ Vdc}$, $V_{BE}(\text{off}) = 0.5\text{ Vdc}$, $I_C = 10\text{ mA}$, $I_{B1} = 1.0\text{ mA}$)	1, 5	t_d	-	35	ns
Rise Time		1, 5, 6	t_r	-	35	ns
Storage Time	($V_{CC} = 3.0\text{ Vdc}$, $I_C = 10\text{ mA}$, $I_{B1} = I_{B2} = 1.0\text{ mA}$)	2, 7	t_s	-	175 200	ns
Fall Time		2, 8	t_f	-	50	ns

* Pulse Test: Pulse Width = $300\text{ }\mu\text{s}$, Duty Cycle = 2.0%.

FIGURE 1 — DELAY AND RISE TIME EQUIVALENT TEST CIRCUIT

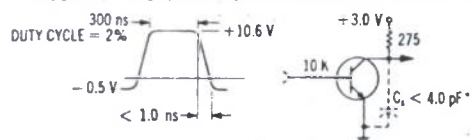
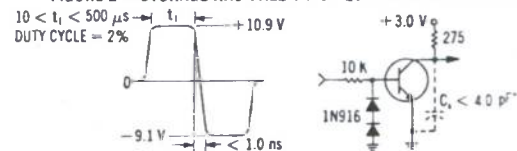


FIGURE 2 — STORAGE AND FALL TIME EQUIVALENT TEST CIRCUIT



*Total shunt capacitance of test jig and connectors

2N3905 (SILICON)

2N3906



CASE 29(1)
(TO-92)

PNP silicon annular transistors, designed for general purpose switching and amplifier applications, features one-piece, injection-molded plastic package for high reliability. The 2N3905 and 2N3906 are complementary with NPN types 2N3903 and 2N3904, respectively.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current	I_C	200	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ $T_A = 60^\circ\text{C}$ Derate above 25°C	P_D	310	mW
		210	mW
		2.81	mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +135	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.357	$^\circ\text{C}/\text{mW}$

2N3905, 2N3906 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Breakdown Voltage (I _C = 10 μAdc, I _E = 0)		BV _{CBO}	40	-	Vdc
Collector-Emitter Breakdown Voltage* (I _C = 1.0 mAdc, I _B = 0)		BV _{CEO} *	40	-	Vdc
Emitter-Base Breakdown Voltage (I _E = 10 μAdc, I _C = 0)		BV _{EBO}	5.0	-	Vdc
Collector Cutoff Current (V _{CE} = 30 Vdc, V _{BE(off)} = 3.0 Vdc)		I _{CEX}	-	50	nAdc
Base Cutoff Current (V _{CE} = 30 Vdc, V _{BE(off)} = 3.0 Vdc)		I _{BL}	-	50	nAdc

ON CHARACTERISTICS

DC Current Gain* (I _C = 0.1 mAdc, V _{CE} = 1.0 Vdc)	2N3905	15	h _{FE} *	30	-	-
	2N3906			60	-	-
	2N3905			40	-	-
	2N3906			80	-	-
	2N3905			50	150	-
	2N3906			100	300	-
Collector-Emitter Saturation Voltage* (I _C = 10 mAdc, I _B = 1.0 mAdc)	2N3905	16, 17	V _{CE(sat)} *	-	0.25	Vdc
	2N3906			-	0.4	Vdc
	2N3905			-	0.85	Vdc
Base-Emitter Saturation Voltage* (I _C = 10 mAdc, I _B = 1.0 mAdc)	2N3905	17	V _{BE(sat)} *	0.65	0.85	Vdc
	2N3906			-	0.95	Vdc
	2N3905			-	0.95	Vdc

SMALL-SIGNAL CHARACTERISTICS

Current-Gain-Bandwidth Product (I _C = 10 mAdc, V _{CE} = 20 Vdc, f = 100 MHz)	2N3905 2N3906		f _T	200 250	-	MHz
Output Capacitance (V _{CB} = 5.0 Vdc, I _E = 0, f = 100 kHz)		3	C _{ob}	-	4.5	pF
Input Capacitance (V _{BE} = 0.5 Vdc, I _C = 0, f = 100 kHz)		3	C _{ib}	-	10	pF
Input Impedance (I _C = 1.0 mAdc, V _{CE} = 10 Vdc, f = 1.0 kHz)	2N3905 2N3906	13	h _{ie}	0.5 2.0	8.0 12	k ohms
Voltage Feedback Ratio (I _C = 1.0 mAdc, V _{CE} = 10 Vdc, f = 1.0 kHz)	2N3905 2N3906	14	h _{re}	0.1 1.0	5.0 10	X 10 ⁻⁴
Small-Signal Current Gain (I _C = 1.0 mAdc, V _{CE} = 10 Vdc, f = 1.0 kHz)	2N3905 2N3906	11	h _{fe}	50 100	200 400	-
Output Admittance (I _C = 1.0 mAdc, V _{CE} = 10 Vdc, f = 1.0 kHz)	2N3905 2N3906	12	h _{oe}	1.0 3.0	40 60	μmhos
Noise Figure (I _C = 100 μAdc, V _{CE} = 5.0 Vdc, R _S = 1.0 k ohm, f = 10 Hz to 15.7 kHz)	2N3905 2N3906	9, 10	NF	-	5.0 4.0	dB

SWITCHING CHARACTERISTICS

Delay Time (V _{CC} = 3.0 Vdc, V _{BE(off)} = 0.5 Vdc, I _C = 10 mAdc, I _{B1} = 1.0 mAdc)	2N3905 2N3906	1, 5	t _d	-	35	ns
Rise Time (V _{CC} = 3.0 Vdc, I _C = 10 mAdc, I _{B1} = 1.0 mAdc)	2N3905 2N3906	1, 5, 6	t _r	-	35	ns
Storage Time (V _{CC} = 3.0 Vdc, I _C = 10 mAdc, I _{B1} = I _{B2} = 1.0 mAdc)	2N3905 2N3906	2, 7	t _s	-	200 225	ns
Fall Time (V _{CC} = 3.0 Vdc, I _C = 10 mAdc, I _{B1} = I _{B2} = 1.0 mAdc)	2N3905 2N3906	2, 8	t _f	-	60 75	ns

* Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

FIGURE 1 — DELAY AND RISE TIME EQUIVALENT TEST CIRCUIT

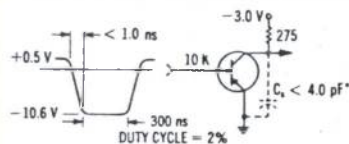
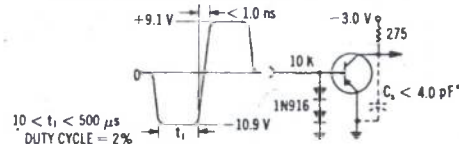


FIGURE 2 — STORAGE AND FALL TIME EQUIVALENT TEST CIRCUIT

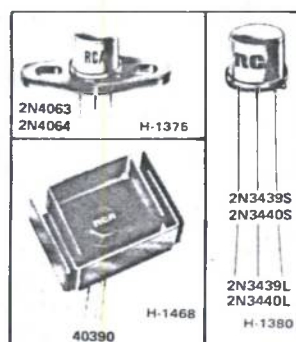


*Total shunt capacitance of test jig and connectors

RCA
Solid State
Division

Power Transistors

2N4063 2N4064
2N3439 2N3440 40390



High-Voltage Silicon N-P-N Transistors

For High-Speed Switching and Linear-Amplifier Applications

Features

- High voltage ratings:
 $V_{CBO} = 450$ V max. (2N3439, 2N4063)
 $= 300$ V max. (2N3440, 2N4064)
 $V_{CEO(sus)} = 350$ V max. (2N3439, 2N4063)
 $= 250$ V max. (2N3440, 2N4064)
- Maximum-area-of-operation curves
- Low saturation voltages

These devices are available with either 1½-inch leads (TO-5 package) or ½-inch leads (TO-39 package). The longer-lead versions are specified by suffix "L" after the type number; the shorter-lead versions are specified by suffix "S" after the type number.

RCA-2N3439*, 2N3440**, 2N4063, 2N4064, and 40390 are epitaxial-base silicon n-p-n transistors with high breakdown voltages, high-frequency response, and fast switching speeds. These transistors are intended for industrial, commercial, and military equipment. Typical applications include high-voltage differential and operational amplifiers, high-voltage inverters, and high-voltage, low-current switching and series regulators.

The 2N3439 and the 2N3440 differ primarily in their voltage ratings; the 2N4063 and 2N4064 have the same voltage ratings as the 2N3439 and 2N3440 respectively, but employ a flange package. Type 40390 is a 2N3440 with a factory-attached heat radiator; it is intended for printed-circuit-board applications.

* Formerly RCA Dev. No. TA2458.

** Formerly RCA Dev. No. TA2470.

Absolute-Maximum Values:

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	450	300	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE	$V_{CEO(sus)}$	350	250	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	7	7	V
COLLECTOR CURRENT	I_C	1	1	A
BASE CURRENT	I_B	0.5	0.5	A
TRANSISTOR DISSIPATION	P_T	10	10(2N3440) 10(2N4064) 3.5(40390) 1(2N3439) See Fig. 2. See Fig. 9.	W
At case temperatures up to 25°C				
At free-air temperatures up to 25°C				
At free-air temperatures up to 50°C				
At free-air temperatures above 25°C or 50°C				
For pulse operation				
TEMPERATURE RANGE:				
Storage & Operating (Junction)				-65 to 200 °C
LEAD TEMPERATURE (During soldering):				
At distance $\geq 1/32$ in. from seating plane for 10 s max.				255 °C

ELECTRICAL CHARACTERISTICS

Characteristic

Collector-Cutoff Current

Emitter-Cutoff Current

DC Forward-Current Transfer

Collector-to-Emitter Sustaining Voltage:
(See Figs. 3 & 4)
With base open

Base-to-Emitter Saturation Voltage

Collector-to-Emitter Saturation Voltage

Small-Signal, Forward-Current Transfer Ratio (at 5 MHz)

Output Capacitance (at 1 MHz)

Second-Breakdown Collector Current:
With base forward biased

Thermal Resistance:
Junction-to-Case

CAUTION: The sustaining voltage should be measured by means of a

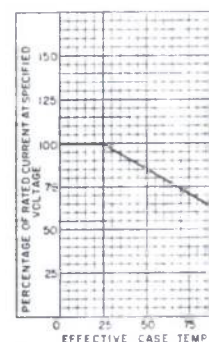


Fig. 1 - Current at

Transistors
2N4063
2N4064
40390

3439
3440

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C) = 25°C

Characteristic	Symbol	TEST CONDITIONS							LIMITS				Units
		DC Collector Volts		DC Emitter or Base Volts		DC Current (milliamperes)			Types 2N3439 2N4063		Types 2N3440 2N4064 40390		
		V _{CB}	V _{CE}	V _{EB}	V _{BE}	I _C	I _E	I _B	Min.	Max.	Min.	Max.	
Collector-Cutoff Current	I _{CEO}		300 200		•			0 0	- -	20 -	- -	- 50	μA μA
	I _{CEV}		450 300		-1.5 -1.5				- -	500 -	- -	- 500	μA μA
Emitter-Cutoff Current	I _{EBO}			6		0			-	20	-	20	μA
DC Forward-Current Transfer Ratio	h _{FE}		10 10			20 2			40 30	160 -	40 -	160 -	
Collector-to-Emitter Sustaining Voltage: (See Figs. 3 & 4.) With base open	V _{CEO(sus)}					50		0	350 ^a	-	250 ^a	-	V
Base-to-Emitter Saturation Voltage	V _{BE(sat)}					50		4	-	1.3	-	1.3	V
Collector-to-Emitter Saturation Voltage	V _{CE(sat)}					50		4	-	0.5	-	0.5	V
Small-Signal, Forward-Current Transfer Ratio (at 5 MHz)	h _{fe}		10			10			3	-	3	-	
Output Capacitance (at 1 MHz)	C _{ob}	10					0		-	10	-	10	pF
Second-Breakdown Collector Current: With base forward biased	I _{S/b}		200						50	-	50	-	mA
Thermal Resistance: Junction-to-Case	θ _{J-C}								-	17.5	-	17.5	°C/W

^aCAUTION: The sustaining voltage $V_{CE(sus)}$ MUST NOT be measured on a curve tracer. The sustaining voltage should be measured by means of the test circuit shown in Fig. 3.

These devices are available with either 1½-inch leads (TO-5 package) or ½-inch leads (TO-39 package). The longer-lead versions are specified by suffix "L" after the type number; the shorter-lead versions are specified by suffix "S" after the type number.

2N3440 differ primarily in their voltage ratings. 2N4064 have the same voltage ratings as 2N3440 respectively, but employ a flange for printed-circuit-board applications.

TA2458.
TA2470.

2N3439 2N3440
2N4063 2N4064
40390

450 300 V
350 250 V
7 V
1 A
0.5 0.5 A

10 10(2N3440) W
10 10(2N4064) W
3.5 3.5(40390) W
1(2N3439) 1(2N3440) W
See Fig. 2.
See Fig. 9.

-65 to 200 → °C

255 → °C

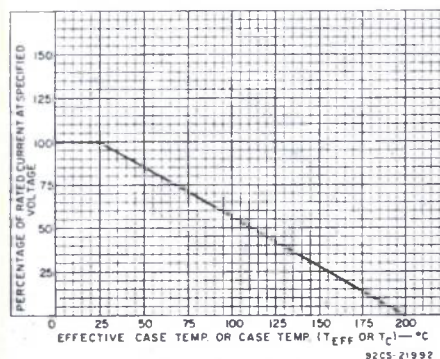


Fig. 1 - Current derating curve for all types.

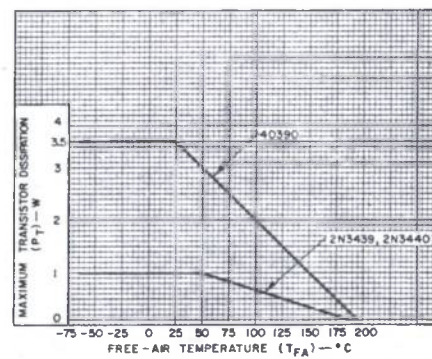


Fig. 2 - Dissipation derating curve for 2N3439, 2N3440, and 40390.

2N4354 • 2N4355 • 2N4356

PNP LOW LEVEL, LOW NOISE AMPLIFIERS AND HIGH CURRENT SWITCHES

DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTORS

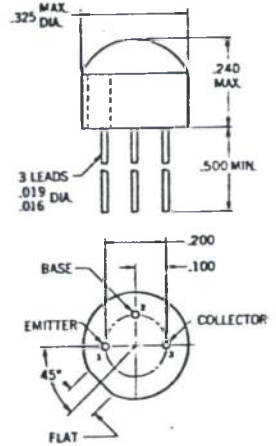
- HIGH BREAKDOWN —60 AND —30 VOLT (MIN) V_{CE0}
- EXCELLENT BETA LINEARITY . . . FROM 100 μ A TO 500 mA
- LOW NOISE FIGURE 3 dB (MAX) AT 1.0 kHz
- LOW $V_{CE(sat)}$ 1.0 VOLT (MAX) AT $I_C = 1.0$ A
- COMPLEMENTARY WITH 2N3567, 2N3568, 2N3569

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures	
Storage Temperature	—55°C to +125°C
Operating Junction Temperature	125°C
Lead Temperature (Soldering, 10 second time limit)	260°C
Maximum Power Dissipation (Notes 2 and 3)	0.8 Watt
Total Dissipation at 25°C Case Temperature at 25°C Ambient Temperature	0.35 Watt

Maximum Voltages	2N4354	2N4355	2N4356
V_{CBO} Collector to Base Voltage	—60 Volts	—60 Volts	—80 Volts
V_{CEO} Collector to Emitter Voltage (Note 4)	—60 Volts	—60 Volts	—80 Volts
V_{EBO} Emitter to Base Voltage	—5.0 Volts	—5.0 Volts	—5.0 Volts

PHYSICAL DIMENSIONS
in accordance with
JEDEC (TO-18) outline



NOTES: All dimensions in inches.
Leads are gold plated.
Package is electrically non-conducting material.
Package weight is 0.66 gram.

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N4354			2N4355			2N4356			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
h_{FE}	DC Pulse Current Gain (Note 5)	25	110		60	180		25	160			$I_C = 100 \mu A$ $V_{CE} = -10 V$
h_{FE}	DC Pulse Current Gain (Note 5)	40	120		75	200		40	180			$I_C = 1 mA$ $V_{CE} = -10 V$
h_{FE}	DC Pulse Current Gain (Note 5)	50	120	500	100	200	400	50	180	250		$I_C = 10 mA$ $V_{CE} = -10 V$
h_{FE}	DC Pulse Current Gain (Note 5)	40	115		75	190		40	170			$I_C = 100 mA$ $V_{CE} = -10 V$
h_{FE}	DC Pulse Current Gain (Note 5)	30	110		75	170		30	160			$I_C = 500 mA$ $V_{CE} = -10 V$
h_{fe}	High Frequency Current Gain ($f = 100 MHz$)	1.0	2.0	5.0	1.0	2.0	5.0	1.0	2.0	5.0		$I_C = 50 mA$ $V_{CE} = -10 V$
BV_{CBO}	Collector to Base Breakdown Voltage	—60			—60			—80			Volts	$I_C = 10 \mu A$ $I_E = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	—5.0			—5.0			—5.0			Volts	$I_C = 0$ $I_E = 10 \mu A$
$V_{CE(sus)}$	Collector to Emitter Sustaining Voltage (Notes 4 and 5)	—60			—60			—80			Volts	$I_C = 10 mA$ $I_B = 0$ (pulsed)
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 5)				—0.5	—1.0					Volts	$I_C = 1.0 A$ $I_B = 100 mA$
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 5)					—1.2					Volts	$I_C = 1.0 A$ $I_B = 100 mA$
$V_{BE(ON)}$	Pulsed Base Emitter "ON" Voltage (Note 5)				—1.05	—1.20					Volts	$I_C = 1.0 A$ $V_{CE} = -1.0 V$

*Planar is a patented Fairchild process.

NOTES:

- (1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
- (2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.
- (3) These ratings give a maximum junction temperature of 125°C and junction to case thermal resistance of 125°C/Watt (derating factor of 8.0 mW/°C); junction to ambient thermal resistance of 286°C/Watt (derating factor of 3.5 mW/°C).
- (4) Rating refers to a high current point where collector to emitter voltage is lowest.
- (5) Pulse Conditions: length = 300 μ s; duty cycle = 1%.
- (6) See switching circuit for exact values of I_C , I_B , and I_E .

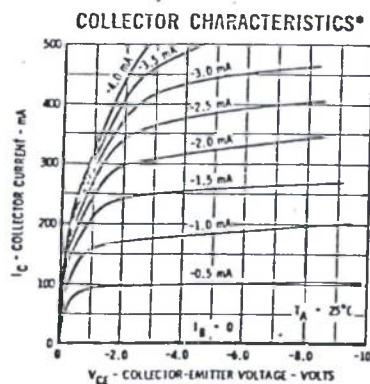
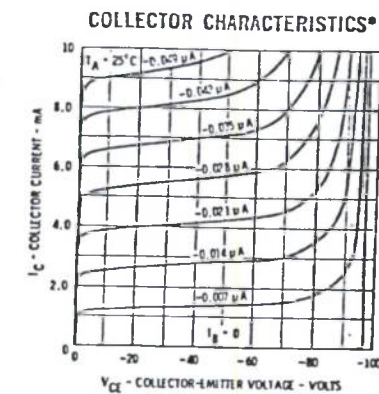
FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

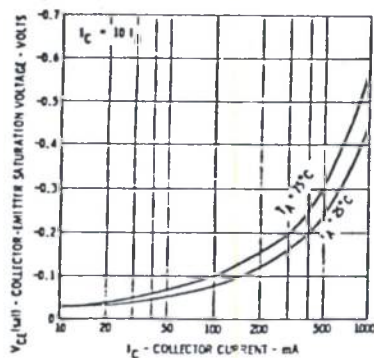
ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	TYP.	MAX.	UNITS	TEST CONDITIONS
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 5)	-0.10	-0.15	Volts	$I_C = 150 \text{ mA}$ $I_B = 15 \text{ mA}$
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 5)	-0.25	-0.5	Volts	$I_C = 500 \text{ mA}$ $I_B = 50 \text{ mA}$
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 5)	-0.8	-0.9	Volts	$I_C = 150 \text{ mA}$ $I_B = 15 \text{ mA}$
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 5)		-1.1	Volts	$I_C = 500 \text{ mA}$ $I_B = 50 \text{ mA}$
$V_{BE(ON)}$	Pulsed Base Emitter "ON" Voltage (Note 5)	-0.95	-1.1	Volts	$I_C = 500 \text{ mA}$ $V_{CE} = -0.5 \text{ V}$
I_{CBO}	Collector Cutoff Current	0.2	50	nA	$I_E = 0$ $V_{CE} = -50 \text{ V}$
$I_{CBO}(+75^\circ\text{C})$	Collector Cutoff Current	0.02	5.0	μA	$I_E = 0$ $V_{CE} = -50 \text{ V}$
I_{EBO}	Emitter to Base Current	1.0	100	nA	$I_C = 0$ $V_{EB} = -4.0 \text{ V}$
C_{cb}	Collector to Base Capacitance ($f = 1.0 \text{ MHz}$)	15	30	pF	$I_C = 0$ $V_{CB} = -10 \text{ V}$
C_{eb}	Emitter to Base Capacitance ($f = 1.0 \text{ MHz}$)	75	110	pF	$I_C = 0$ $V_{EB} = -0.5 \text{ V}$
t_{on}	Turn-on Time (Note 6)	23	100	ns	$I_C \approx 500 \text{ mA}$ $I_{B1} \approx 50 \text{ mA}$
t_{off}	Turn-off Time (Note 6)	200	400	ns	$I_C \approx 500 \text{ mA}$ $I_{B1} \approx 50 \text{ mA}$
NF	Noise Figure ($f = 1.0 \text{ kHz}$)	1.0	3.0	dB	$I_{B2} \approx -50 \text{ mA}$ $I_C = 100 \mu\text{A}$ $V_{CE} = -10 \text{ V}$ $R_S = 1.0 \text{ k}\Omega$

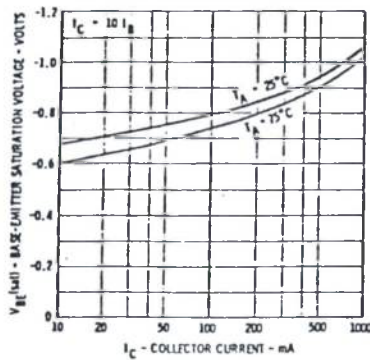
TYPICAL ELECTRICAL CHARACTERISTICS



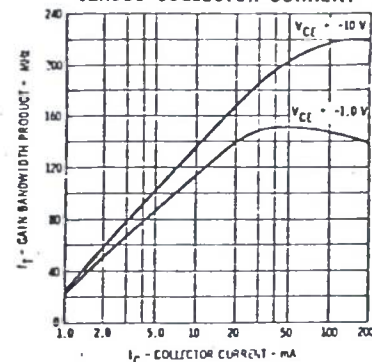
COLLECTOR SATURATION VOLTAGE
VERSUS COLLECTOR CURRENT



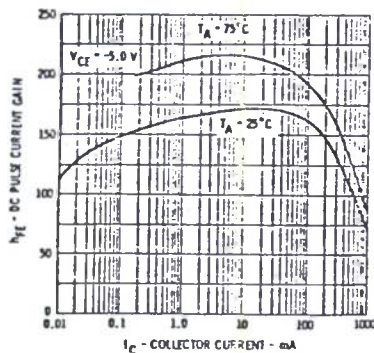
BASE SATURATION VOLTAGE
VERSUS COLLECTOR CURRENT



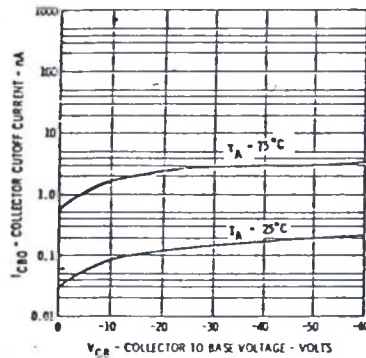
GAIN BANDWIDTH PRODUCT
VERSUS COLLECTOR CURRENT



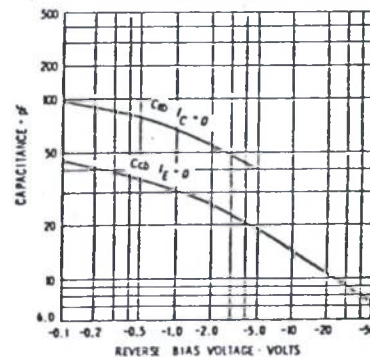
DC PULSE CURRENT GAIN
VERSUS COLLECTOR CURRENT



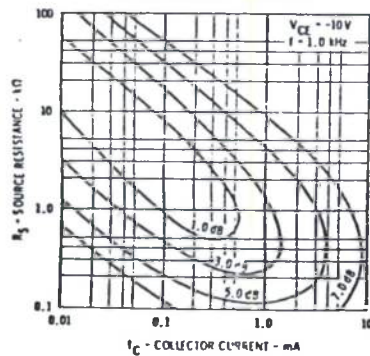
COLLECTOR CUTOFF CURRENT
VERSUS REVERSE BIAS VOLTAGE



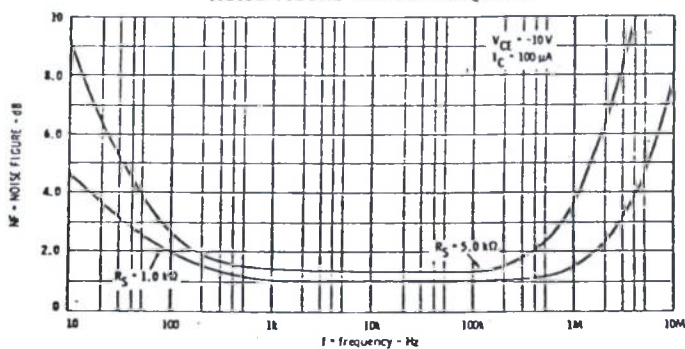
COMMON BASE OPEN CIRCUIT
INPUT AND OUTPUT
CAPACITANCE VERSUS REVERSE
BIAS VOLTAGE



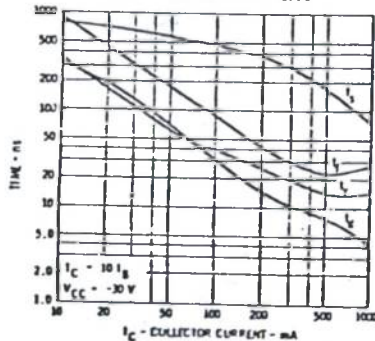
CONTOURS OF CONSTANT NARROW
BAND NOISE FIGURE



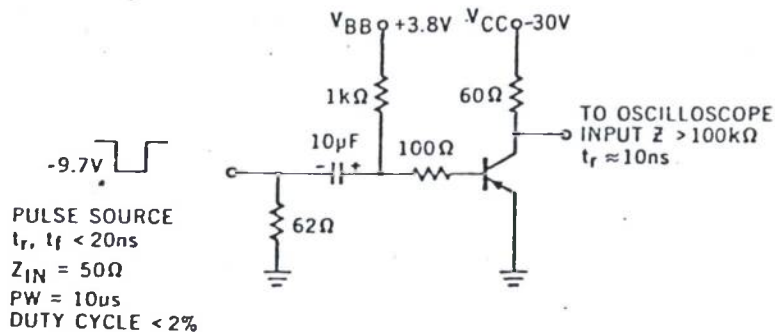
NOISE FIGURE VERSUS FREQUENCY



SWITCHING TIMES VERSUS
COLLECTOR CURRENT



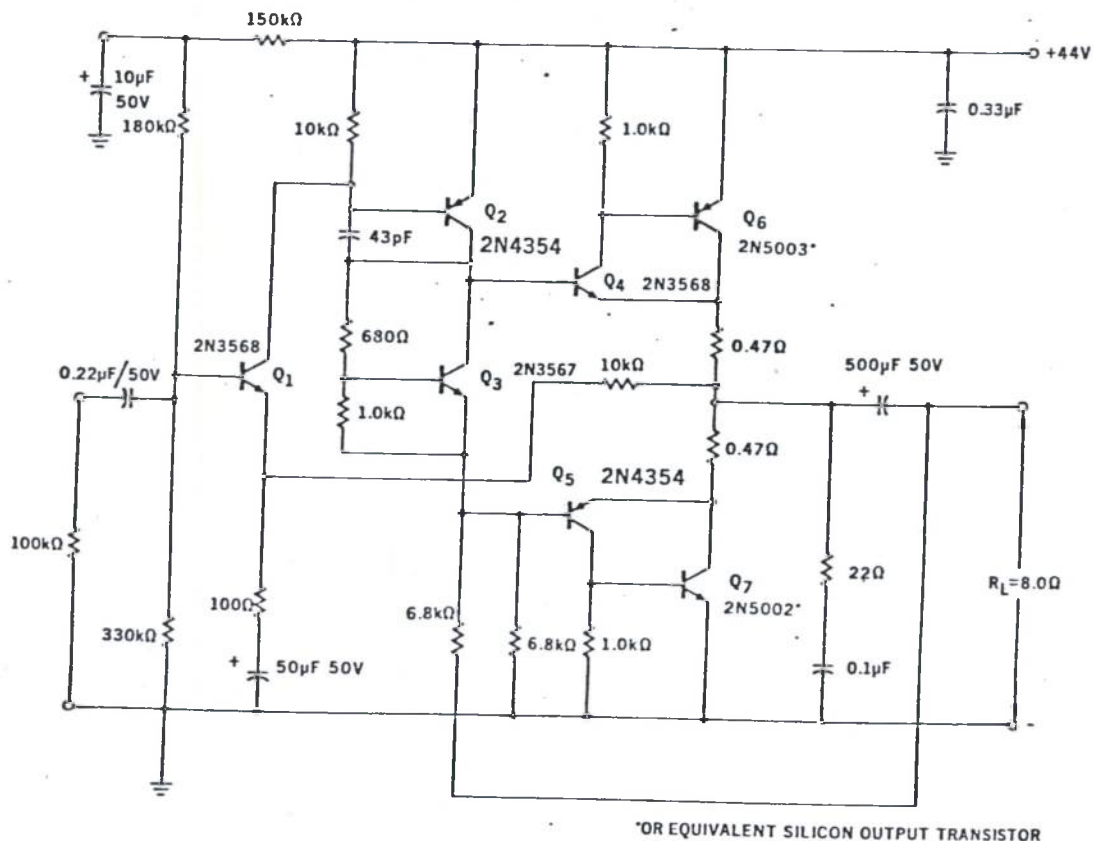
t_{on} AND t_{off} TEST CIRCUIT



TYPICAL SMALL SIGNAL CHARACTERISTICS ($f = 1 \text{ kHz}$)

SYMBOL	CHARACTERISTICS	TYP.	UNITS	TEST CONDITIONS	
h_{ie}	Input Resistance	800	Ω	$I_C = 10 \text{ mA}$	$V_{CE} = -10 \text{ V}$
h_{oe}	Output Conductance	75	μmho	$I_C = 10 \text{ mA}$	$V_{CE} = -10 \text{ V}$
h_{re}	Voltage Feedback Ratio	180	$\times 10^{-4}$	$I_C = 10 \text{ mA}$	$V_{CE} = -10 \text{ V}$
h_{fe}	Small Signal Current Gain	140		$I_C = 10 \text{ mA}$	$V_{CE} = -10 \text{ V}$

TYPICAL 25 WATT POWER AMPLIFIER
USING THE 2N4354 IN THE DRIVER STAGES

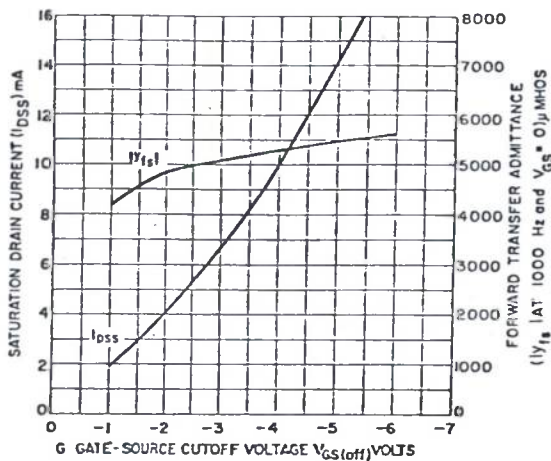


ELECTRICAL CHARACTERISTICS @ 25°C (UNLESS OTHERWISE NOTED)

	SYM.	2N4416 -16 A		2N4417		Units	CONDITIONS
		min.	max.	min.	max.		
Small-Signal, Common-Source, Short-Circuit Output Susceptance	$1M (y_{os})$		4000		3000	μmhos	$V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 400 \text{ MHz}$
Small-Signal, Common-Source, Short-Circuit Output Conductance	$1RE (y_{os})$		75		75	μmhos	$V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 100 \text{ MHz}$
Small-Signal, Common-Source, Short-Circuit Output Susceptance	$1M (y_{os})$		1000		800	μmhos	$V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 100 \text{ MHz}$
Small-Signal, Common-Source, Short-Circuit Forward Transconductance	$1RE (y_{fs})$		4000		4000	μmhos	$V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 400 \text{ MHz}$
Common-Source Power Gain	G_{ps}	10		10		dB	$V_{DS} = 15 \text{ V}, I_D = 5 \text{ mA}, f = 400 \text{ MHz}$ (See Fig. 1)
Common-Source Power Gain	G_{ps}	18		18		dB	$V_{DS} = 15 \text{ V}, I_D = 5 \text{ mA}, f = 100 \text{ MHz}$ (See Fig. 22)
Common-Source Spot Noise Figure	NF		4.0		4.0	dB	$V_{DS} = 15 \text{ V}, I_D = 5 \text{ mA}, f = 400 \text{ MHz}$ (See Fig. 22) $R_G = 1000 \text{ ohms}$
Common-Source Spot Noise Figure	NF		2.0		2.0	dB	$V_{DS} = 15 \text{ V}, I_D = 5 \text{ mA}, f = 100 \text{ MHz}$ (See Fig. 22) $R_G = 1000 \text{ ohms}$

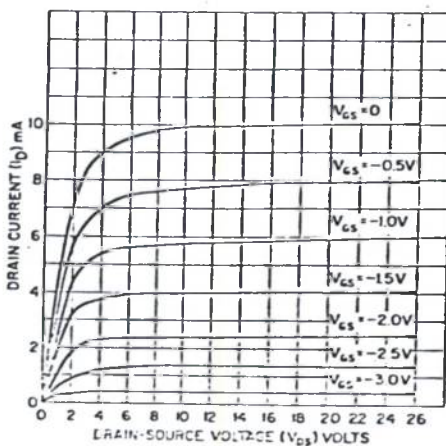
TYPICAL PERFORMANCE CURVES @ 25°C (UNLESS OTHERWISE NOTED)

PARAMETER INTER-RELATIONSHIP



SATURATION DRAIN CURRENT AND FORWARD TRANSFER ADMITTANCE VS. GATE-SOURCE CUTOFF VOLTAGE
FIGURE 1

DRAIN CHARACTERISTIC



DRAIN CURRENT VS. DRAIN-SOURCE VOLTAGE

TRANSFER CHARACTERISTIC

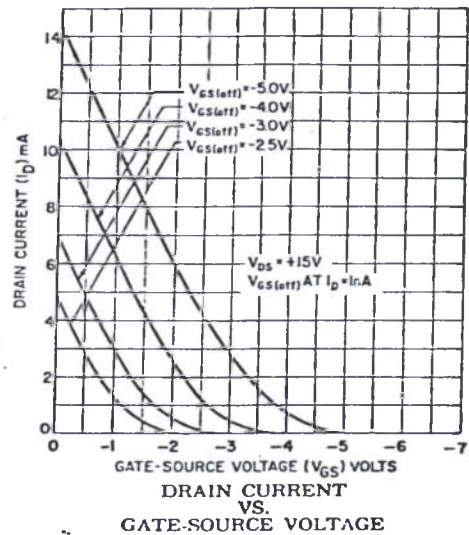
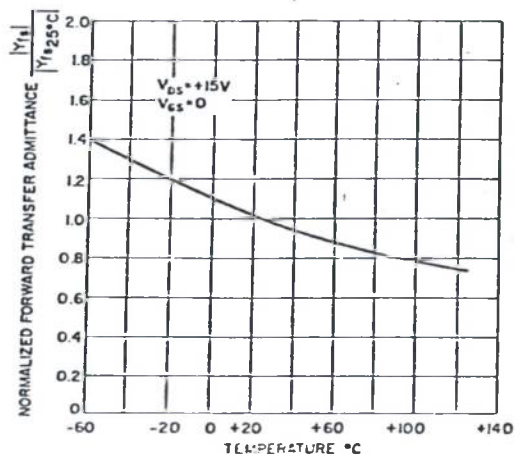


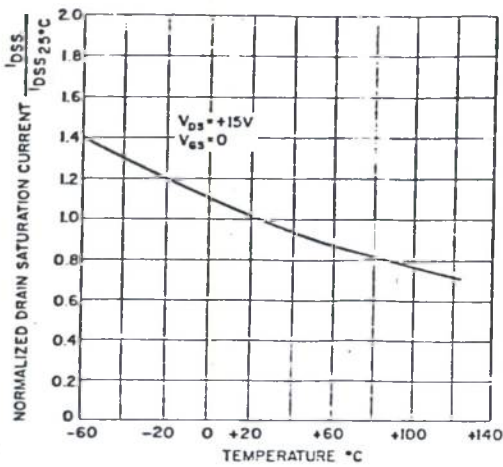
FIGURE 2

TRANSFER CHARACTERISTIC



NORMALIZED FORWARD TRANSFER ADMITTANCE VS. TEMPERATURE

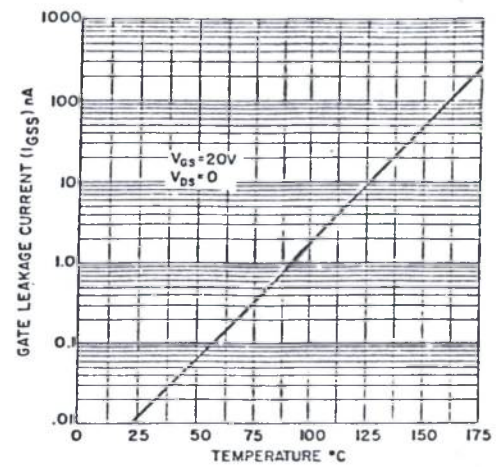
DRAIN CHARACTERISTIC



NORMALIZED DRAIN SATURATION CURRENT
VS.
TEMPERATURE

FIGURE 5

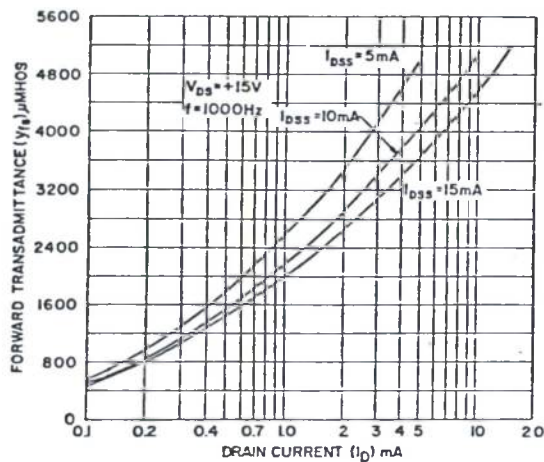
LEAKAGE CHARACTERISTIC



GATE LEAKAGE CURRENT
VS.
TEMPERATURE

FIGURE 6

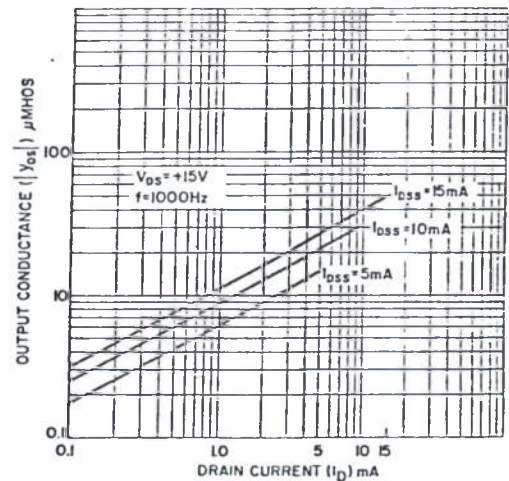
TRANSFER CHARACTERISTIC



FORWARD TRANSADMITTANCE
VS.
DRAIN CURRENT

FIGURE 7

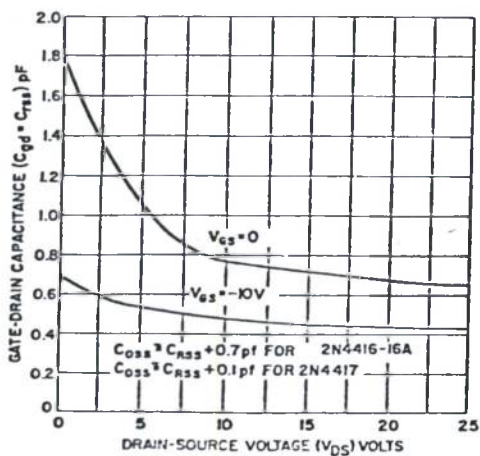
OUTPUT CHARACTERISTIC



OUTPUT CONDUCTANCE
VS.
DRAIN CURRENT

FIGURE 8

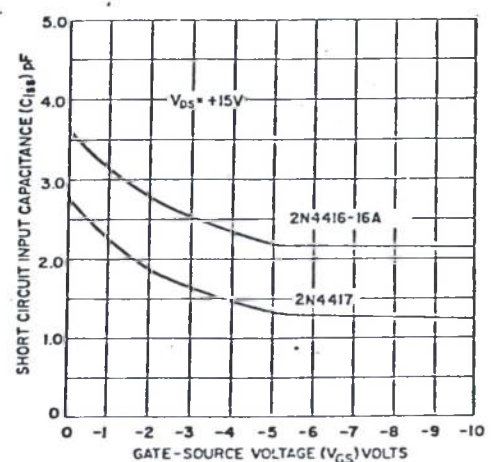
CAPACITANCE VOLTAGE CHARACTERISTIC



GATE-DRAIN CAPACITANCE
VS.
DRAIN SOURCE VOLTAGE

FIGURE 9

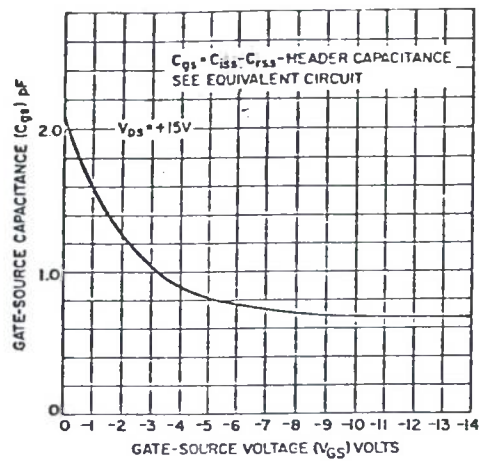
CAPACITANCE VOLTAGE CHARACTERISTIC



SHORT CIRCUIT INPUT CAPACITANCE
VS.
GATE-SOURCE VOLTAGE

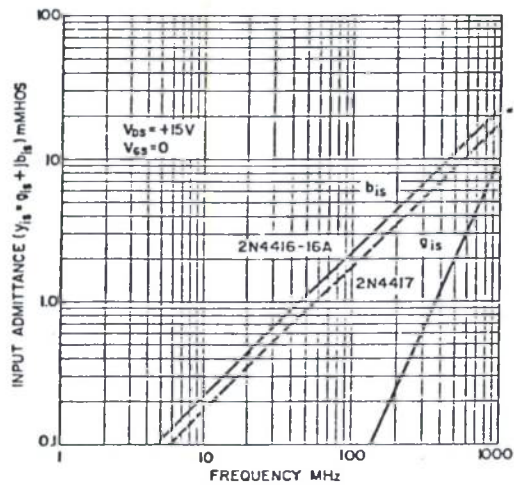
FIGURE 10

CAPACITANCE VOLTAGE CHARACTERISTIC

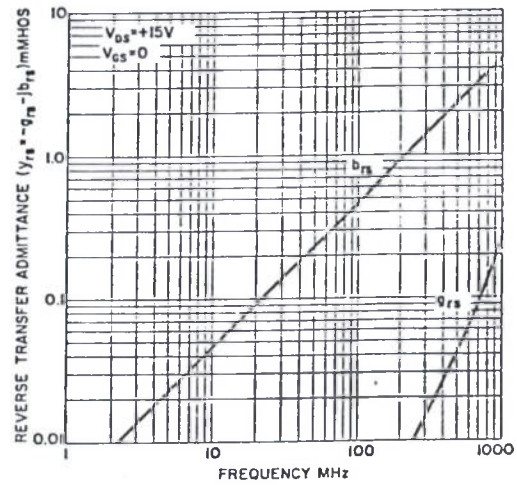


GATE-SOURCE CAPACITANCE
VS.
GATE-SOURCE VOLTAGE
.FIGURE 11

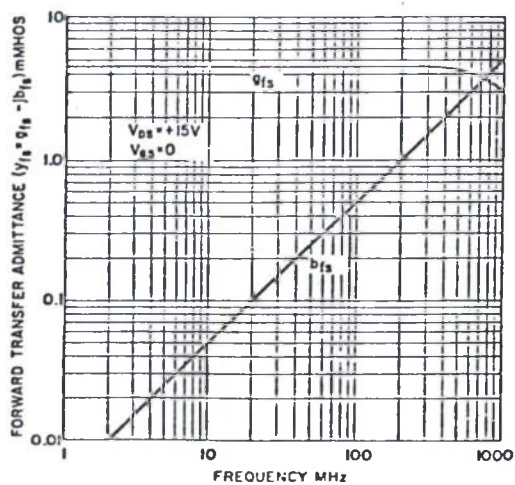
HIGH FREQUENCY COMMON SOURCE CHARACTERISTICS



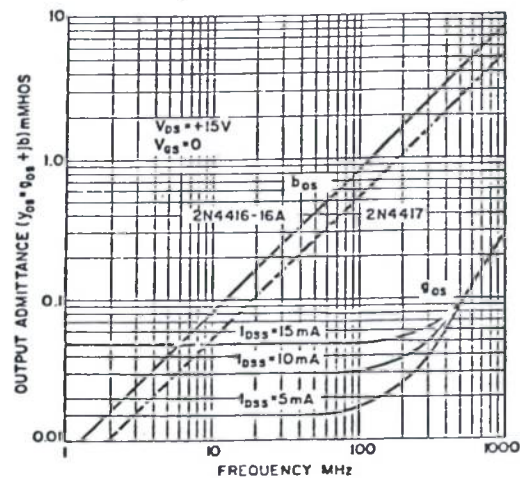
INPUT ADMITTANCE
VS.
FREQUENCY
FIGURE 12



REVERSE TRANSFER ADMITTANCE
VS.
FREQUENCY
FIGURE 13

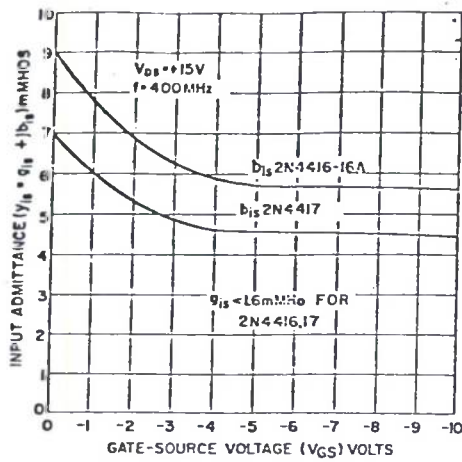


FORWARD TRANSFER ADMITTANCE
VS.
FREQUENCY
FIGURE 14



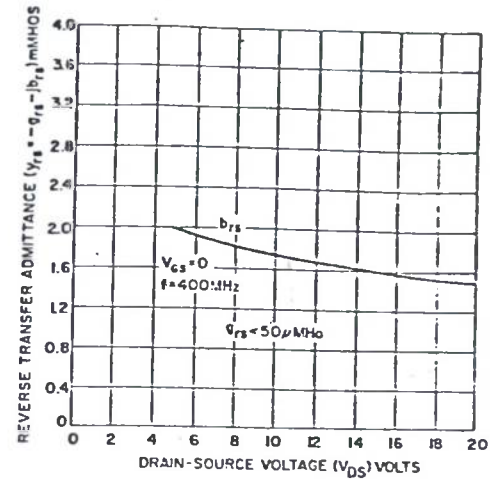
OUTPUT ADMITTANCE
VS.
FREQUENCY
FIGURE 15

HIGH FREQUENCY COMMON SOURCE CHARACTERISTICS



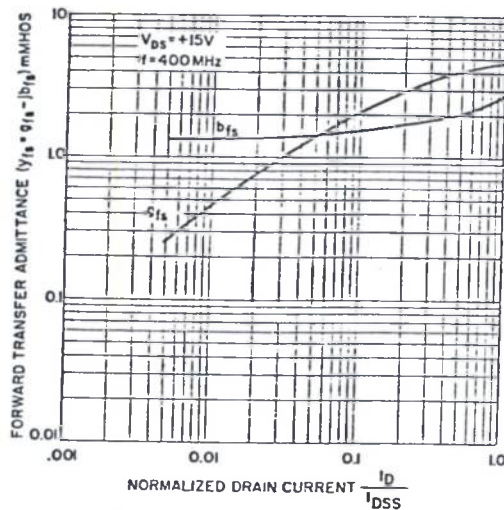
INPUT ADMITTANCE
VS.
GATE-SOURCE VOLTAGE

FIGURE 16



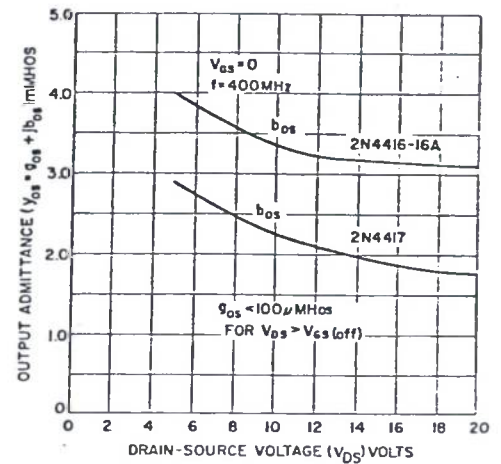
REVERSE TRANSFER ADMITTANCE
VS.
DRAIN-SOURCE VOLTAGE

FIGURE 17



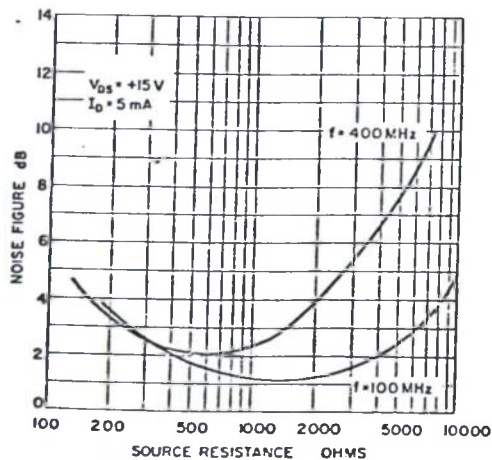
FORWARD TRANSFER ADMITTANCE
VS.
NORMALIZED DRAIN CURRENT

FIGURE 18



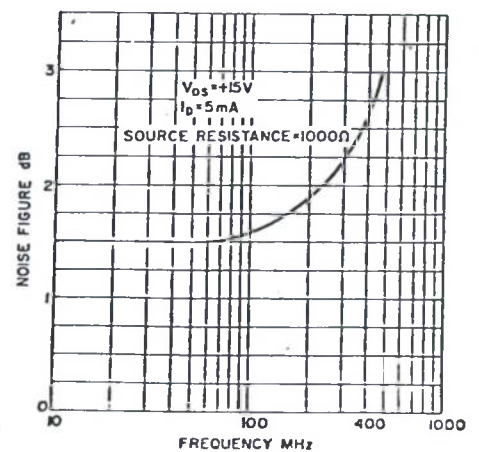
OUTPUT ADMITTANCE
VS.
DRAIN SOURCE VOLTAGE

FIGURE 19



NOISE FIGURE
VS.
SOURCE RESISTANCE

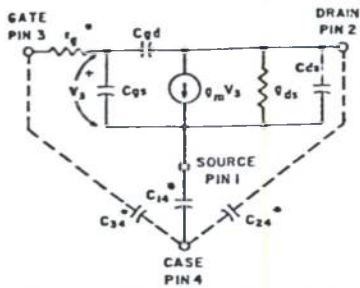
FIGURE 20



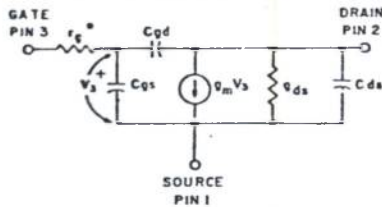
NOISE FIGURE
VS.
FREQUENCY

FIGURE 21

EQUIVALENT CIRCUIT



Approximate small signal equivalent circuit for the 2N4416 Field Effect Transistor.



Approximate small signal equivalent circuit for the 2N4417 Field Effect Transistor.

The 2N4416 and 2N4417 transistors are identical in every respect except for their respective package configurations. Therefore capacitance values for C_{gs} , C_{gd} , and C_{ds} should be set equal to zero, in equation 1 through 4, when computing the y parameters for the 2N4417. All of the other circuit component values are the same for both devices. Typical component values for C_{gs} , C_{gd} , g_{ds} , and g_{gd} may be obtained for any set of bias conditions, from the curves.

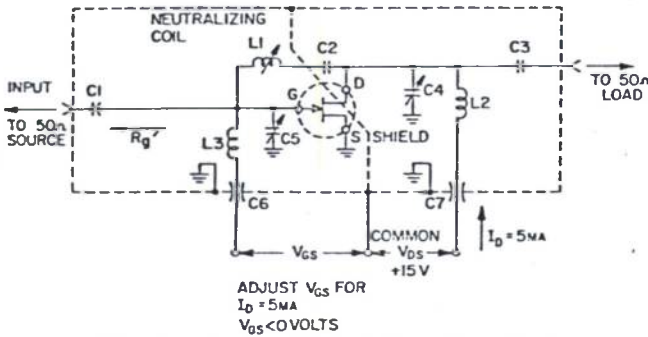
1. $y_{is} \approx r_g[\omega(C_{gs} + C_{gd})F + j\omega(C_{gs} + C_{gd})]$
2. $y_{rs} \approx -\omega^2 C_{gd}(C_{gs} + C_{gd})r_g - j\omega C_{gd}$
3. $y_{fs} \approx g_{m1} - \omega^2 C_{gd}(C_{gs} + C_{gd})r_g - j\omega[C_{gd} + (C_{gs} + C_{gd})r_g g_{m1}]$
4. $y_{os} \approx g_{ds} + (\omega C_{gd})^2 r_g + j\omega(C_{gs} + C_{gd} + C_{ds})$

Small signal common source y parameter equations for the 2N4416 and 2N4417 Field Effect Transistors.

NOTES:

1. The above equations are accurate to about 1 GHz and are good for both the 2N4416 and 2N4417 Field Effect Transistors.
2. The case is connected to the source for the common source configuration and to the gate for common gate operation.
3. C_{gs} , C_{gd} , and C_{ds} are pin to case capacitances for the TO-72 header $C_{gs} \approx 0.6$ pF, $C_{gd} \approx 0.6$ pF, $C_{ds} \approx 0.7$ pF.
4. $C_{ds} \approx 0.1$ pF.
5. $r_g \approx 24$ ohms for both the 2N4416 and 2N4417 Field Effect Transistors.
6. $g_{m1} = |y_{fs}|$ at 1000 Hz.
7. $g_{ds1} = |y_{os}|$ at 1000 Hz.
8. All references to 2N4416, are applicable to 2N4416A.

TEST CIRCUIT



100 MHz & 400 MHz NEUTRALIZED AMPLIFIER

FIGURE 22

REF. DESIG.	VALUE	
	100 MHz	400 MHz
C1	7.0 pF	1.8 pF
C2	1000 pF	27 pF
C3	3.0 pF	1.0 pF
C4	1.0-12 pF	0.8-8 pF
C5	1.0-12 pF	0.8-8 pF
C6	0.0015 μ F	0.001 μ F
C7	0.0015 μ F	0.001 μ F
L1	3.0 μ H	0.2 μ H
L2	0.25 μ H	0.03 μ H
L3	0.14 μ H	0.022 μ H

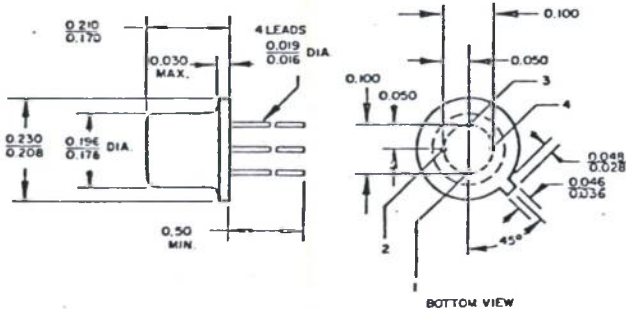
NOTES

1. Amplifier used to measure power gain and noise figure.
2. Transformed equivalent Source resistance (R_g') is 1000 Ω at 100 MHz for 100 MHz amplifier, and 1000 Ω at 400 MHz for 400 MHz amplifier.
3. When using 2N4416, pin 4 (case) should be grounded.
4. All references to 2N4416 are applicable to 2N4416A.

MECHANICAL DATA

All dimensions in inches unless otherwise noted

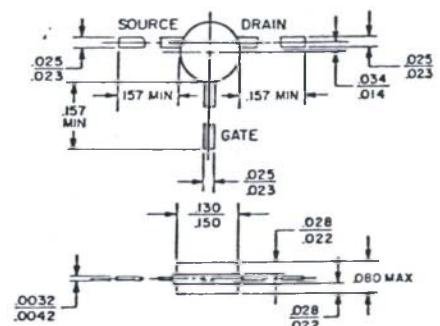
2N4416-16A: JEDEC TO-72



TERMINAL CONNECTIONS

- 1—Source
- 2—Drain
- 3—Gate
- 4—Case

2N4417: Union Carbide CC-3



PRINTED IN U.S.



SEMICONDUCTOR

2N4888

LOW NOISE HIGH VOLTAGE AMPLIFIER

DIFFUSED SILICON PLANAR* II TRANSISTORS

- VERY HIGH VOLTAGE (V_{CE0}) -- 150 VOLTS (Min.)
- LOW NOISE FIGURE -- 3.0 dB (Max.) @ 1.0 kHz
- LOW OUTPUT CAPACITANCE (C_{ob0}) -- 4.0 pF (Max.)
- HIGH BETA (h_{FE}) -- 80-300 @ 10 mA
- EXCELLENT BETA LINEARITY FROM 10 μ A to 50 mA

ABSOLUTE MAXIMUM RATINGS [Note 1]

Maximum Temperatures

Storage Temperature

Operating Junction Temperature

Soldering Temperature (10 second time limit)

Maximum Power Dissipation

Total Dissipation at 25°C Case Temperature (Note 2)

at 75°C Case Temperature (Note 2)

at 25°C Ambient Temperature (Note 2)

Maximum Voltages

V_{CBO} Collector to Base Voltage

V_{CEO} Collector to Emitter Voltage (Note 3)

V_{EB0} Emitter to Base Voltage

-55°C to +125°C

+125°C

+260°C

0.8 Watt

0.4 Watt

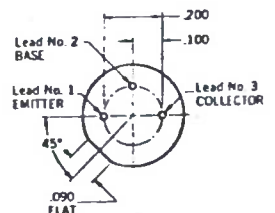
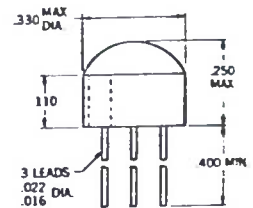
0.3 Watt

-150 Volts

-150 Volts

-6.0 Volts

PHYSICAL DIMENSIONS



NOTES: All dimensions in inches.
Leads are gold plated copper.
Package weight is 0.68 gram.

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N4888			2N4889			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
V_{CE0}	Collector to Emitter Sustaining Voltage	-150			-150			Volts	$I_C = 2.0 \text{ mA}$ $I_E = 0$
BV_{CE0}	Collector to Base Breakdown Voltage	-150			-150			Volts	$I_C = 100 \mu\text{A}$ $I_E = 0$
NF	Narrow Band Noise Figure ($f = 100 \text{ Hz}$)				3.0	10		dB	$I_C = 250 \mu\text{A}$ $V_{CE} = -5.0 \text{ V}$ $R_S = 1.0 \text{ k}\Omega$ B.W. = 15 Hz
NF	Narrow Band Noise Figure ($f = 1.0 \text{ kHz}$)				0.8	3.0		dB	$I_C = 30 \mu\text{A}$ $V_{CE} = -5.0 \text{ V}$ $R_S = 10 \text{ k}\Omega$ B.W. = 150 Hz
NF	Narrow Band Noise Figure ($f = 10 \text{ kHz}$)				1.5	3.0		dB	$I_C = 250 \mu\text{A}$ $V_{CE} = -5.0 \text{ V}$ $R_S = 1.0 \text{ k}\Omega$ B.W. = 1.5 kHz
NF	Wide Band Noise Figure ($f = 10 \text{ Hz to } 10 \text{ kHz}$)				2.0	4.0		dB	$I_C = 250 \mu\text{A}$ $V_{CE} = -5.0 \text{ V}$ $R_S = 1.0 \text{ k}\Omega$ B.W. = 15.7 kHz
NF	Narrow Band Noise Figure ($f = 1.0 \text{ MHz}$)				2.0	4.0		dB	$I_C = 1.0 \text{ mA}$ $V_{CE} = -10 \text{ V}$ $R_S = 1.0 \text{ k}\Omega$ B.W. = 2.0 kHz
h_{FE}	DC Pulse Current Gain (Note 4)		30		60	135			$I_C = 100 \mu\text{A}$ $V_{CE} = -10 \text{ V}$
h_{FE}	DC Pulse Current Gain (Note 4)	30	40		70	150			$I_C = 1.0 \text{ mA}$ $V_{CE} = -10 \text{ V}$
h_{FE}	DC Pulse Current Gain (Note 4)	40	45	400	80	150	300		$I_C = 10 \text{ mA}$ $V_{CE} = -10 \text{ V}$
C_{ob0}	Common-Base, Open Circuit Output Capacitance ($f = 1.0 \text{ MHz}$)		2.5	4.0		2.5	4.0	pF	$V_{CE} = -20 \text{ V}$ $I_E = 0$

Additional Electrical Characteristics on page 2

* Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

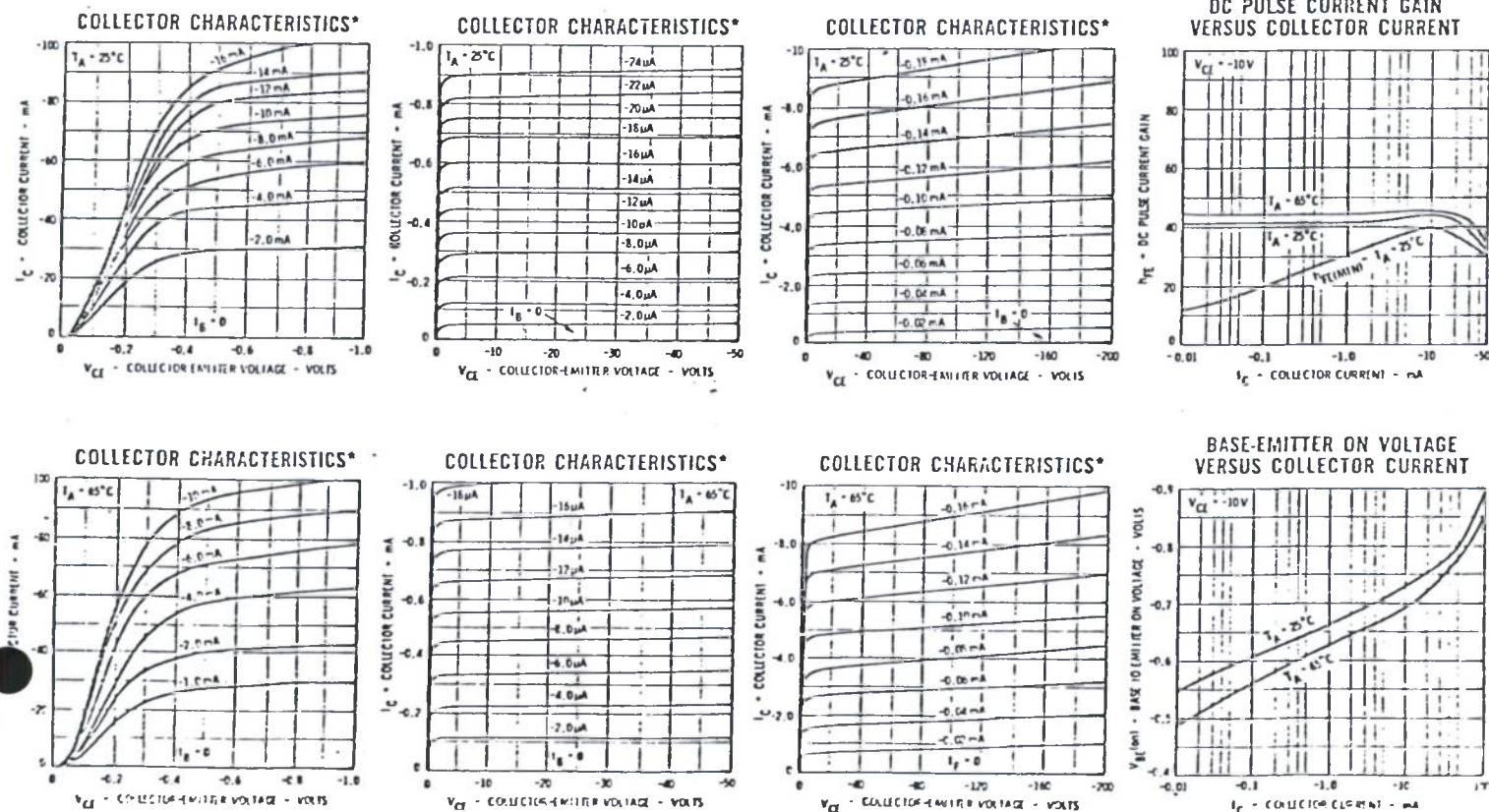
SYMBOL	CHARACTERISTIC	2N4888			2N4889			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
I_{CBO}	Collector Cutoff Current		0.7	50		0.7	10	nA	$V_{CE} = -100V$ $I_E = 0$
$I_{CBO}(65^\circ C)$	Collector Cutoff Current		0.01	2.5		0.01	0.5	μA	$V_{CE} = -100V$ $I_E = 0$
$V_{CE}(sat)$	Pulsed Collector Saturation Voltage (Note 4)		-0.1	-0.5		-0.1	-0.5	Volts	$I_C = 10mA$ $I_B = 1.0mA$
BV_{EBO}	Emitter to Base Breakdown Voltage	-6.0			-6.0			Volts	$I_E = 10\mu A$ $I_C = 0$
I_{EBO}	Emitter Cutoff Current		0.4	50		0.4	10	nA	$V_{EB} = -4.0V$ $I_C = 0$
$V_{BE}(on)$	Pulsed Base Emitter On Voltage (Note 4)		-0.66	-0.8		-0.59	-0.7	Volts	$I_C = 1.0mA$ $V_{CE} = -10V$
$V_{BE}(sat)$	Pulsed Base Saturation Voltage (Note 4)		-0.74	-0.9		-0.74	-0.9	Volts	$I_C = 10mA$ $I_B = 1.0mA$
C_{in}	Common-Base, Open-Circuit Input Capacitance		11	30		11	25	pF	$V_{EB} = -0.5V$ $I_C = 0$
h_{fe}	High Frequency Current Gain ($f = 20MHz$)	1.5	1.8	8.0	2.0	3.3	8.0		$I_C = 1.0mA$ $V_{CE} = -10V$

NOTES:

- (1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
- (2) These ratings give a maximum junction temperature of 125°C and junction to case thermal resistance of 125°C/Watt (derating factor of 8.0 mW/°C); junction to ambient thermal resistance of 333°C/Watt (derating factor of 3.0 mW/°C).
- (3) This rating refers to a high current point where collector to emitter voltage is lowest. For more information send for Fairchild Publication APP-4/2.
- (4) Pulse Conditions: length = 300 μs ; duty cycle = 1%.

2N4888

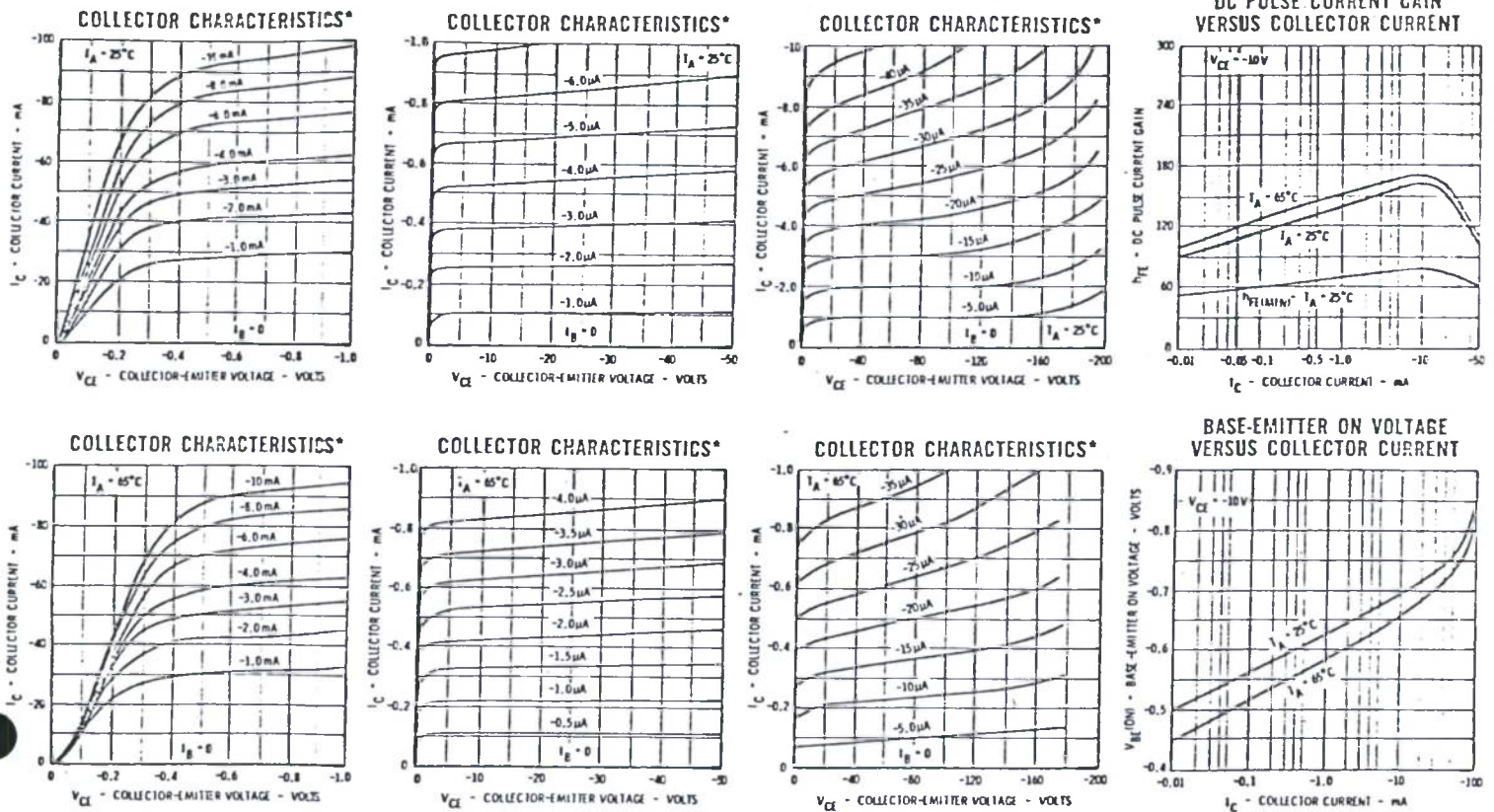
TYPICAL ELECTRICAL CHARACTERISTICS



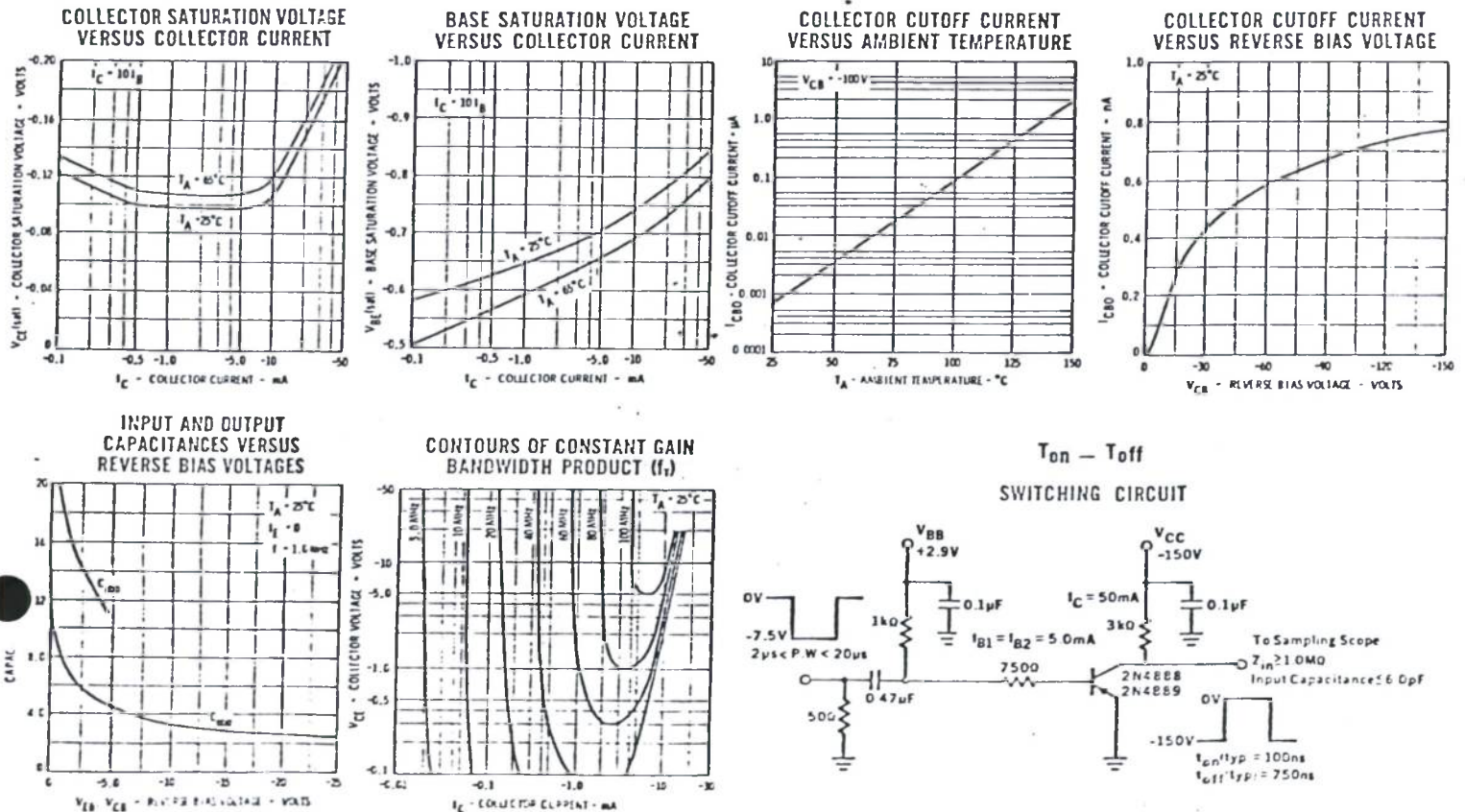
FAIRCHILD TRANSISTORS 2N4888 • 2N4889

2N4889

TYPICAL ELECTRICAL CHARACTERISTICS

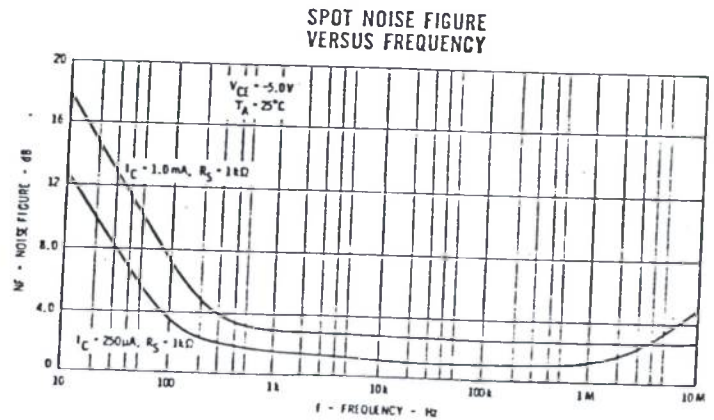
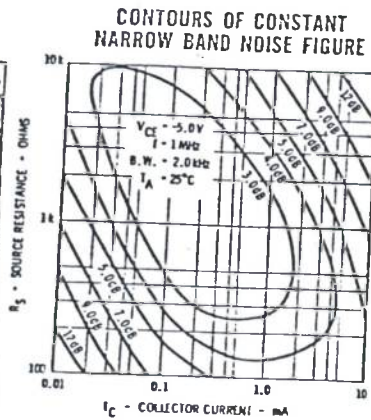
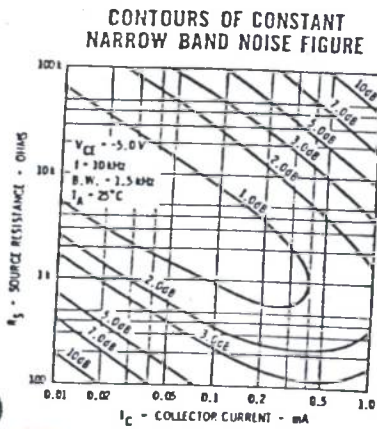
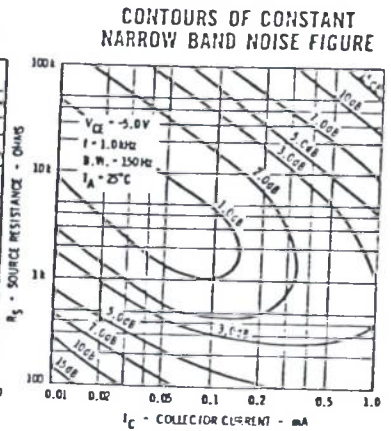
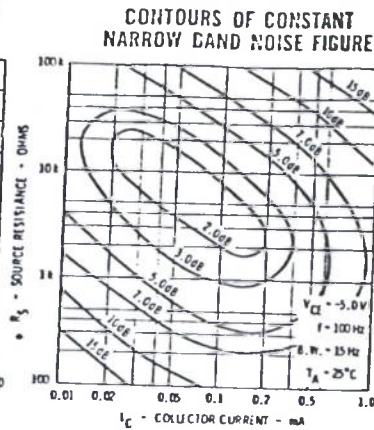
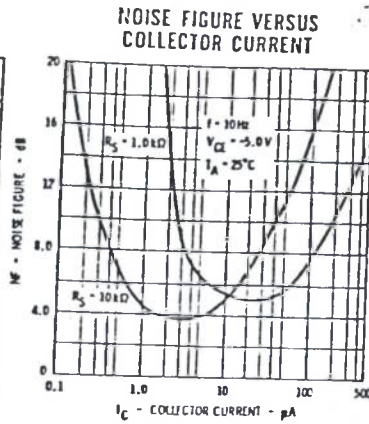
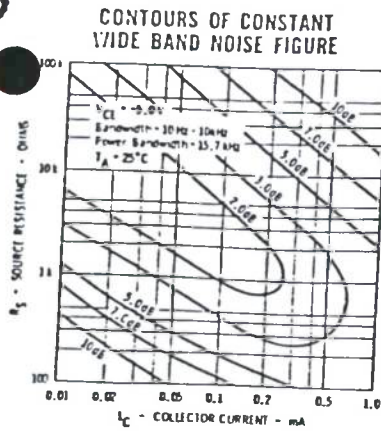


2N4888 • 2N4889



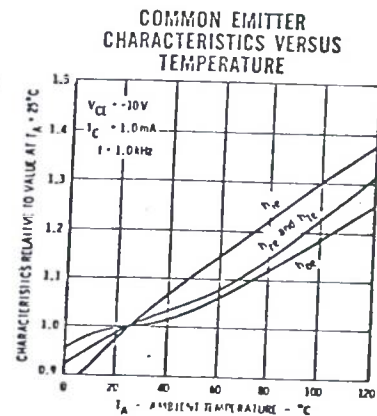
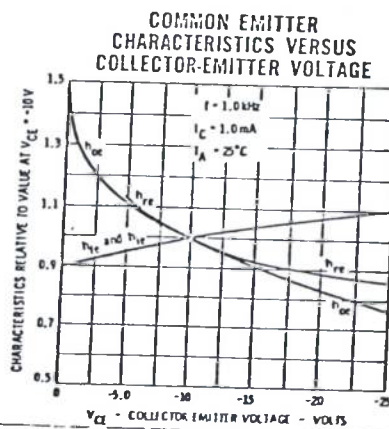
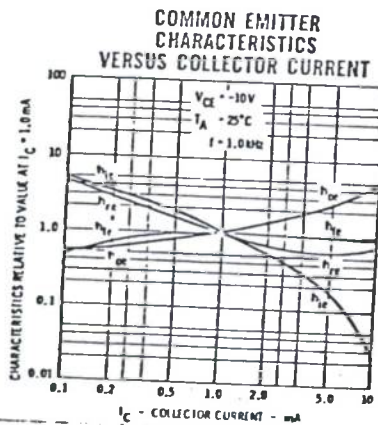
2N4889

TYPICAL ELECTRICAL CHARACTERISTICS



ALL SIGNAL CHARACTERISTICS ($f = 1.0 \text{ kHz}$)

SYMBOL	CHARACTERISTIC	2N4888			2N4889			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
h_{ie}	Small Signal Current Gain	30	40	500	65	150	400		$I_c = 1.0 \text{ mA}$ $V_{ce} = -10 \text{ V}$
h_{ie}	Input Resistance	0.75	1.2	20	1.7	5.0	12	$k\Omega$	$I_c = 1.0 \text{ mA}$ $V_{ce} = -10 \text{ V}$
h_{oe}	Output Conductance	1.4	2.5	40	3.0	10	25	μmhos	$I_c = 1.0 \text{ mA}$ $V_{ce} = -10 \text{ V}$
h_{fe}	Voltage Feedback Ratio		1.0			2.5	5.0	$\times 10^{-4}$	$I_c = 1.0 \text{ mA}$ $V_{ce} = -10 \text{ V}$



SEMICONDUCTOR

Fairchild cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in a Fairchild product. No other circuit patent licenses are implied.

2N4916 • 2N4917

PNP HIGH-SPEED SWITCH AND RF AMPLIFIER

DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTORS

- HIGH BETA (h_{FE}) -- 150 to 300 @ 10 mA
- HIGH FREQUENCY (f_T) -- 450 MHz Min. @ 10 mA
- EXCELLENT R.F. PERFORMANCE ($r_{b'e}$) -- 50 ps Max.
- LOW CAPACITANCE (C_{ob}) -- 4.5 pF Max.
- LOW NOISE (100 MHz N.F.) -- 6.0 dB Max.

ABSOLUTE MAXIMUM RATINGS [Note 1]

Maximum Temperatures

- Storage Temperature
- Operating Junction Temperature
- Lead Temperature (Soldering, 10 sec time limit)

-55°C to +125°C
+125°C Maximum
+260°C Maximum

Maximum Power Dissipation

- Total Dissipation at 25°C Case Temperature [Notes 2 and 3]
- at 25°C Ambient Temperature [Notes 2 and 3]

0.5 Watt
0.2 Watt

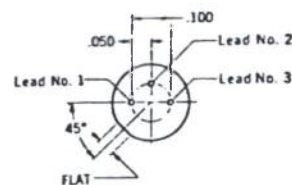
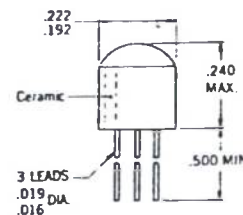
Maximum Voltages and Current

- V_{CB0} Collector to Base Voltage
- V_{CE0} Collector to Emitter Voltage [Note 4]
- V_{EB0} Emitter to Base Voltage
- I_C Collector Current

-30 Volts
-30 Volts
-5.0 Volts
100 mA

PHYSICAL DIMENSIONS

Epoxy package
TO-106



NOTES: All dimensions in inches
All leads electrically isolated from case
Package weight is 0.31 gram

CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N4916			2N4917			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
h_{FE}	DC Current Gain	40	70		100	150			$I_C = 100 \mu A$ $V_{CE} = -1.0 V$
h_{FE}	DC Current Gain	60	100		150	200			$I_C = 1.0 mA$ $V_{CE} = -1.0 V$
h_{FE}	DC Pulse Current Gain [Note 5]	70	150	200	150	200	300		$I_C = 10 mA$ $V_{CE} = -1.0 V$
h_{FE}	DC Pulse Current Gain [Note 5]	15	30		30	60			$I_C = 50 mA$ $V_{CE} = -1.0 V$
$V_{CE}(sat)$	Collector Saturation Voltage	-0.07	-0.13		-0.07	-0.13		Volts	$I_C = 1.0 mA$ $I_B = 0.1 mA$
$V_{CE}(sat)$	Pulsed Collector Saturation Voltage [Note 5]	-0.1	-0.14		-0.1	-0.14		Volts	$I_C = 10 mA$ $I_B = 1.0 mA$
$V_{CE}(sat)$	Pulsed Collector Saturation Voltage [Note 5]	-0.2	-0.3		-0.2	-0.3		Volts	$I_C = 50 mA$ $I_B = 5.0 mA$
$V_{BE}(sat)$	Base Saturation Voltage	-0.65	-0.75		-0.65	-0.75		Volts	$I_C = 1.0 mA$ $I_B = 0.1 mA$
$V_{BE}(sat)$	Pulsed Base Saturation Voltage [Note 5]	-0.7	-0.77	-0.9	-0.7	-0.77	-0.9	Volts	$I_C = 10 mA$ $I_B = 1.0 mA$
$V_{BE}(sat)$	Pulsed Base Saturation Voltage [Note 5]	-0.75	-0.88	-1.1	-0.75	-0.88	-1.1	Volts	$I_C = 50 mA$ $I_B = 5.0 mA$
t_{on}	Turn On Time [Note 6]		20	40		20	40	ns	$I_C \approx 50 mA$ $I_{B1} \approx 5.0 mA$
t_{off}	Turn Off Time [Note 6]		95	150		95	150	ns	$I_C \approx 50 mA$ $I_{B1} \approx 5.0 mA$
h_{FE}	High Frequency Current Gain ($f = 100 MHz$)	4.0	5.5		4.5	6.0			$I_C = 10 mA$ $V_{CE} = -20 V$

* Planar is a patented Fairchild process.

NOTES:

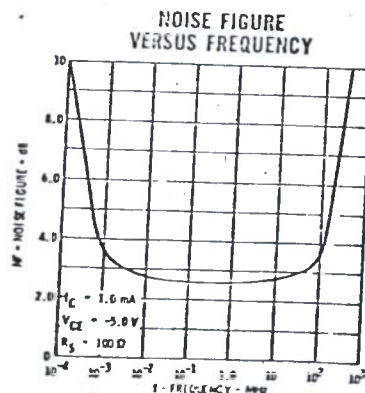
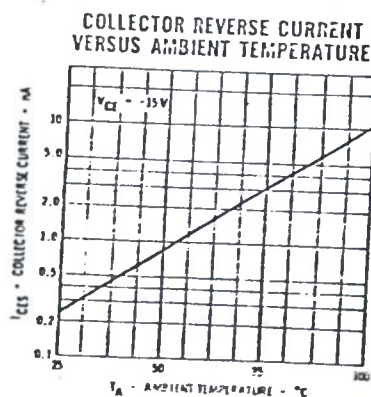
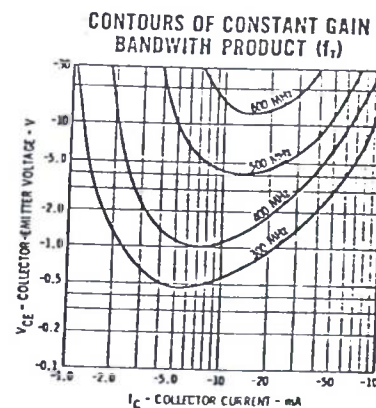
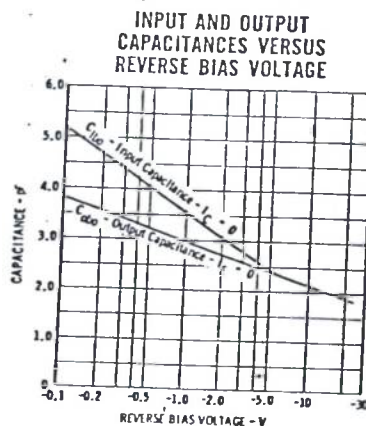
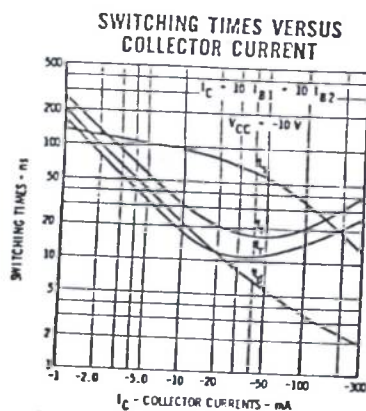
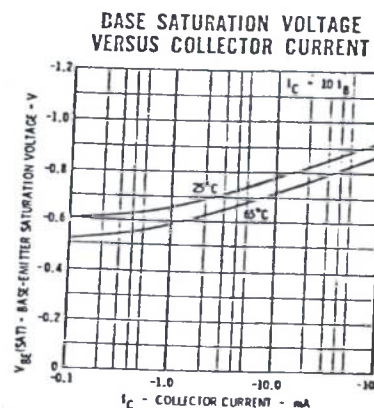
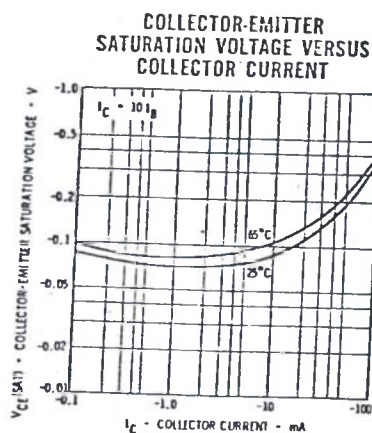
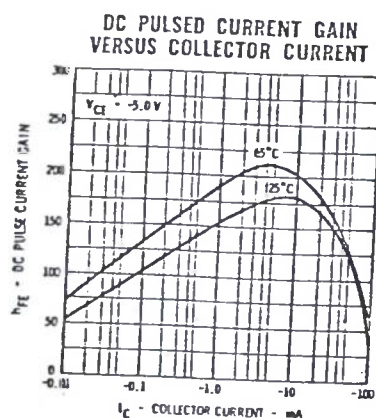
- (1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
- (2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.
- (3) These ratings give a maximum junction temperature of 125°C and junction to case thermal resistance of 200°C/Watt (derating factor of 5.0 mW/°C); junction to ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).
- (4) This rating refers to a high-current point where collector to emitter voltage is lowest.
- (5) Pulse Conditions: length = 300 μs ; duty cycle = 1%.
- (6) See switching circuit for exact values of I_C , I_{B1} and I_{B2} .
- (7) Power Bandwidth of 15.7 kHz with 3 dB points at 10 Hz and 10 kHz.

FAIRCHILD
SEMICONDUCTOR

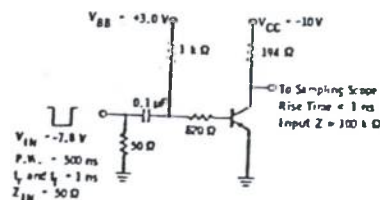
ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N4916			2N4917			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
V_{CE0} (sust)	Collector to Emitter Sustaining Voltage [Notes 4 and 5]	-30			-30			Volts	$I_C = 10 \text{ mA}$ $I_B = 0$
BV_{CBO}	Collector to Base Breakdown Voltage	-30			-30			Volts	(pulsed) $I_C = 10 \mu\text{A}$ $I_E = 0$
BV_{CES}	Collector to Emitter Breakdown Voltage	-30			-30			Volts	$I_C = 10 \mu\text{A}$ $V_{BE} = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	-5.0			-5.0			Volts	$I_C = 0$ $I_E = 10 \mu\text{A}$
I_{CES}	Collector Reverse Current		25			25		nA	$V_{CE} = -15 \text{ V}$ $V_{BE} = 0$
I_{CIS} (65°C)	Collector Reverse Current		25			25		nA	$V_{CE} = -15 \text{ V}$ $V_{BE} = 0$
C_{ob}	Open Circuit Output Capacitance	2.2	4.5		2.2	4.5		pF	$I_C = 0$ $V_{CE} = -10 \text{ V}$
C_{ib}	Open Circuit Input Capacitance	4.0	8.0		4.0	8.0		pF	$I_C = 0$ $V_{BE} = -0.5 \text{ V}$
r_{bc}	Collector-Base Time Constant (f = 80 MHz)		50			50		ps	$I_C = 10 \text{ mA}$ $V_{CE} = -20 \text{ V}$
NF	Noise Figure (f = 100 MHz)	3.5	6.0		3.5	6.0		dB	$I_C = 1.0 \text{ mA}$ $V_{CE} = -5.0 \text{ V}$
NF	Noise Figure [Note 7]	2.5	4.0		2.5	4.0		dB	$R_s = 100 \Omega$ $BW = 15 \text{ MHz}$
									$I_C = 100 \mu\text{A}$ $V_{CE} = -5.0 \text{ V}$
									$R_s = 1.0 \text{ k}\Omega$

TYPICAL ELECTRICAL CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTORS

SEE 2N5003 & 2N5005 FOR PLOT CONT. INFO.

- 0 MHz (MIN) f_T
5 A AND 5.0 A
TESTING HARDWARE REQUIRED?
PACK RESISTORS
- H Y E R**
- Phoenix
264-8291
- Altamague
245-8707
- 65°C to +200°C
—65°C to +200°C
- San Jose
264-8291

I_C Collector Current

5.0 Amps

Technical drawing of a 3-lead vacuum tube pinout. The drawing shows a top view of the base with dimensions for emitter and collector leads, and a side view showing the pin dimensions and lead lengths. Labels include 'Emitter Lead No. 1', 'Collector Lead No. 3', '3 LEADS', '10-32 UNF 2A THD (COATED)', and 'Ease Lead No. 2'.

SEMI-CONDUCTOR CORP.

FAIRCHILD TRANSISTORS 2N5002 • 2N5004

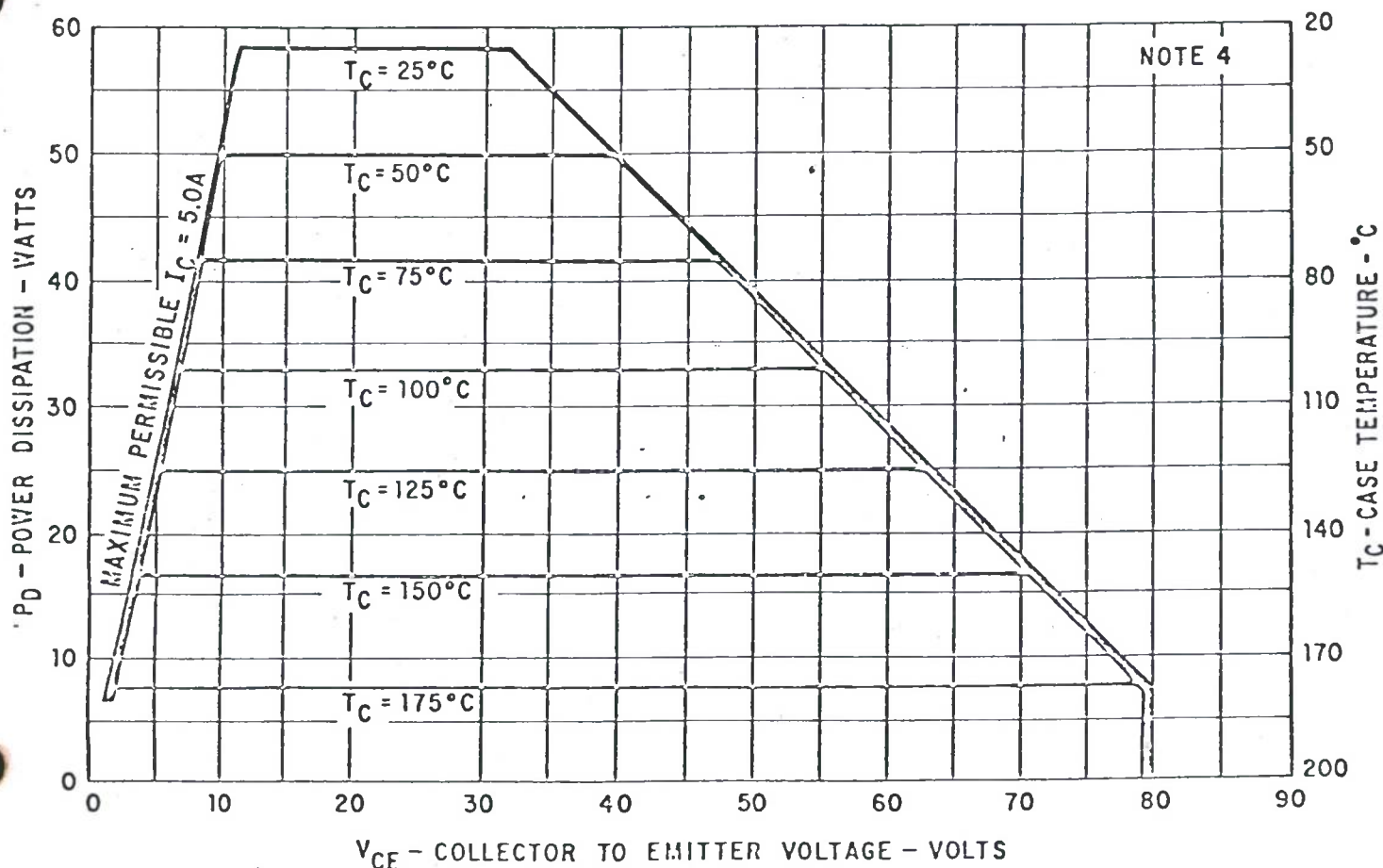
ELECTRICAL CHARACTERISTICS (25°C Case Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N5002			2N5004			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 3)	1.16	1.45		1.16	1.45		Volts	$I_C = 2.5 A$ $I_B = 0.25 A$
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 3)	1.50	2.2		1.50	2.2		Volts	$I_C = 5.0 A$ $I_B = 0.5 A$
$V_{BE(on)}$	Pulsed Base Emitter "ON" Voltage (Note 3)		1.45			1.45		Volts	$I_C = 2.5 A$ $V_{CE} = 5.0 V$
I_{CES}	Collector Cutoff Current	0.007	1.0		0.007	1.0		μA	$V_{CE} = 60 V$ $V_{BE} = 0$
I_{EBO}	Emitter Cutoff Current		1.0			1.0		μA	$I_C = 0$ $V_{EB} = 5.0 V$
$I_{CEX(150^\circ C)}$	Collector Reverse Current		500			500		μA	$V_{CE} = 60 V$ $V_{EB} = 2.0 V$
C_{cb}	Collector to Base Capacitance	90	250		90	250		pF	$I_E = 0$ $V_{CB} = 10 V$

NOTES:

- (1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
- (2) This rating refers to a high current point where collector to emitter voltage is lowest. For more information send for Fairchild Publication APP-4/2.
- (3) Pulse Conditions: length = 300 μs ; duty cycle = 1%.
- (4) Contact factory for maximum permissible power under pulsed or reverse biased operating conditions.

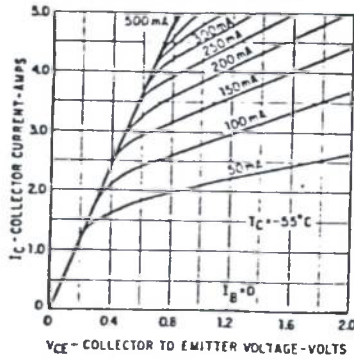
MAXIMUM PERMISSIBLE DC FORWARD BIASED POWER DISSIPATION



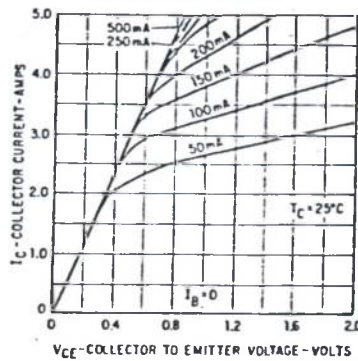
FAIRCHILD TRANSISTORS 2N5002 • 2N5004

TYPICAL ELECTRICAL CHARACTERISTICS

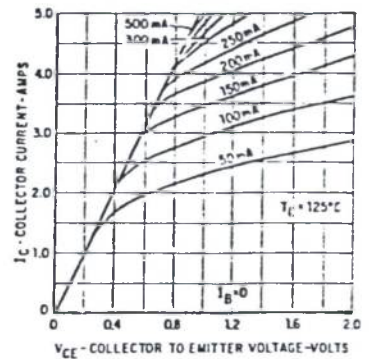
COLLECTOR CHARACTERISTICS*
SATURATION REGION



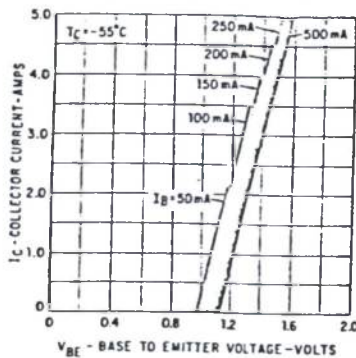
COLLECTOR CHARACTERISTICS*
SATURATION REGION



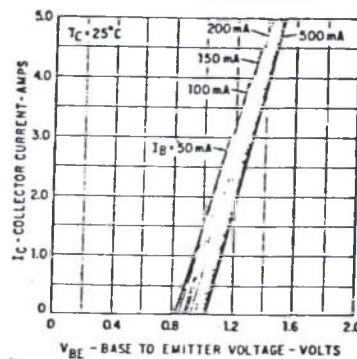
COLLECTOR CHARACTERISTICS*
SATURATION REGION



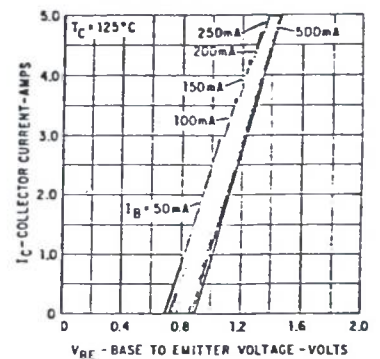
BASE CHARACTERISTICS*



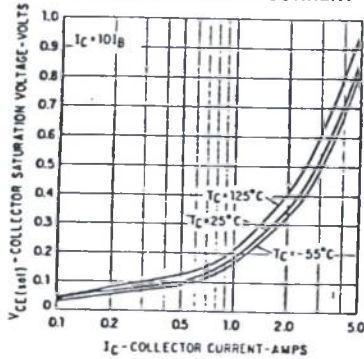
BASE CHARACTERISTICS*



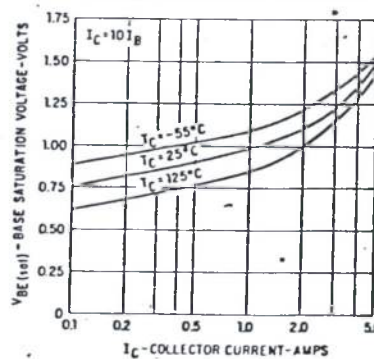
BASE CHARACTERISTICS*



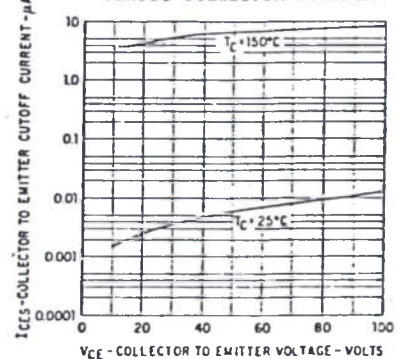
COLLECTOR SATURATION VOLTAGE
VERSUS COLLECTOR CURRENT



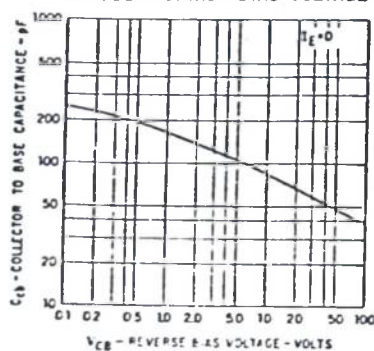
BASE SATURATION VOLTAGE
VERSUS COLLECTOR CURRENT



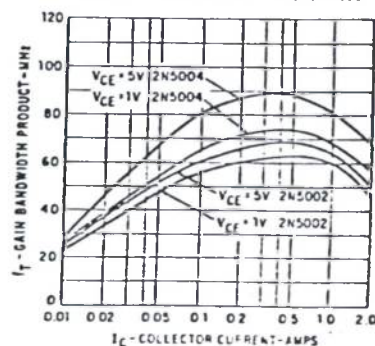
COLLECTOR CUTOFF CURRENT
VERSUS COLLECTOR VOLTAGE



COLLECTOR TO BASE CAPACITANCE
VERSUS REVERSE BIAS VOLTAGE



GAIN BANDWIDTH PRODUCT
VERSUS COLLECTOR CURRENT



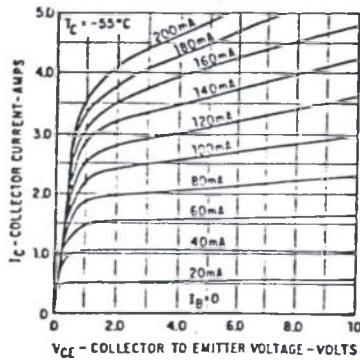
*Single Family Characteristics on Transistor Curve Tracer.

FAIRCHILD TRANSISTORS 2N5002 • 2N5004

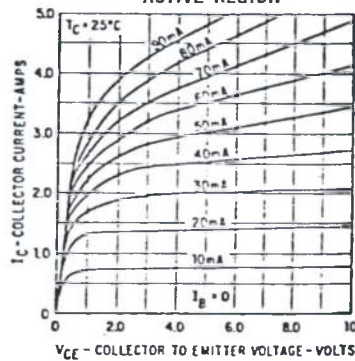
TYPICAL ELECTRICAL CHARACTERISTICS

2N5002

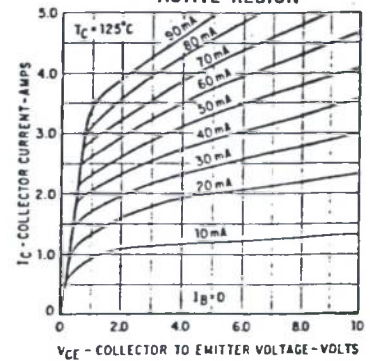
COLLECTOR CHARACTERISTICS*
ACTIVE REGION



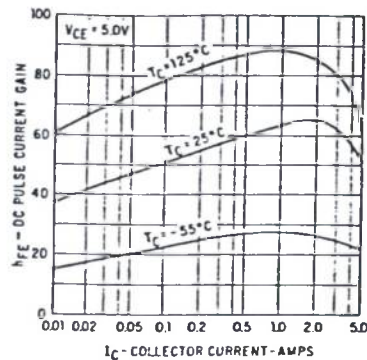
COLLECTOR CHARACTERISTICS*
ACTIVE REGION



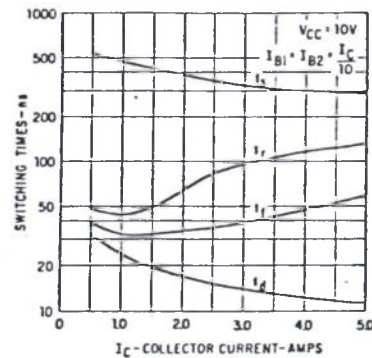
COLLECTOR CHARACTERISTICS*
ACTIVE REGION



DC PULSE CURRENT GAIN
VERSUS COLLECTOR CURRENT

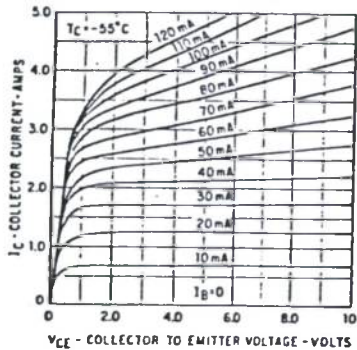


SWITCHING TIMES VERSUS
COLLECTOR CURRENT

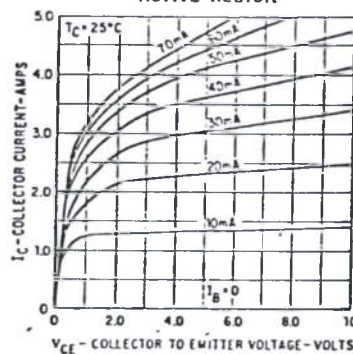


2N5004

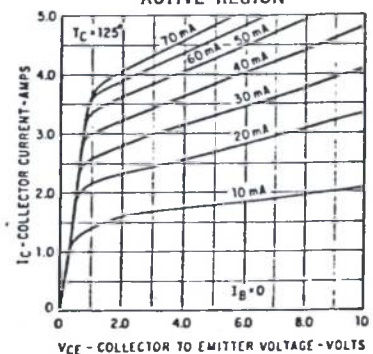
COLLECTOR CHARACTERISTICS*
ACTIVE REGION



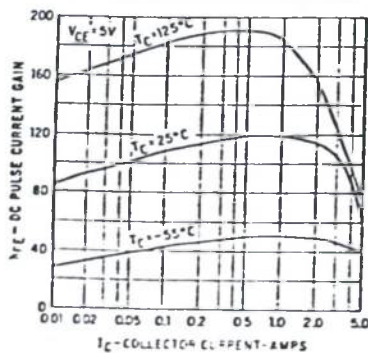
COLLECTOR CHARACTERISTICS*
ACTIVE REGION



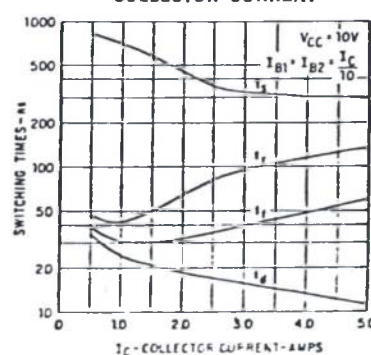
COLLECTOR CHARACTERISTICS*
ACTIVE REGION



DC PULSE CURRENT GAIN
VERSUS COLLECTOR CURRENT



SWITCHING TIMES VERSUS
COLLECTOR CURRENT



*Single Family Characteristics on Transistor Curve Tracer.

2N5003 • 2N5005

50 WATT PNP POWER TRANSISTORS

DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTORS

SEE 2N5002 • 2N5004 FOR NPN COMPLEMENT

FEATURES

- HIGH POWER -- 50 WATTS @ $T_C = 50^\circ\text{C}$, $V_{CE} = -40\text{ V}$
- HIGH VOLTAGE -- -80 V (MIN) V_{CEO}
- HIGH CURRENT SAT. VOLTAGE -- -1.5 V (MAX) $V_{CE}(\text{sat})$ @ 5.0 A
- HIGH FREQUENCY -- 60 AND 70 MHz (MIN) f_T
- BETA GUARANTEED @ 3 POINTS -- 50 mA, 2.5 A AND 5.0 A
- ISOLATED COLLECTOR PACKAGE -- NO ISOLATING HARDWARE REQUIRED
- DISCRETE EMITTER GEOMETRY WITH INTEGRATED FEEDBACK RESISTORS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

- Storage Temperature
- Operating Junction Temperature
- Lead Temperature (Soldering, 60 seconds time limit)

Maximum Power Dissipation

- Total Dissipation at 50°C Case Temperature, $V_{CE} = -40\text{ V}$
(See Maximum Permissible Power Curve and Note 4)

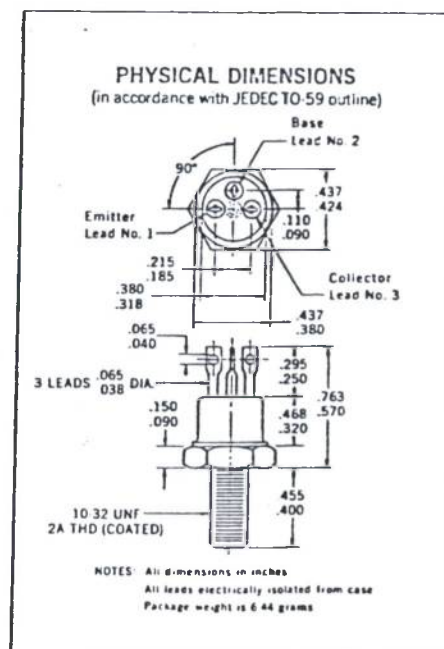
Maximum Voltages and Current

- V_{CES} Collector to Emitter Voltage
- V_{CEO} Collector to Emitter Voltage (Note 2)
- V_{EBO} Emitter to Base Voltage
- I_C Collector Current

-65°C to $+200^\circ\text{C}$
 -65°C to $+200^\circ\text{C}$
 $+300^\circ\text{C}$

50 Watts

-100 Volts
 -80 Volts
 -5.5 Volts
 5.0 Amps



ELECTRICAL CHARACTERISTICS (25°C Case Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N5003			2N5005			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
$V_{CEO}(\text{sust})$	Collector to Emitter Sustaining Voltage (Notes 2 and 3)	-80			-80			Volts	$I_C = 100\text{ mA}$, $I_B = 0$
BV_{CES}	Collector to Emitter Breakdown Voltage	-100			-100			Volts	$I_C = 1.0\text{ mA}$, $V_{BE} = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	-5.5			-5.5			Volts	$I_C = 0$, $I_E = 1.0\text{ mA}$
h_{FE}	DC Pulse Current Gain (Note 3)	20	52		50	133			$I_C = 50\text{ mA}$, $V_{CE} = -5.0\text{ V}$
h_{FE}	DC Pulse Current Gain (Note 3)	30	50	90	70	114	200		$I_C = 2.5\text{ A}$, $V_{CE} = -5.0\text{ V}$
$h_{FE}(-55^\circ\text{C})$	DC Pulse Current Gain (Note 3)	15	32		35	90			$I_C = 2.5\text{ A}$, $V_{CE} = -5.0\text{ V}$
h_{FE}	DC Pulse Current Gain (Note 3)	20	38		40	77			$I_C = 5.0\text{ A}$, $V_{CE} = -5.0\text{ V}$
h_{fe}	High Frequency Current Gain ($f = 20\text{ MHz}$)	3.0	4.05		3.5	4.85			$I_C = 0.5\text{ A}$, $V_{CE} = -5.0\text{ V}$
$V_{CE}(\text{sat})$	Pulsed Collector Saturation Voltage (Note 3)	-0.45	-0.75		-0.45	-0.75		Volts	$I_C = 2.5\text{ A}$, $I_B = 0.25\text{ A}$
$V_{CE}(\text{sat})$	Pulsed Collector Saturation Voltage (Note 3)	-0.9	-1.5		-0.9	-1.5		Volts	$I_C = 5.0\text{ A}$, $I_B = 0.5\text{ A}$

Additional Electrical Characteristics on page 2

*Planar is a patented Fairchild process.

FAIRCHILD TRANSISTORS 2N5003 • 2N5005

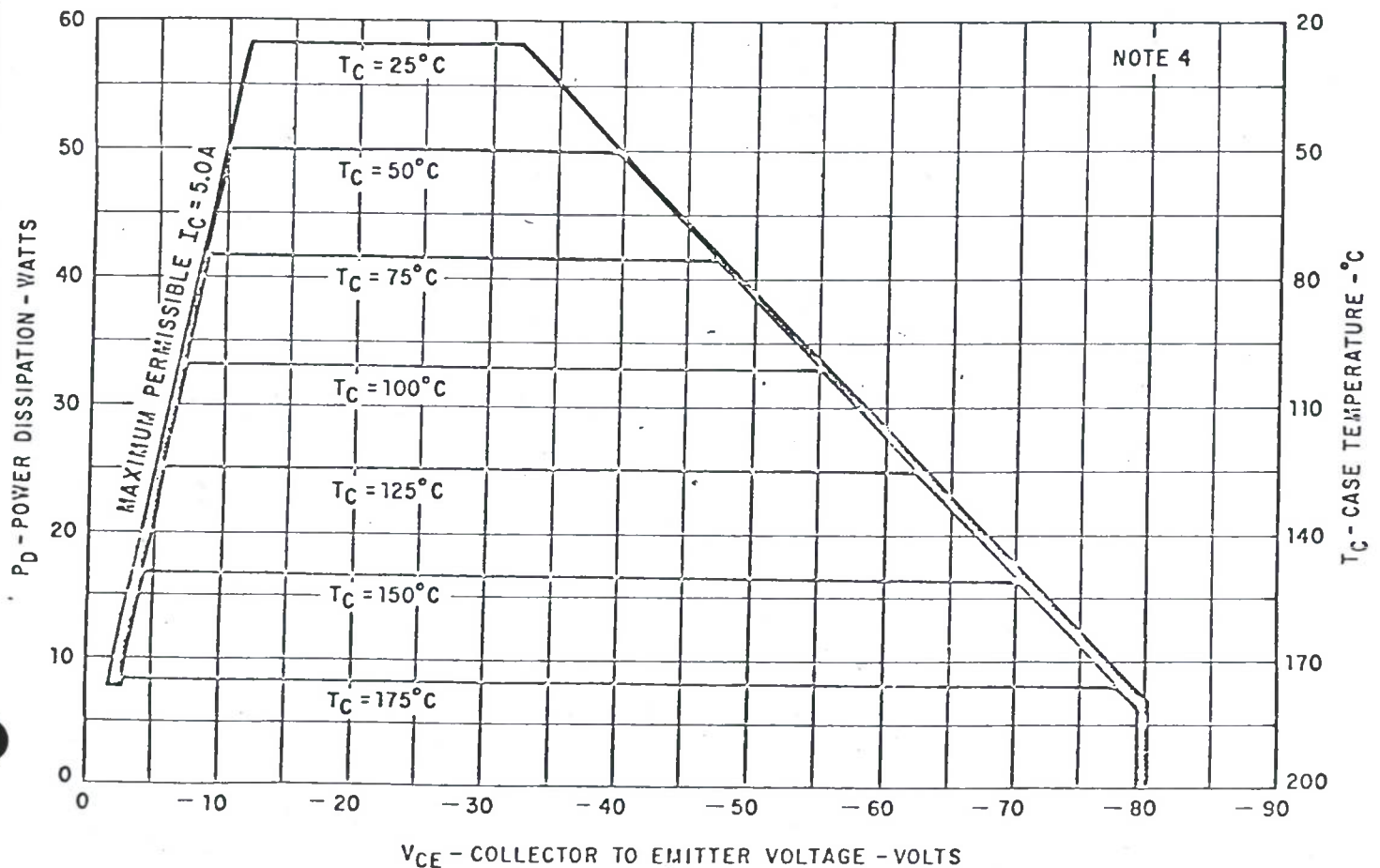
ELECTRICAL CHARACTERISTICS (25°C Case Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N5003			2N5005			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
$V_{BE}(sat)$	Pulsed Base Saturation Voltage (Note 3)	-1.1	-1.45		-1.1	-1.45		Volts	$I_C = 2.5 A$ $I_B = 0.25 A$
$V_{BE}(sat)$	Pulsed Base Saturation Voltage (Note 3)	-1.55	-2.2		-1.55	-2.2		Volts	$I_C = 5.0 A$ $I_B = 0.5 A$
$V_{BE}(on)$	Pulsed Base Emitter "ON" Voltage (Note 3)		-1.45			-1.45		Volts	$I_C = 2.5 A$ $V_{CE} = -5.0 V$
I_{CES}	Collector Cutoff Current	0.006	1.0		0.006	1.0		μA	$V_{CE} = -60 V$ $V_{BE} = 0$
I_{EBO}	Emitter Cutoff Current		1.0			1.0		μA	$I_C = 0$ $V_{BE} = 4.0 V$
$I_{CEX}(150^\circ C)$	Collector Reverse Current		500			500		μA	$V_{CE} = -60 V$ $V_{BE} = 2.0 V$
C_{cb}	Collector to Base Capacitance	170	250		170	250		pF	$I_E = 0$ $V_{CB} = -10 V$

NOTES:

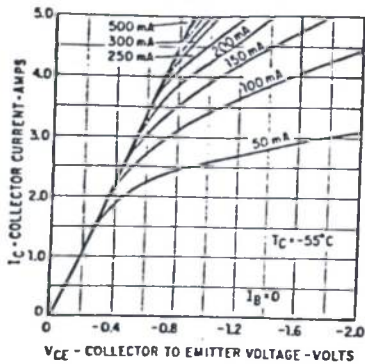
- (1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
- (2) This rating refers to a high current point where collector to emitter voltage is lowest. For more information send for Fairchild Publication APP-4/2.
- (3) Pulse Conditions: length = 300 μs ; duty cycle = 1%.
- (4) Contact factory for maximum permissible power under pulsed or reverse biased operating conditions.

MAXIMUM PERMISSIBLE DC FORWARD BIASED POWER DISSIPATION

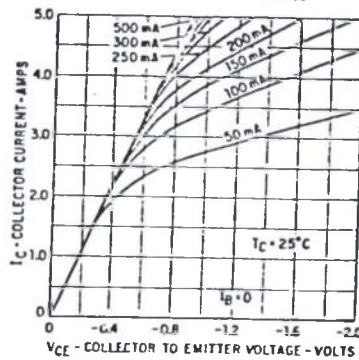


TYPICAL ELECTRICAL CHARACTERISTICS

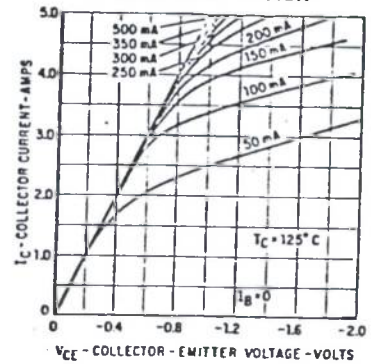
COLLECTOR CHARACTERISTICS
SATURATION REGION



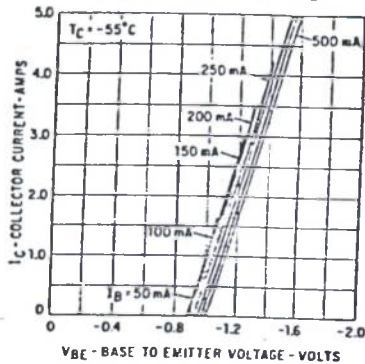
COLLECTOR CHARACTERISTICS
SATURATION REGION



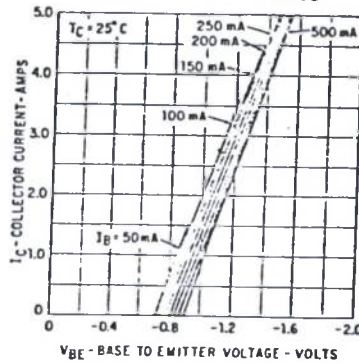
COLLECTOR CHARACTERISTICS
SATURATION REGION



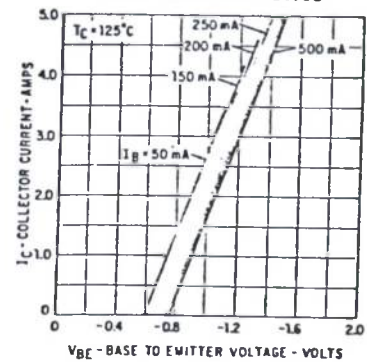
BASE CHARACTERISTICS



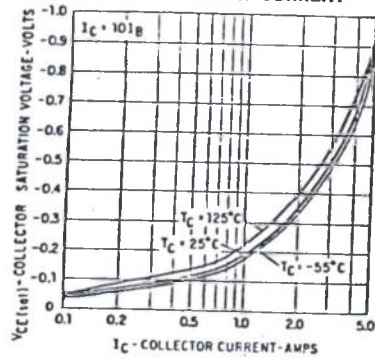
BASE CHARACTERISTICS



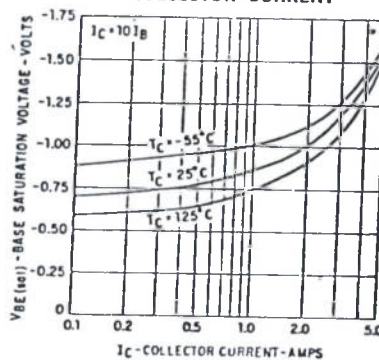
BASE CHARACTERISTICS



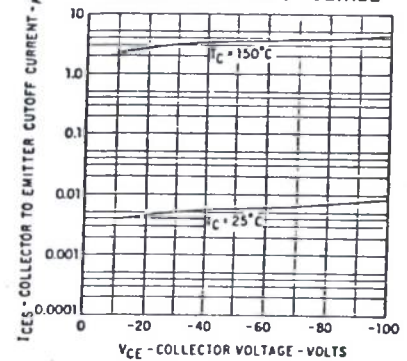
COLLECTOR SATURATION VOLTAGE
VS. COLLECTOR CURRENT



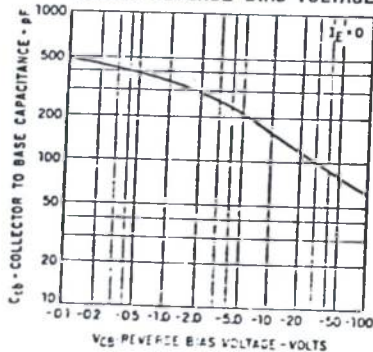
BASE SATURATION VOLTAGE VS.
COLLECTOR CURRENT



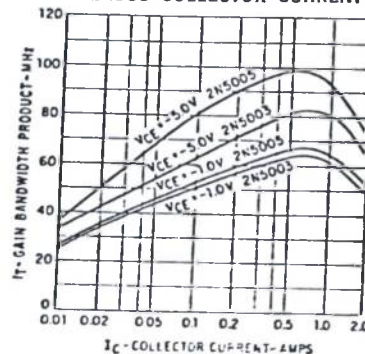
COLLECTOR CUTOFF CURRENT
VERSUS COLLECTOR VOLTAGE



COLLECTOR TO BASE CAPACITANCE
VERSUS REVERSE BIAS VOLTAGE



GAIN BANDWIDTH PRODUCT
VERSUS COLLECTOR CURRENT

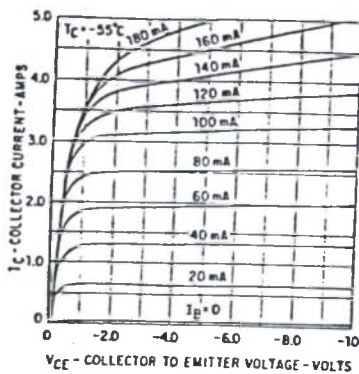


FAIRCHILD TRANSISTORS 2N5003 • 2N5005

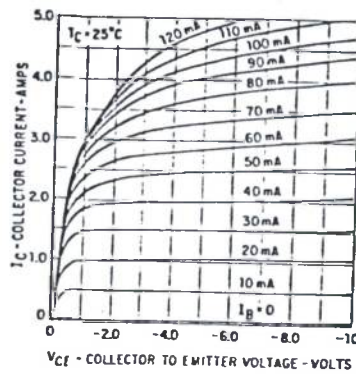
TYPICAL ELECTRICAL CHARACTERISTICS

2N5003

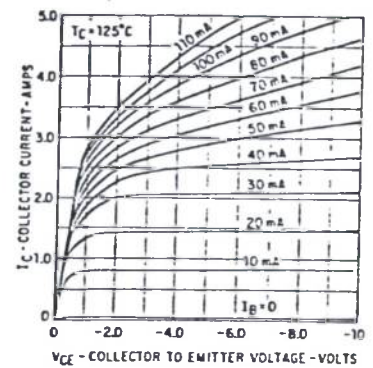
COLLECTOR CHARACTERISTICS



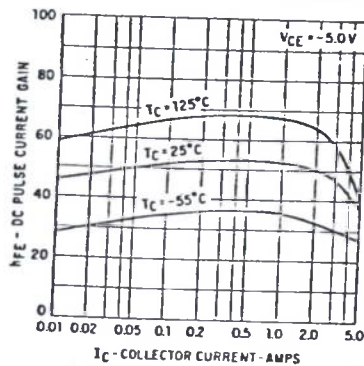
COLLECTOR CHARACTERISTICS



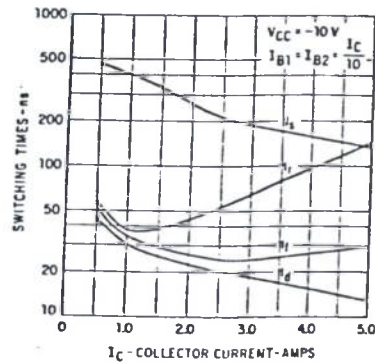
COLLECTOR CHARACTERISTICS



DC PULSE CURRENT GAIN
VERSUS COLLECTOR CURRENT

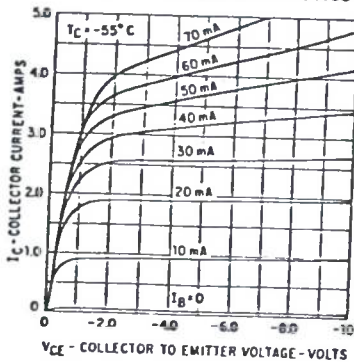


SWITCHING TIMES VERSUS
COLLECTOR CURRENT

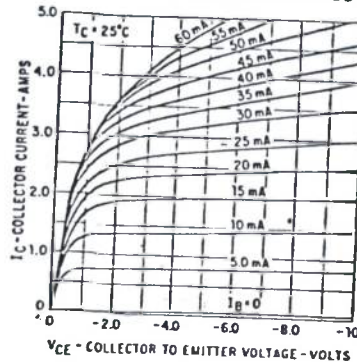


2N5005

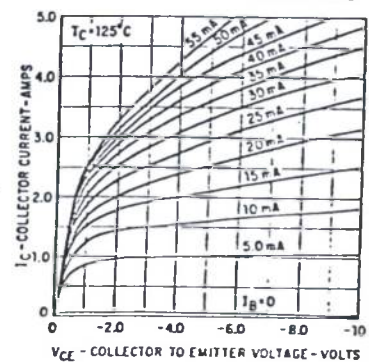
COLLECTOR CHARACTERISTICS



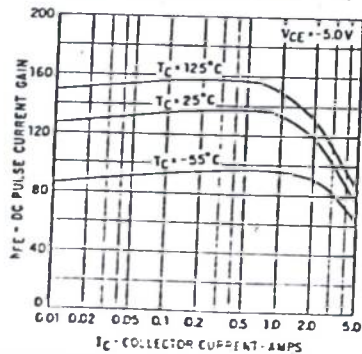
COLLECTOR CHARACTERISTICS



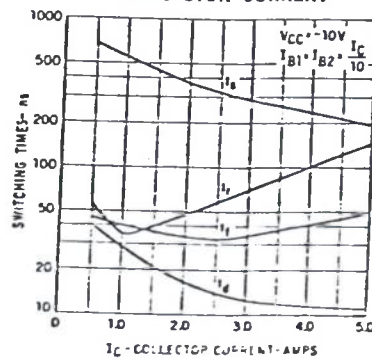
COLLECTOR CHARACTERISTICS



DC PULSE CURRENT GAIN
VERSUS COLLECTOR CURRENT



SWITCHING TIMES VERSUS
COLLECTOR CURRENT



2N5134

NPN HIGH-SPEED SATURATED SWITCH

DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTOR

- HIGH FREQUENCY CURRENT GAIN ... $f_T = 400$ MHz (MIN)
- LOW CAPACITANCE ... $C_{cb} = 4$ pF (MAX)
- LOW CHARGE STORAGE TIME ... $\tau_s = 18$ ns (MAX)
- LOW $V_{CE(sat)}$... 0.2 VOLT (MAX) AT 10 mA

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

Storage Temperature

Operating Junction Temperature

Lead Temperature (Soldering, 10 second time limit)

-55°C to +125°C

125°C Maximum

260°C Maximum

Maximum Power Dissipation

Total Dissipation at 25°C Case Temperature (Notes 2 and 3)

at 25°C Ambient Temperature

0.5 Watt

0.2 Watt

Maximum Voltages and Current

 V_{CBO} Collector to Base Voltage

20 Volts

 V_{CES} Collector to Emitter Voltage

20 Volts

 V_{CEO} Collector to Emitter Voltage

10 Volts

 V_{EBO} Emitter to Base Voltage

3.5 Volts

 I_C Collector Current (10 μ s Pulse)

500 mA

 I_C DC Collector Current

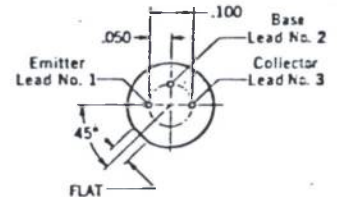
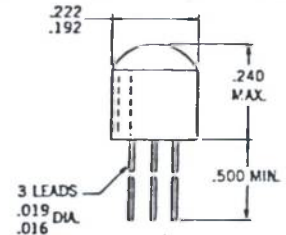
100 mA

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
h_{FE}	DC Pulse Current Gain (Note 5)	20	66	150		$I_C = 10$ mA $V_{CE} = 1.0$ V
h_{FE}	DC Pulse Current Gain (Note 5)	15	71			$I_C = 30$ mA $V_{CE} = 0.4$ V
h_{FE}	DC Pulse Current Gain (Note 5)		40			$I_C = 100$ mA $V_{CE} = 1.0$ V
$V_{BE(sat)}$	Base Saturation Voltage	0.70	0.80	0.90	Volts	$I_C = 10$ mA $I_B = 1.0$ mA
$V_{BE(sat)}$	Base Saturation Voltage	0.72	0.85	1.10	Volts	$I_C = 10$ mA $I_B = 3.3$ mA
$V_{BE(sat)}$	Base Saturation Voltage		0.90		Volts	$I_C = 30$ mA $I_B = 3.0$ mA
$V_{BE(sat)}$	Base Saturation Voltage		1.10		Volts	$I_C = 100$ mA $I_B = 10$ mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.14	0.25	Volts	$I_C = 10$ mA $I_B = 1.0$ mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.12	0.20	Volts	$I_C = 10$ mA $I_B = 3.3$ mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.17		Volts	$I_C = 30$ mA $I_B = 3.0$ mA
$V_{CE(sat)} (+65^\circ\text{C})$	Collector Saturation Voltage		0.19		Volts	$I_C = 10$ mA $I_B = 1.0$ mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.28		Volts	$I_C = 100$ mA $I_B = 10$ mA
h_{fe}	High Frequency Current Gain ($f = 100$ MHz)	2.5	5.75			$I_C = 10$ mA $V_{CE} = 10$ V
C_{cb}	Collector-Base Capacitance		2.3	4.0	pF	$I_E = 0$ $V_{CB} = 5.0$ V
I_{CES}	Collector Reverse Current		0.05	0.40	μ A	$V_{CE} = 15$ V $V_{BE} = 0$
$I_{CBO}(65^\circ\text{C})$	Collector Cutoff Current		1.0	10	μ A	$I_E = 0$ $V_{CB} = 15$ V
BV_{CES}	Collector to Emitter Breakdown Voltage	20			Volts	$I_C = 10$ μ A $V_{BE} = 0$
BV_{CBO}	Collector to Base Breakdown Voltage	20			Volts	$I_C = 10$ μ A $I_E = 0$
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage (Notes 4 and 5)	10			Volts	$I_C = 10$ mA (pulsed) $I_B = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	3.5			Volts	$I_C = 0$ $I_E = 10$ μ A
τ_s	Charge Storage Time Constant (Note 6)		7.0	18	ns	$I_C = I_{B1} \approx 10$ mA, $I_{B2} \approx -10$ mA
t_{on}	Turn On Time (Note 6)		8.0	18	ns	$I_C \approx 10$ mA, $I_{B1} \approx 3.3$ mA
t_{off}	Turn Off Time (Note 6)		7.0	18	ns	$I_C \approx 10$ mA, $I_{B1} \approx 3.3$ mA, $I_{B2} \approx -3.3$ mA

PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-106) outline



NOTES: All dimensions in inches
All leads electrically isolated from case
Package weight is 0.31 gram. Package
is electrically non-conductive material

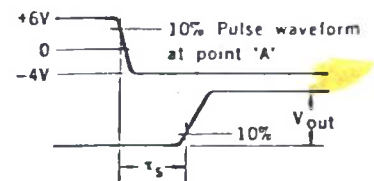
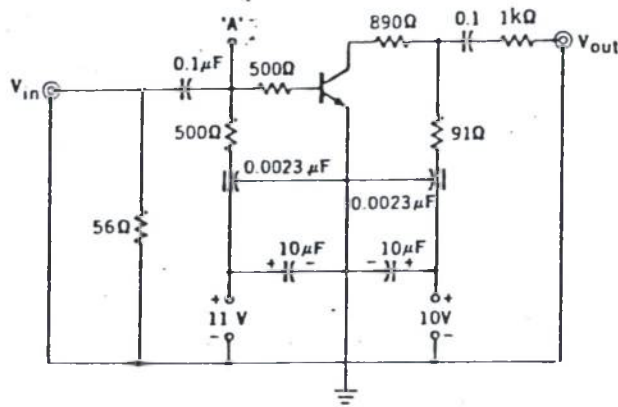
*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

CHARGE STORAGE TIME MEASUREMENT CIRCUIT

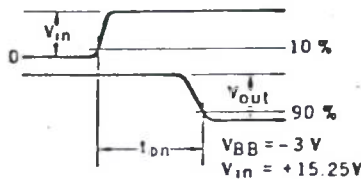


Pulse Generator
 V_{in} Rise Time < 1 ns
 Source Impedance = 50Ω
 PW ≥ 300 ns
 Duty Cycle $< 2\%$

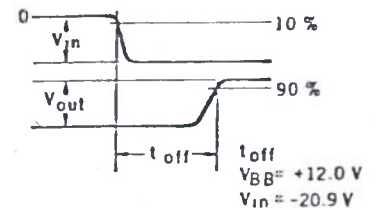
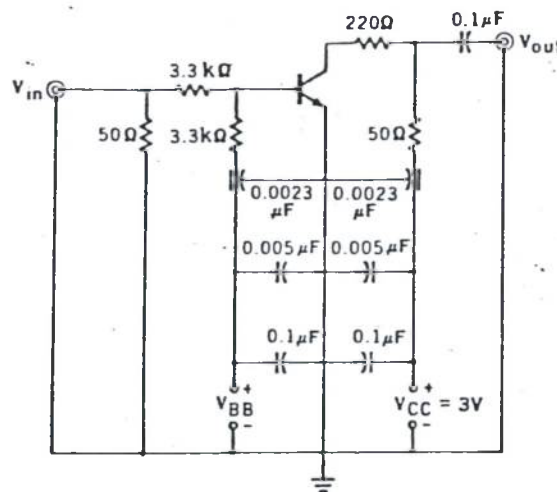


To Sampling Oscilloscope
 Input Impedance = 50Ω
 Rise Time ≤ 1 ns

$t_{ON} - t_{OFF}$ MEASUREMENT CIRCUIT

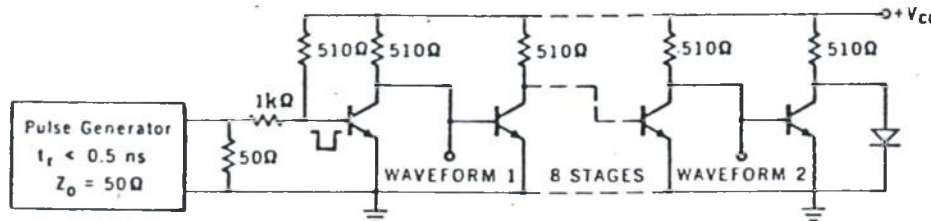


Pulse Generator
 V_{in} Rise Time < 1 ns
 Source Impedance = 50Ω
 PW ≥ 300 ns
 Duty Cycle $< 2\%$



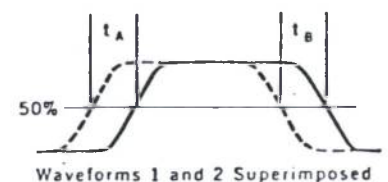
To Sampling Oscilloscope
 Input Impedance = 50Ω
 Rise Time ≤ 1 ns

CIRCUIT FOR MEASUREMENT OF PROPAGATION DELAY



$$\bar{t}_{pd} = \frac{t_A + t_B}{20}$$

$\bar{t}_{pd}$ = Average Propagation per Transistor



NOTES:

- (1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
- (2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.
- (3) These ratings give a maximum junction temperature of 125°C and junction to case thermal resistance of $200^{\circ}\text{C}/\text{Watt}$ (derating factor of $5.0 \text{ mW}/^{\circ}\text{C}$). Junction to ambient thermal resistance of $500^{\circ}\text{C}/\text{Watt}$ (derating factor of $2.0 \text{ mW}/^{\circ}\text{C}$).
- (4) Rating refers to a high-current point where collector to emitter voltage is lowest.
- (5) Pulse Conditions: length = $300 \mu\text{s}$; duty cycle = 1% .
- (6) See switching circuits for exact value of I_C , I_{B1} , and I_{B2} .

PNP HIGH-SPEED SWITCH AND RF AMPLIFIER

DIFFUSED SILICON PLANAR* EPITAXIAL TRANSISTOR

- HIGH BETA $h_{FE} = 150$ (TYP) AT 10 mA
- HIGH FREQUENCY . . . $f_T = 500$ MHz (TYP) AT 10 mA
- LOW CAPACITANCE . . . $C_{cb} = 2.2$ pF (TYP)
- HIGH VOLTAGE $V_{CEO} = 20$ VOLTS (MIN)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

Storage Temperature

Operating Junction Temperature

Lead Temperature (Soldering, 10 second time limit)

−55°C to +125°C

+125°C Maximum

+260°C Maximum

Maximum Power Dissipation (Notes 2 and 3)

Total Dissipation at 25°C Case Temperature

at 25°C Ambient Temperature

0.5 Watt

0.2 Watt

Maximum Voltages and Current

V_{CBO} Collector to Base Voltage

−20 Volts

V_{CEO} Collector to Emitter Voltage (Note 4)

−20 Volts

V_{EBO} Emitter to Base Voltage

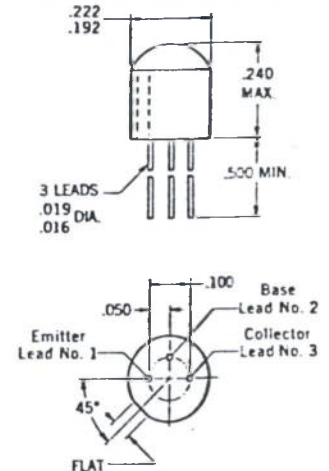
−5.0 Volts

I_C Collector Current

100 mA

PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-18) outline



NOTES: All dimensions in inches
All leads electrically isolated from case
Package weight is 0.31 gram. Package
is electrically non-conductive material

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
h_{FE}	DC Current Gain	30	70			$I_C = 100 \mu A$ $V_{CE} = -10 V$
h_{FE}	DC Current Gain	40	100			$I_C = 1.0 mA$ $V_{CE} = -10 V$
h_{FE}	DC Pulse Current Gain (Note 5)	40	150			$I_C = 10 mA$ $V_{CE} = -1.0 V$
h_{FE}	DC Pulse Current Gain (Note 5)	15	30			$I_C = 50 mA$ $V_{CE} = -10 V$
$V_{CE(sat)}$	Collector Saturation Voltage			−0.15	Volts	$I_C = 1.0 mA$ $I_B = 0.1 mA$
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 5)			−0.20	Volts	$I_C = 10 mA$ $I_B = 1.0 mA$
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 5)		−0.2	−0.5	Volts	$I_C = 50 mA$ $I_B = 5.0 mA$
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 5)	−0.7	−0.77	−1.0	Volts	$I_C = 10 mA$ $I_B = 1.0 mA$
$V_{BE(sat)}$	Pulsed Base Saturation Voltage (Note 5)		−0.75	−1.25	Volts	$I_C = 50 mA$ $I_B = 5.0 mA$
t_{on}	Turn On Time (Note 6)			50	ns	$I_C \approx 50 mA$ $I_{B1} \approx 5.0 mA$
t_{off}	Turn Off Time (Note 6)			200	ns	$I_C \approx 50 mA$ $I_{B1} \approx 5.0 mA$
h_{fe}	High Frequency Current Gain ($f = 100$ MHz)	3.0	5.0			$I_C = 10 mA$ $V_{CE} = -20 V$

Additional Electrical Characteristics on page 2

*Planar is a patented Fairchild process.

NOTES:

- (1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
- (2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.
- (3) These ratings give a maximum junction temperature of 125°C and junction to case thermal resistance of 200°C/Watt (derating factor of 5.0 mW/°C); junction to ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).
- (4) Rating refers to a high-current point where collector to emitter voltage is lowest. For more information send for Fairchild Publication APP-4/2.
- (5) Pulse Conditions: length = 300 μs ; duty cycle = 1%.
- (6) See switching circuit for exact values of I_C , I_{B1} , and I_{B2} .

NOTES:

- (1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
- (2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.
- (3) These ratings give a maximum junction temperature of 125°C and junction to case thermal resistance of $200^{\circ}\text{C}/\text{Watt}$ (derating factor of $5.0\text{ mW}/^{\circ}\text{C}$); junction to ambient thermal resistance of $500^{\circ}\text{C}/\text{Watt}$ (derating factor of $2.0\text{ mW}/^{\circ}\text{C}$).
- (4) This rating refers to a high-current point where collector to emitter voltage is lowest.
- (5) Pulse Conditions: length = $300\text{ }\mu\text{s}$; duty cycle = 1%.
- (6) $R_s = 10\text{ k}\Omega$, Power Bandwidth of 150 Hz.
- (7) $R_s = 10\text{ k}\Omega$, Power Bandwidth of 15.7 kHz with 3.0 dB points at 10 Hz and 10 kHz.
- (8) $R_s = 1.0\text{ k}\Omega$, Power Bandwidth of 150 Hz.

MPS-U55
MPS-U56

PNP SILICON ANNULAR* AMPLIFIER TRANSISTORS

... designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage —
 $BV_{CEO} = 60 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc} - \text{MPS-U55}$
 $80 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc} - \text{MPS-U56}$
- High Power Dissipation — $P_D = 5.0 \text{ W @ } T_C = 25^\circ\text{C}$
- Complements to MPS-U05 and MPS-U06

PNP SILICON ANNULAR* AMPLIFIER TRANSISTORS

MAY 1969 — DS 5327

NEW ADDRESS & PHONE

HAMILTON ELECTRO SALES

1400 West 46th Ave./DENVER, COLORADO 80216

PHONE: (303) 433-8551/TWX: 910-931-0580

EFFECTIVE APRIL 1st, 1969

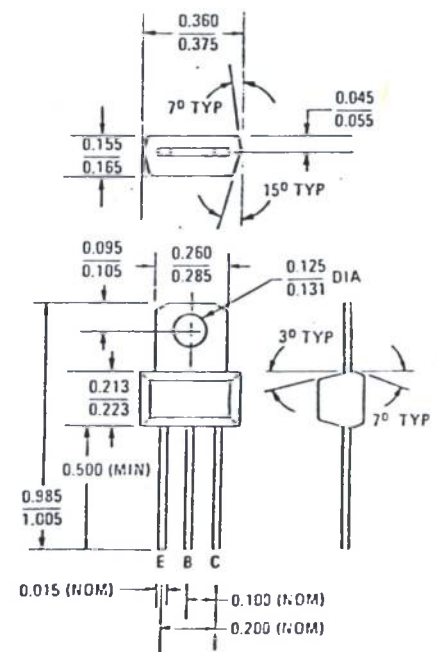


MAXIMUM RATINGS

Rating	Symbol	MPS-U55	MPS-U56	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	4.0		Vdc
Collector Current — Continuous	I_C	1.0		Adc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 9.10		Watt mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	5.0 45.4		Watt mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +135		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	22	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	θ_{JA}	110	$^\circ\text{C/W}$



Collector connected
to tab
CASE 152

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage ($I_C = 1.0 \text{ mAdc}$, $I_B = 0$)	MPS-U05 MPS-U06	BV_{CEO}	60 80	—	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100 \mu\text{Adc}$, $I_C = 0$)		BV_{EBO}	4.0	—	—	Vdc
Collector Cutoff Current ($V_{CB} = 40 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 60 \text{ Vdc}$, $I_E = 0$)	MPS-U05 MPS-U06	I_{CBO}	— —	— —	100 100	nAdc

ON CHARACTERISTICS

DC Current Gain ($I_C = 50 \text{ mAdc}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 250 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 250 \text{ mAdc}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 500 \text{ mAdc}$, $V_{CE} = 5.0 \text{ Vdc}$)	h_{FE}	100 — 50 —	180 125 170 100	— — — —	—
Collector-Emitter Saturation Voltage ($I_C = 250 \text{ mAdc}$, $I_B = 10 \text{ mAdc}$) ($I_C = 250 \text{ mAdc}$, $I_B = 25 \text{ mAdc}$)	$V_{CE(sat)}$	— —	0.25 0.1	0.6 —	Vdc
Base-Emitter Saturation Voltage ($I_C = 250 \text{ mAdc}$, $I_B = 25 \text{ mAdc}$)	$V_{BE(sat)}$	—	0.83	—	Vdc
Base-Emitter On Voltage ($I_C = 250 \text{ mAdc}$, $V_{CE} = 5.0 \text{ Vdc}$)	$V_{BE(on)}$	—	0.75	1.2	Vdc

SMALL-SIGNAL CHARACTERISTICS

Current-Gain-Bandwidth Product ($I_C = 250 \text{ mAdc}$, $V_{CE} = 5.0 \text{ Vdc}$, $f = 100 \text{ MHz}$)	f_T	50	150	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 100 \text{ kHz}$)	C_{ob}	—	6.0	12	pF
Input Capacitance ($V_{BE} = 0.5 \text{ Vdc}$, $I_C = 0$, $f = 100 \text{ kHz}$)	C_{ib}	—	14	—	pF

FIGURE 1 — TYPICAL DC CURRENT GAIN

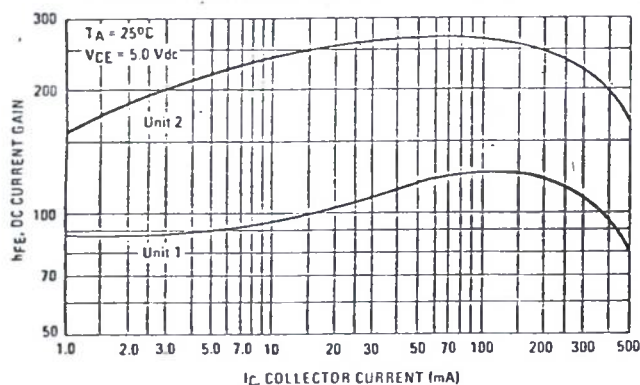


FIGURE 2 — "SATURATION" AND "ON" VOLTAGES

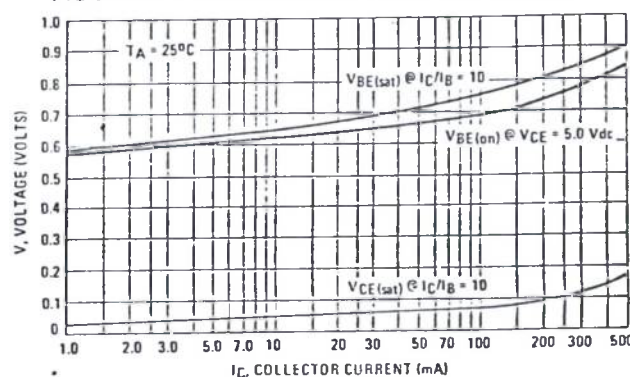
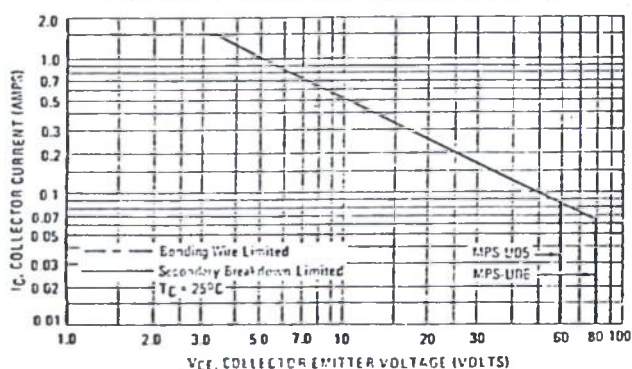


FIGURE 3 — DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 135^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.



MOTOROLA Semiconductor Products Inc.

BOX 20912 • PHOENIX, ARIZONA 85036 • A SUBSIDIARY OF MOTOROLA INC.

MPS-U05
MPS-U06

NPN SILICON ANNULAR* AMPLIFIER TRANSISTORS

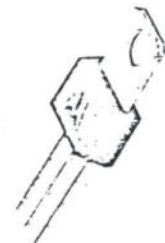
... designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage –
BVCEO = 60 Vdc (Min) @ IC = 1.0 mAdc – MPS-U05
80 Vdc (Min) @ IC = 1.0 mAdc – MPS-U06
- High Power Dissipation – PD = 5.0 W @ TC = 25°C
- Complements to MPS-U55 and MPS-U56

NEW ADDRESS & PHONE HAMILTON ELECTRO SALES

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MAY 1969 – DS 5326

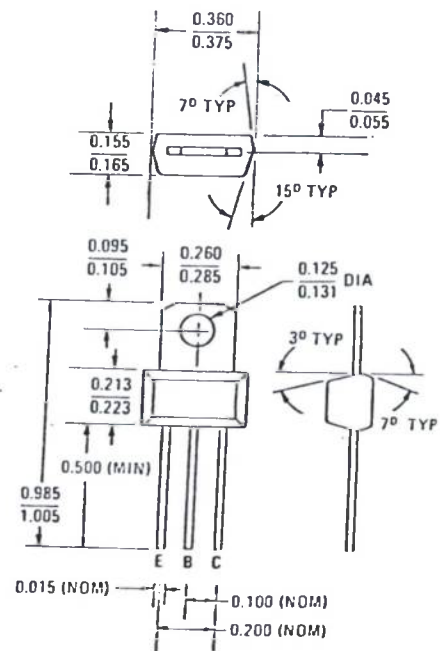


MAXIMUM RATINGS

Rating	Symbol	MPS-U05	MPS-U06	Unit
Collector-Emitter Voltage	VCEO	60	80	Vdc
Collector-Base Voltage	VCB	60	80	Vdc
Emitter-Base Voltage	VEB	4.0		Vdc
Collector Current – Continuous	IC	1.0		Adc
Total Device Dissipation @ TA = 25°C Derate above 25°C	PD	1.0	9.10	Watt mW/°C
Total Device Dissipation @ TC = 25°C Derate above 25°C	PD	5.0	45.4	Watts mW/°C
Operating and Storage Junction Temperature Range	TJ, Tstg	-55 to +135		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θJC	22	°C/W
Thermal Resistance, Junction to Ambient	θJA	110	°C/W



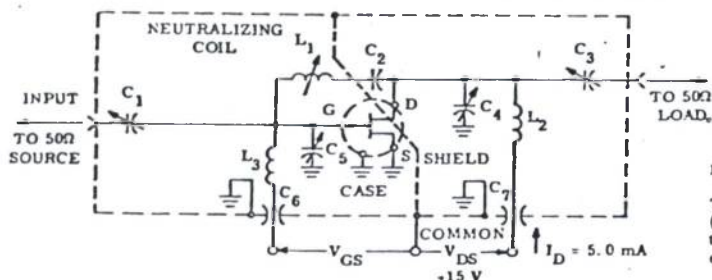
Collector connected
to tab

CASE 152

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
SMALL-SIGNAL CHARACTERISTICS					
Forward Transadmittance ($V_{DS} = 15 \text{ Vdc}$, $V_{GS} = 0$, $f = 1.0 \text{ kHz}$)	$ y_{fs} $	3000	-	6000	μmhos
2N5484		3500	-	7000	
2N5485		4000	-	8000	
2N5486					
Forward Transconductance ($V_{DS} = 15 \text{ Vdc}$, $V_{GS} = 0$, $f = 100 \text{ MHz}$) ($V_{DS} = 15 \text{ Vdc}$, $V_{GS} = 0$, $f = 400 \text{ MHz}$)	$\text{Re}(y_{fs})$	2500	-	-	μmhos
2N5484		3000	-	-	
2N5485		3500	-	-	
2N5486					
Output Admittance ($V_{DS} = 15 \text{ Vdc}$, $V_{GS} = 0$, $f = 1.0 \text{ kHz}$)	$ y_{os} $	-	-	50	μmhos
2N5484		-	-	60	
2N5485		-	-	75	
2N5486		-	-		
Output Conductance ($V_{DS} = 15 \text{ Vdc}$, $V_{GS} = 0$, $f = 100 \text{ MHz}$) ($V_{DS} = 15 \text{ Vdc}$, $V_{GS} = 0$, $f = 400 \text{ MHz}$)	$\text{Re}(y_{os})$	-	-	75	μmhos
2N5484		-	-	100	
2N5485, 2N5486		-	-		
Input Conductance ($V_{DS} = 15 \text{ Vdc}$, $V_{GS} = 0$, $f = 100 \text{ MHz}$) ($V_{DS} = 15 \text{ Vdc}$, $V_{GS} = 0$, $f = 400 \text{ MHz}$)	$\text{Re}(y_{is})$	-	-	100	μmhos
2N5484		-	-	1000	
2N5485, 2N5486		-	-		
Input Capacitance ($V_{DS} = 15 \text{ Vdc}$, $V_{GS} = 0$, $f = 1.0 \text{ MHz}$)	C_{iss}	-	-	5.0	pF
Reverse Transfer Capacitance ($V_{DS} = 15 \text{ Vdc}$, $V_{GS} = 0$, $f = 1.0 \text{ MHz}$)	C_{rss}	-	-	1.0	pF
Output Capacitance ($V_{DS} = 15 \text{ Vdc}$, $V_{GS} = 0$, $f = 1.0 \text{ MHz}$)	C_{oss}	-	-	2.0	pF
Common-Source Noise Figure ($V_{DS} = 15 \text{ Vdc}$, $V_{GS} = 0$, $R_G = 1.0 \text{ Megohm}$, $f = 1.0 \text{ kHz}$)	NF	-	-	2.5	dB
All Types		-	-		
($V_{DS} = 15 \text{ Vdc}$, $I_D = 1.0 \text{ mAdc}$, $R_G = 1.0 \text{ k ohm}$, $f = 100 \text{ MHz}$)		-	-	3.0	
2N5484		-	-		
($V_{DS} = 15 \text{ Vdc}$, $I_D = 1.0 \text{ mAdc}$, $R_G = 1.0 \text{ k ohm}$, $f = 200 \text{ MHz}$)		-	4.0	-	
2N5484		-			
($V_{DS} = 15 \text{ Vdc}$, $I_D = 4.0 \text{ mAdc}$, $R_G = 1.0 \text{ k ohm}$, $f = 100 \text{ MHz}$)		-	-	2.0	
2N5485, 2N5486		-	-		
($V_{DS} = 15 \text{ Vdc}$, $I_D = 4.0 \text{ mAdc}$, $R_G = 1.0 \text{ k ohm}$, $f = 400 \text{ MHz}$)		-	-	4.0	
2N5485, 2N5486		-	-		
Insertion Power Gain ($V_{DS} = 15 \text{ Vdc}$, $I_D = 1.0 \text{ mAdc}$, $f = 100 \text{ MHz}$) ($V_{DS} = 15 \text{ Vdc}$, $I_D = 1.0 \text{ mAdc}$, $f = 200 \text{ MHz}$) ($V_{DS} = 15 \text{ Vdc}$, $I_D = 4.0 \text{ mAdc}$, $f = 100 \text{ MHz}$) ($V_{DS} = 15 \text{ Vdc}$, $I_D = 4.0 \text{ mAdc}$, $f = 400 \text{ MHz}$)	G_{ps}	16	-	25	dB
2N5484		-	14	-	
2N5484		-		-	
2N5485, 2N5486		18	-	30	
2N5485, 2N5486		10	-	20	

FIGURE 1 - 100 MHz & 400 MHz NEUTRALIZED AMPLIFIER



NOTE:

The noise source is a hot-cold body (A1L type 70 or equivalent) with a test receiver (A1L type 136 or equivalent).

ADJUST V_{GS} FOR

$I_D = 5.0 \text{ mA}$

$V_{GS} < 0 \text{ VOLTS}$

- * L_1 17 turns (approximately - depending upon circuit layout), AWG #28 enameled copper wire, close wound on 9/32" ceramic coil form. Tuning provided by a powdered iron slug.
- L_2 4 1/2 turns, AWG #18 enameled copper wire, 5/16" long, 3/8" I. D. (AIR CORE).
- L_3 3 1/2 turns, AWG #18 enameled copper wire, 1/4" long, 3/8" I. D. (AIR CORE).

- ** L_1 6 turns (approximately - depending upon circuit layout), AWG #24 enameled copper wire, close wound on 7/32" ceramic coil form. Tuning provided by an aluminum slug.
- L_2 1 turn, AWG #10 enameled copper wire, 3/8" I. D. (AIR CORE).
- L_3 1/2 turn, AWG #10 enameled copper wire, 1/4" I. D. (AIR CORE).

Reference Designation	VALUE	
	100 MHz	400 MHz
C_1	1-12 pF	0.8-8.0 pF
C_2	1000 pF	27 pF
C_3	1-12 pF	0.8-8.0 pF
C_4	1-12 pF	0.8-8.0 pF
C_5	1-12 pF	0.8-8.0 pF
C_6	0.0015 μF	0.001 μF
C_7	0.0015 μF	0.001 μF
L_1	3.0 μH^*	0.2 μH^{**}
L_2	0.25 μH^*	0.03 μH^{**}
L_3	0.14 μH^*	0.022 μH^{**}

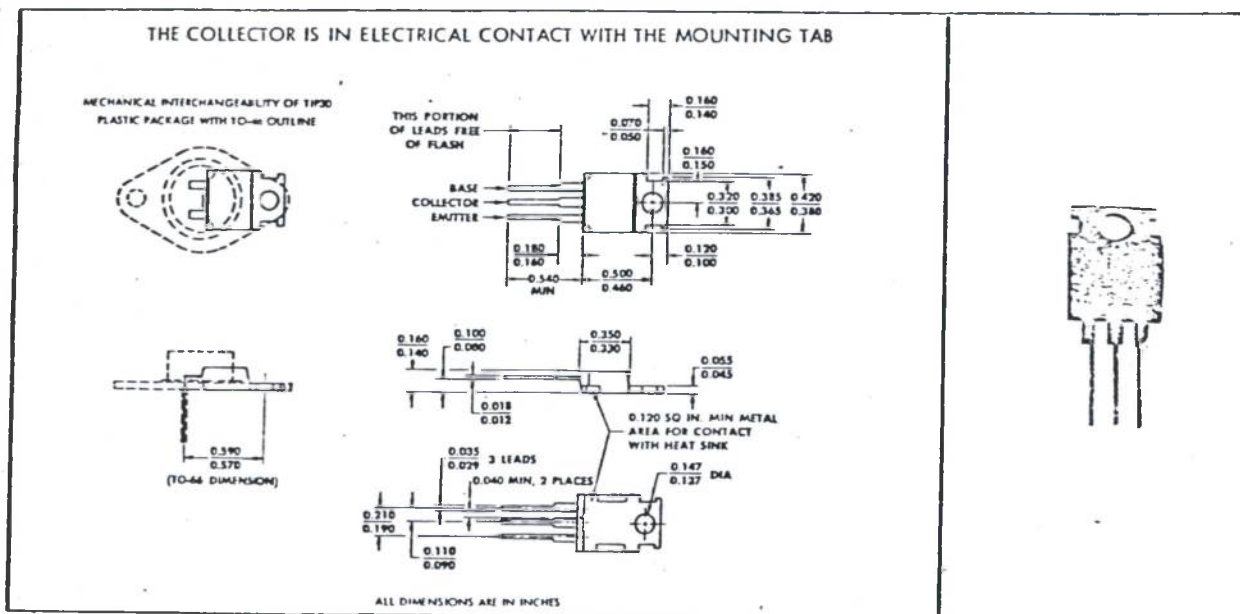


MOTOROLA Semiconductor Products Inc.

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH TIP29, TIP29A

- 30 Watts at 25°C Case Temperature
- 1 A Rated Collector Current
- Min f_T of 3 MHz at 10 V, 200 mA

mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP30	TIP30A
Collector-Base Voltage	-40 V	-60 V
Collector-Emitter Voltage (See Note 1)	-40 V	-60 V
Emitter-Base Voltage	← -5 V →	
Continuous Collector Current	← -1 A →	
Continuous Base Current	← -0.4 A →	
Safe Operating Region at (or below) 25°C Case Temperature	See Figure 2	
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 2)	← 30 W →	
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	← 2 W →	
Operating Collector Junction Temperature Range	-65°C to 150°C	
Storage Temperature Range	-65°C to 150°C	
Lead Temperature 1/8 Inch from Case for 10 Seconds	← 260°C →	

NOTES: 1. These values apply when the base-emitter diode is open-circuited.
2. Derate linearly to 150°C case temperature at the rate of 0.24 W/deg.
3. Derate linearly to 150°C free-air temperature at the rate of 16 mW/deg.



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5017 • DALLAS, TEXAS 75222

P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP30		TIP30A		UNIT
		MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 4	-40		-60		V
I_{CEO} Collector Cutoff Current	$V_{CE} = -30 \text{ V}$, $I_B = 0$	-0.3		-0.3		mA
I_{CES} Collector Cutoff Current	$V_{CE} = -40 \text{ V}$, $V_{BE} = 0$	-0.2				mA
	$V_{CE} = -60 \text{ V}$, $V_{BE} = 0$			-0.2		
I_{EBO} Emitter Cutoff Current	$V_{EB} = -5 \text{ V}$, $I_C = 0$	-1		-1		mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -0.2 \text{ A}$, See Notes 4 and 5	40	200	40	200	
	$V_{CE} = -4 \text{ V}$, $I_C = -1 \text{ A}$, See Notes 4 and 5	10		10		
V_{BE} Base-Emitter Voltage	$V_{CE} = -4 \text{ V}$, $I_C = -1 \text{ A}$, See Notes 4 and 5	-1.3		-1.3		V
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -125 \text{ mA}$, $I_C = -1 \text{ A}$, See Notes 4 and 5	-0.7		-0.7		V
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -0.2 \text{ A}$, $f = 1 \text{ kHz}$	20		20		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -0.2 \text{ A}$, $f = 1 \text{ MHz}$	3		3		

NOTES: 4. These parameters must be measured using pulse techniques. $t_p \leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

Pulse width must be such that halving or doubling does not cause a change greater than the required accuracy of the measurement.

5. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER	MAX	UNIT
θ_{J-C} Junction-to-Case Thermal Resistance	4.17	deg/W
θ_{J-A} Junction-to-Free-Air Thermal Resistance	62.5	

switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = -200 \text{ mA}$, $I_{B(1)} = -20 \text{ mA}$, $I_{B(2)} = 20 \text{ mA}$, $V_{BE(off)} = 3.4 \text{ V}$, $R_L = 150 \Omega$, See Figure 1	0.25	μs
t_{off} Turn-Off Time		0.90	

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.



P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

PARAMETER MEASUREMENT INFORMATION

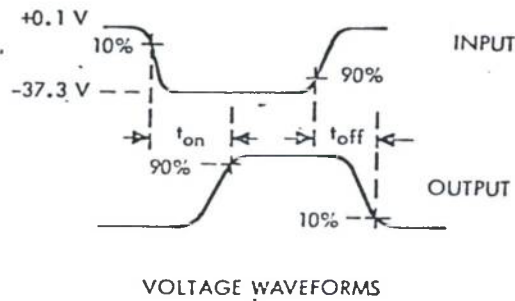
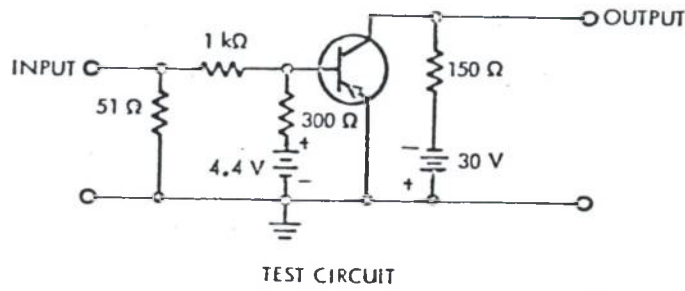


FIGURE 1

- NOTES:
- a. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 15 \text{ ns}$, $t_f \leq 15 \text{ ns}$, $Z_{out} = 50 \Omega$, $t_p = 10 \mu\text{s}$, duty cycle $\leq 2\%$.
 - b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15 \text{ ns}$, $R_{in} \geq 10 \text{ M}\Omega$, $C_{in} \leq 11.5 \text{ pF}$.
 - c. Resistors must be noninductive types.
 - d. The d-c power supplies may require additional bypassing in order to minimize ringing.

MAXIMUM SAFE OPERATING REGION

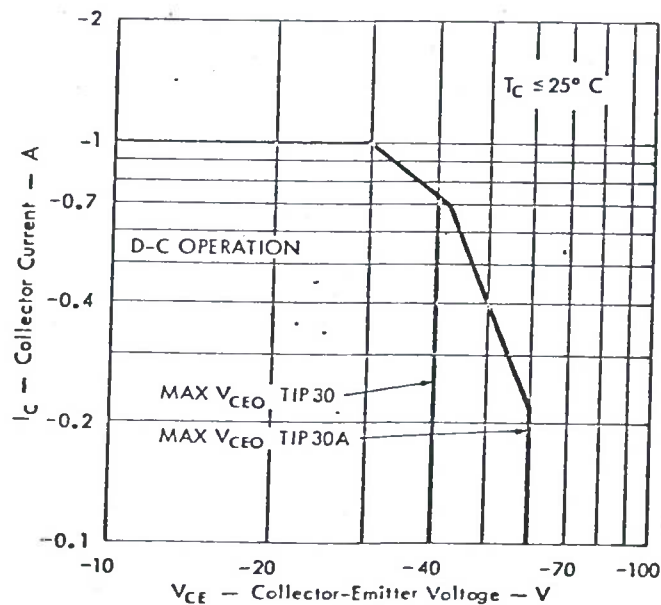


FIGURE 2



TEXAS INSTRUMENTS
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P-N-P SINGLE-DIFFUSED SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

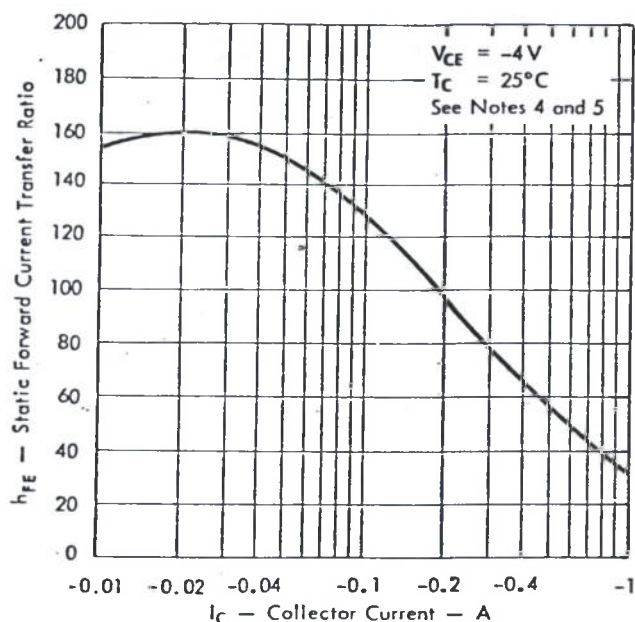


FIGURE 3

BASE-EMITTER VOLTAGE
vs
COLLECTOR CURRENT

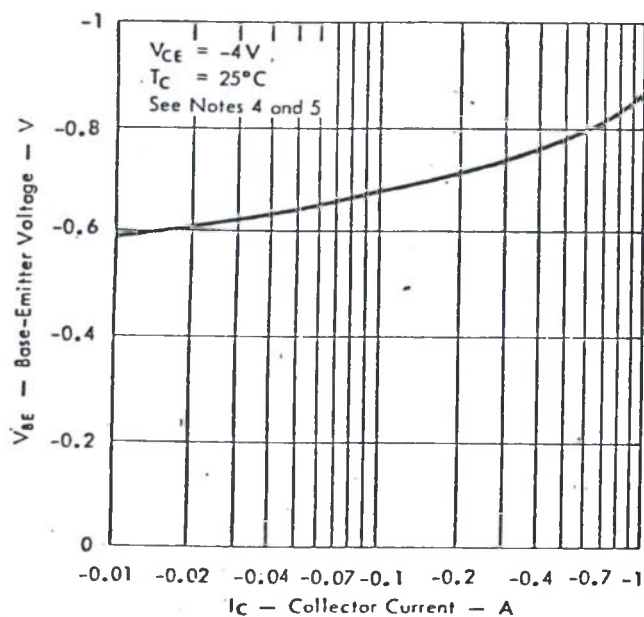


FIGURE 4

COLLECTOR-EMITTER SATURATION VOLTAGE
vs
COLLECTOR CURRENT

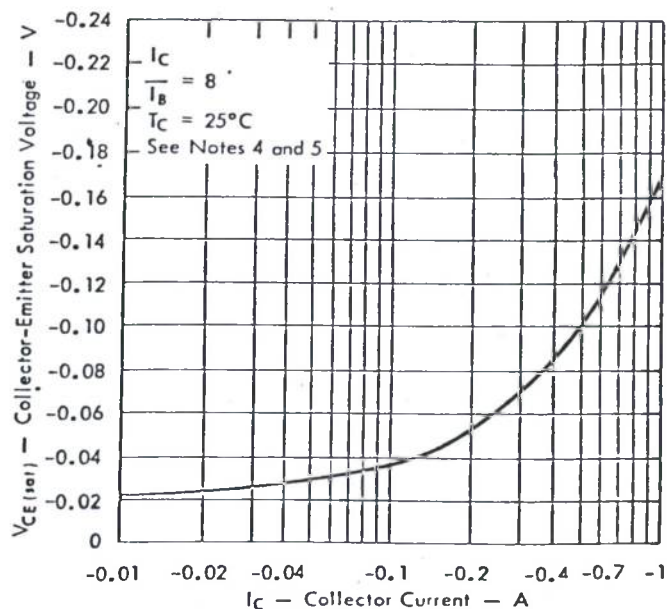


FIGURE 5

NOTES: 4. These parameters must be measured using pulse techniques. $t_p \leq 300 \mu s$, duty cycle $\leq 2\%$.

Pulse width must be such that halving or doubling does not cause a change greater than the required accuracy of the measurement.

5. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

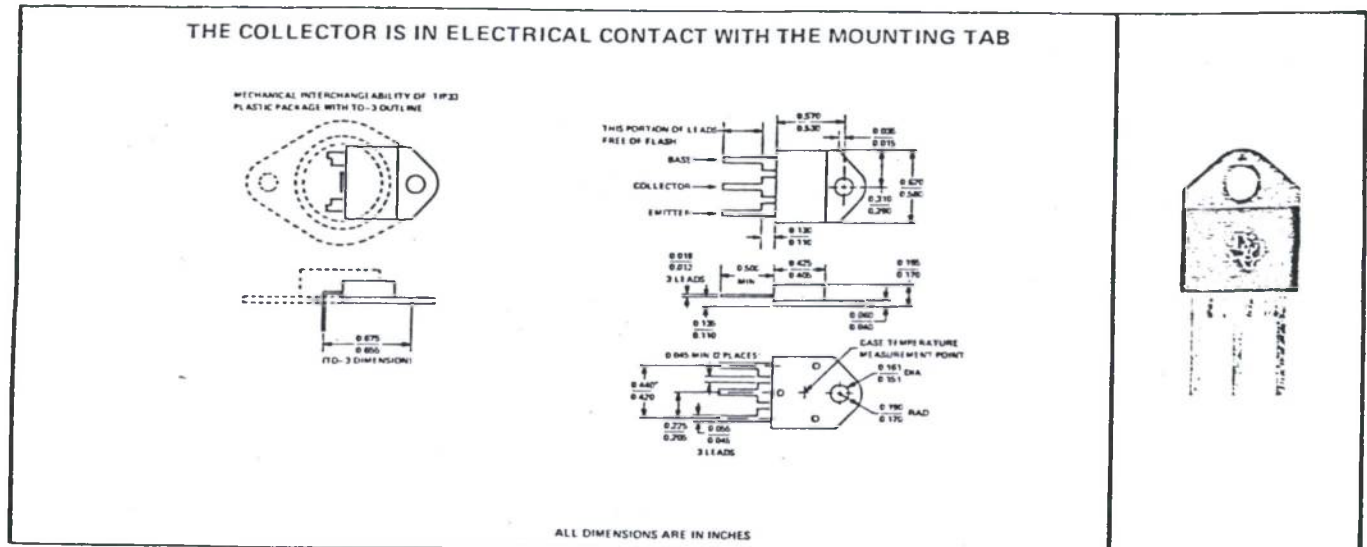


TYPES TIP33, TIP33A, TIP33B, TIP33C N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTOR

FOR POWER-AMPLIFIER AND HIGH-SPEED-SWITCHING APPLICATIONS
DESIGNED FOR COMPLEMENTARY USE WITH TIP34, TIP34A, TIP34B, TIP34C

- 80 W at 25°C Case Temperature
- 10 A Rated Collector Current
- Min f_T of 3 MHz at 10 V, 500 mA

mechanical data



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	TIP33	TIP33A	TIP33B	TIP33C
Collector-Base Voltage	40 V	60 V	80 V	100 V
Collector-Emitter Voltage (See Note 1)	40 V	60 V	80 V	100 V
Emitter-Base Voltage	5 V			
Continuous Collector Current	10 A			
Peak Collector Current (See Note 2)	15 A			
Continuous Base Current	3 A			
Safe Operating Region at (or below) 25°C Case Temperature	See Figure 5			
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	80 W			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	3.5 W			
Unclamped Inductive Load Energy (See Note 5)	62.5 mJ			
Operating Collector Junction Temperature Range	-65°C to 150°C			
Storage Temperature Range	-65°C to 150°C			
Lead Temperature 1/8 Inch from Case for 10 Seconds	260°C			

- NOTES: 1. This value applies when the base-emitter diode is open-circuited.
 2. This value applies for $t_w \leq 0.3$ ms, duty cycle $\leq 10\%$.
 3. Derate linearly to 150°C case temperature at the rate of 0.64 W/°C.
 4. Derate linearly to 150°C free-air temperature at the rate of 28 mW/°C.
 5. This rating is based on the capability of the transistor to operate safely in the circuit of Figure 2. $L = 20$ mH, $R_{BB1} = 100 \Omega$, $V_{BB2} = 0$ V, $R_S = 0.1 \Omega$, $V_{CC} = 10$ V. Energy $\approx I_C^2 L/2$.

TYPES TIP33, TIP33A, TIP33B, TIP33C

N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS	TIP33		TIP33A		TIP33B		TIP33C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 30 \text{ mA}$, See Note 6 $I_B = 0$	40		60		80		100		V
I_{CEO}	Collector Cutoff Current	$V_{CE} = 30 \text{ V}$, $I_B = 0$	0.7		0.7						mA
		$V_{CE} = 60 \text{ V}$, $I_B = 0$					0.7		0.7		
I_{CES}	Collector Cutoff Current	$V_{CE} = 40 \text{ V}$, $V_{BE} = 0$	0.4								mA
		$V_{CE} = 60 \text{ V}$, $V_{BE} = 0$			0.4						
		$V_{CE} = 80 \text{ V}$, $V_{BE} = 0$					0.4				
		$V_{CE} = 100 \text{ V}$, $V_{BE} = 0$							0.4		
I_{EBO}	Emitter Cutoff Current	$V_{EB} = 5 \text{ V}$, $I_C = 0$	1		1		1		1		mA
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 4 \text{ V}$, See Notes 6 and 7 $I_C = 1 \text{ A}$	40		40		40		40		
		$V_{CE} = 4 \text{ V}$, See Notes 6 and 7 $I_C = 3 \text{ A}$	20	100	20	100	20	100	20	100	
V_{BE}	Base-Emitter Voltage	$V_{CE} = 4 \text{ V}$, See Notes 6 and 7 $I_C = 3 \text{ A}$	1.6		1.6		1.6		1.6		V
		$V_{CE} = 4 \text{ V}$, See Notes 6 and 7 $I_C = 10 \text{ A}$	3		3		3		3		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = 0.3 \text{ A}$, See Notes 6 and 7 $I_C = 3 \text{ A}$	1		1		1		1		V
		$I_B = 2.5 \text{ A}$, See Notes 6 and 7 $I_C = 10 \text{ A}$	4		4		4		4		
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $f = 1 \text{ kHz}$ $I_C = 0.5 \text{ A}$	20		20		20		20		
$ h_{fe} $	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 10 \text{ V}$, $f = 1 \text{ MHz}$ $I_C = 0.5 \text{ A}$	.3		3		3		3		

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	1.56	$^{\circ}\text{C/W}$
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	35.7	

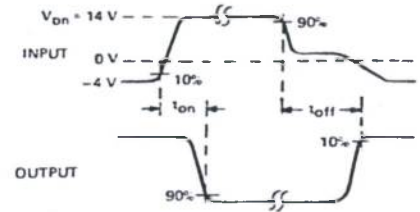
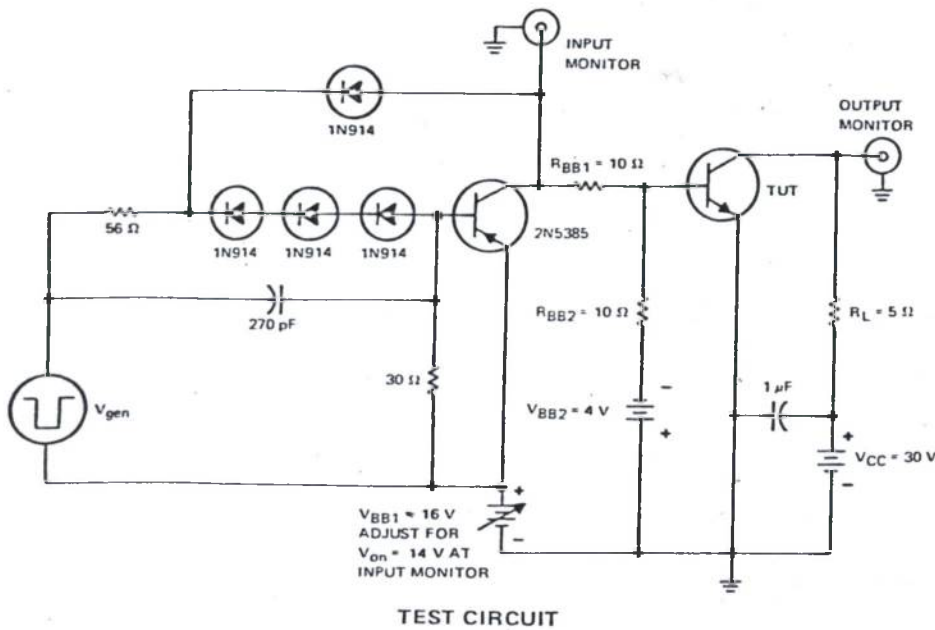
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = 6 \text{ A}$, $V_{BE(off)} = -4 \text{ V}$, $I_B(1) = 0.6 \text{ A}$, $I_B(2) = -0.6 \text{ A}$, $R_L = 5 \Omega$, See Figure 1	0.6	μs
t_{off} Turn-Off Time		1	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

TYPES TIP33, TIP33A, TIP33B, TIP33C N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

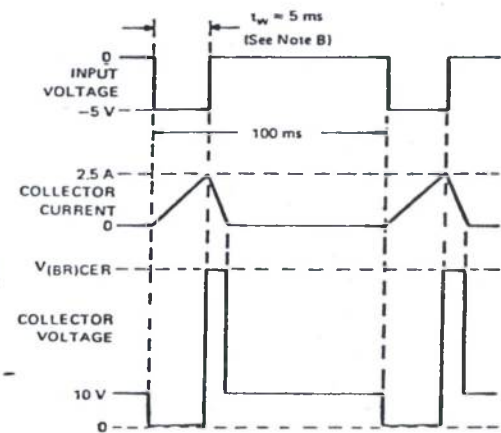
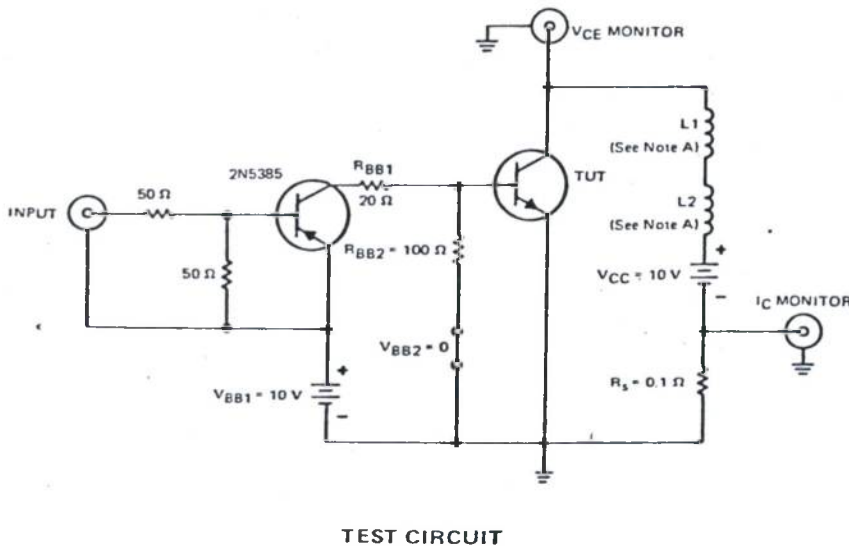
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. V_{gen} is a -30-V pulse (from 0 V) into a 50- Ω termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{out} = 50$ Ω , $t_w = 20$ μ s, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10$ M Ω , $C_{in} \leq 11.5$ pF.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



- NOTES: A. L1 and L2 are 10 mH, 0.11 Ω , Chicago Standard Transformer Corporation C-2688, or equivalent.
 B. Input pulse width is increased until $I_{CM} = 2.5$ A.

FIGURE 2

TYPES TIP33, TIP33A, TIP33B, TIP33C N-P-N SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

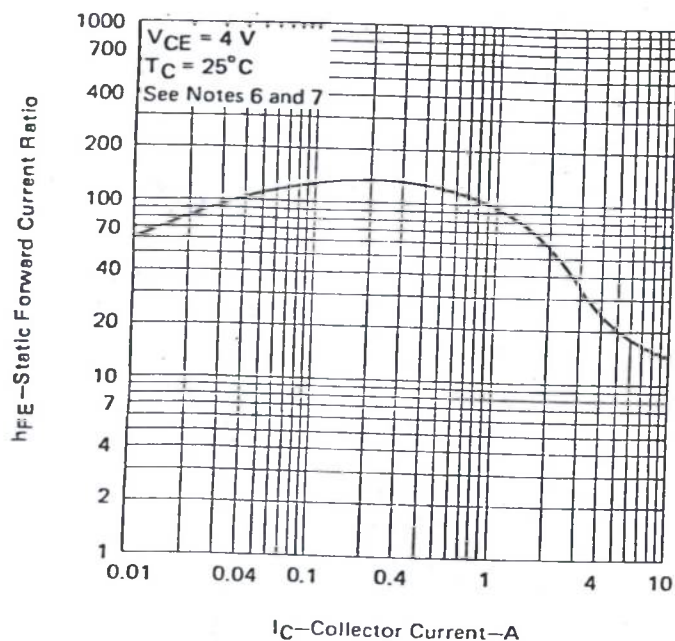


FIGURE 3

- NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

THERMAL INFORMATION

DISSIPATION DERATING CURVE

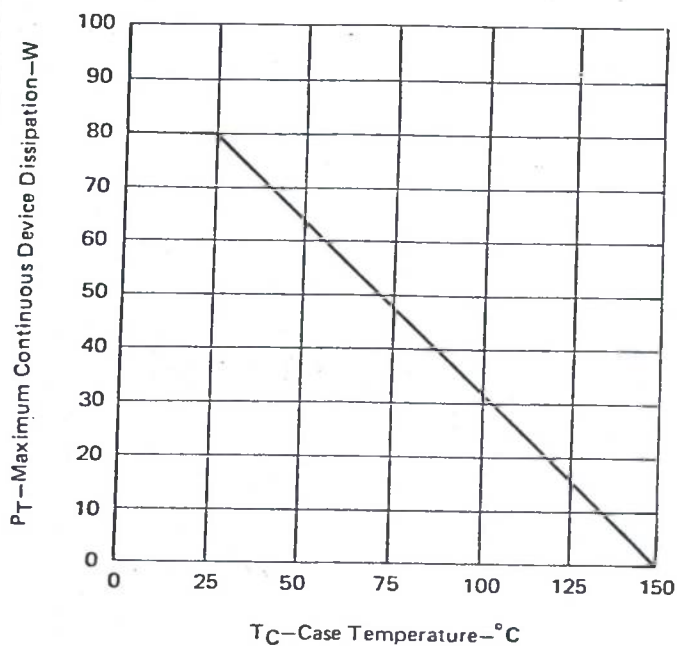


FIGURE 4

MAXIMUM SAFE OPERATING REGION

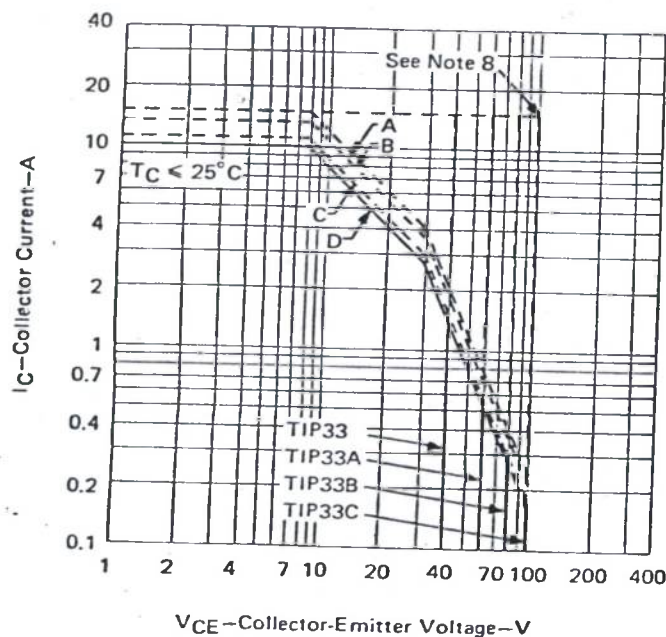


FIGURE 5

NOTE 8: This combination of maximum voltage and current may be achieved only when switching from saturation to cutoff with a clamped inductive load.

KEY FOR FIGURE 5

CURVE	CONDITIONS
A	$t_w = 300 \mu s$, $d = 0.1 = 10\%$
B	$t_w = 1 ms$, $d = 0.1 = 10\%$
C	$t_w = 10 ms$, $d = 0.1 = 10\%$
D	D-C OPERATION

REPLACES BULLETIN NO. DL-S 6810958, JULY 1968
POLICE NO. DL-S 7011405, DECEMBER 1970

- 80 W at 25°C Case Temperature
- 10 A Rated Collector Current
- Min f_T of 3 MHz at 10 V, 500 mA

[illegible]

	TIP34	TIP34A	TIP34B	TIP34C
Collector-Base Voltage	-40 V	-60 V	-80 V	-100 V
Collector-Emitter Voltage (See Note 1)	-40 V	-60 V	-80 V	-100 V
Emitter-Base Voltage	-5 V			
Continuous Collector Current	-10 A			
Peak Collector Current (See Note 2)	-15 A			
Continuous Base Current	-3 A			
Safe Operating Region at (or below) 25°C Case Temperature	See Figure 5			
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	80 W			
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	3.5 W			
Unclamped Inductive Load Energy (See Note 5)	62.5 mJ			
Operating Collector Junction Temperature Range	-65°C to 150°C			
Storage Temperature Range	-65°C to 150°C			
Lead Temperature 1/8 Inch from Case for 10 Seconds	260°C			

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TIP34C, TIP34A, TIP34B, TIP34C P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

TYPICAL CHARACTERISTICS

STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

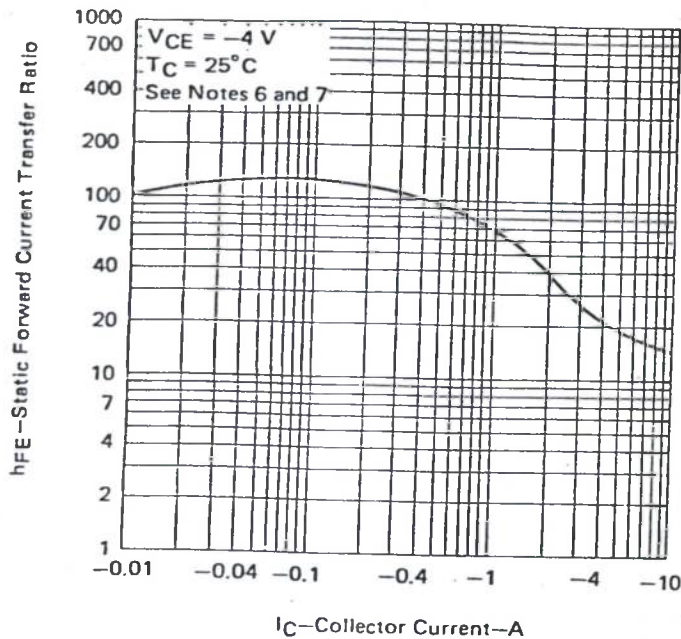


FIGURE 3

- NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300 \mu s$, duty cycle $\leq 2\%$.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

THERMAL INFORMATION

DISSIPATION DERATING CURVE

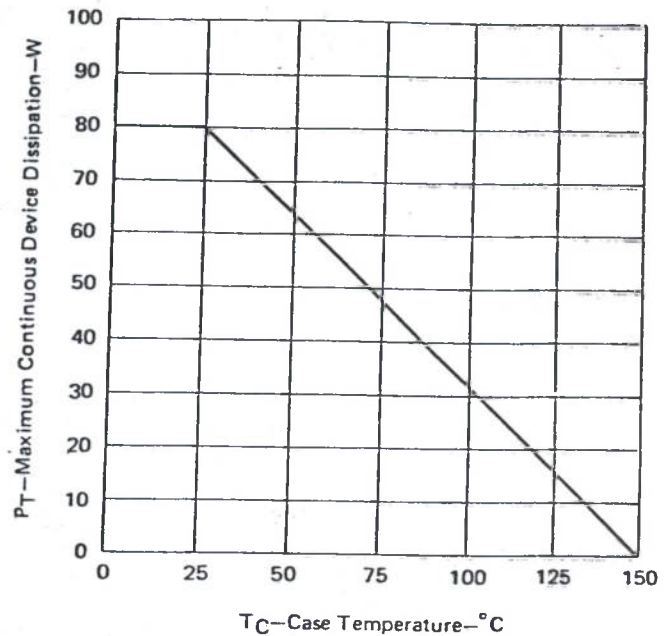


FIGURE 4

MAXIMUM SAFE OPERATING REGION

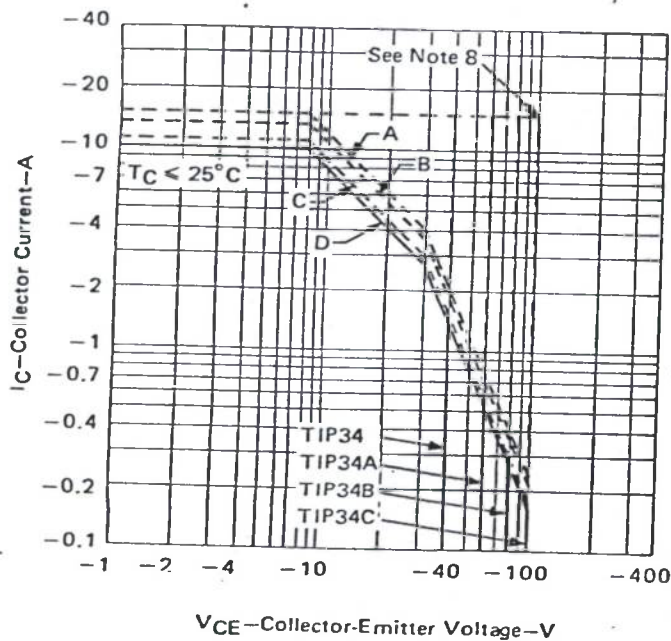


FIGURE 5

KEY FOR FIGURE 5	
CURVE	CONDITIONS
A	$t_w = 300 \mu s$, $d = 0.1 = 10\%$
B	$t_w = 1 ms$, $d = 0.1 = 10\%$
C	$t_w = 10 ms$, $d = 0.1 = 10\%$
D	D-C OPERATION

NOTE 8: This combination of maximum voltage and current may be achieved only when switching from saturation to cutoff with a clamped inductive load.

TYPES TIP34, TIP34A, TIP34B, TIP34C

P-N-P SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TIP34		TIP34A		TIP34B		TIP34C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CEO}$ Collector-Emitter Breakdown Voltage	$I_C = -30 \text{ mA}$, $I_B = 0$, See Note 6	-40		-60		-80		-100		V
I_{CEO} Collector Cutoff Current	$V_{CE} = -30 \text{ V}$, $I_B = 0$	-0.7		-0.7						mA
	$V_{CE} = -60 \text{ V}$, $I_B = 0$					-0.7		-0.7		
I_{CES} Collector Cutoff Current	$V_{CE} = -40 \text{ V}$, $V_{BE} = 0$	-0.4								mA
	$V_{CE} = -60 \text{ V}$, $V_{BE} = 0$			-0.4						
	$V_{CE} = -80 \text{ V}$, $V_{BE} = 0$					-0.4				
	$V_{CE} = -100 \text{ V}$, $V_{BE} = 0$							-0.4		
I_{EBO} Emitter Cutoff Current	$V_{EB} = -5 \text{ V}$, $I_C = 0$	-1		-1		-1		-1		mA
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = -4 \text{ V}$, $I_C = -1 \text{ A}$, See Notes 6 and 7	40		40		40		40		
	$V_{CE} = -4 \text{ V}$, $I_C = -3 \text{ A}$, See Notes 6 and 7	20	100	20	100	20	100	20	100	
V_{BE} Base-Emitter Voltage	$V_{CE} = -4 \text{ V}$, $I_C = -3 \text{ A}$, See Notes 6 and 7	-1.6		-1.6		-1.6		-1.6		V
	$V_{CE} = -4 \text{ V}$, $I_C = -10 \text{ A}$, See Notes 6 and 7	-3		-3		-3		-3		
$V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = -0.3 \text{ A}$, $I_C = -3 \text{ A}$, See Notes 6 and 7	-1		-1		-1		-1		V
	$I_B = -2.5 \text{ A}$, $I_C = -10 \text{ A}$, See Notes 6 and 7	-4		-4		-4		-4		
h_{fe} Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -0.5 \text{ A}$, $f = 1 \text{ kHz}$	20		20		20		20		
$ h_{fe} $ Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -10 \text{ V}$, $I_C = -0.5 \text{ A}$, $f = 1 \text{ MHz}$	3		3		3		3		

NOTES: 6. These parameters must be measured using pulse techniques, $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	1.56	°C/W
$R_{\theta JA}$ Junction-to-Free-Air Thermal Resistance	35.7	

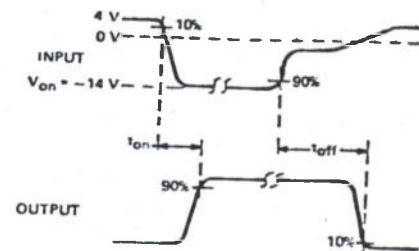
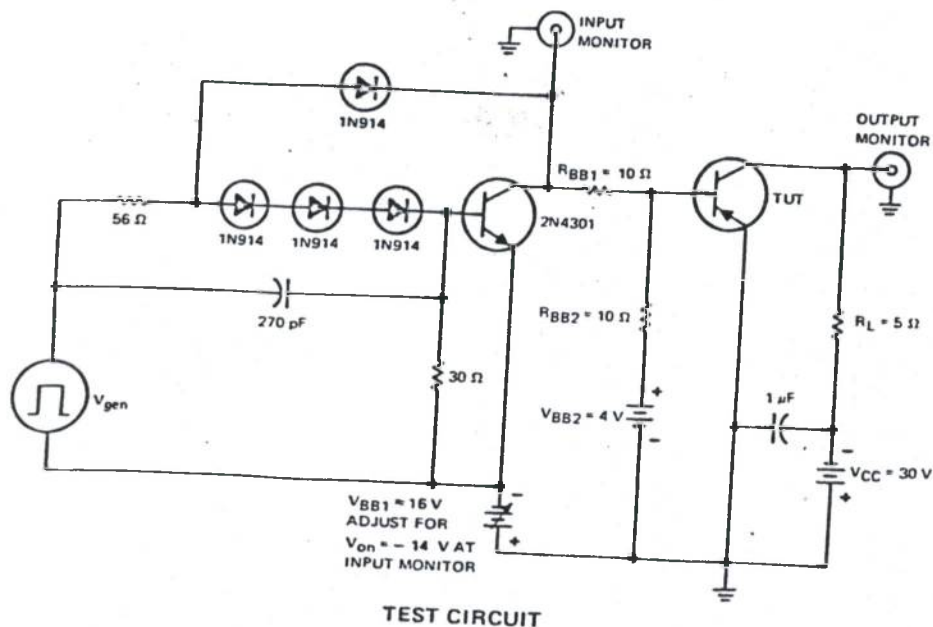
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS†	TYP	UNIT
t_{on} Turn-On Time	$I_C = -6 \text{ A}$, $I_{B(1)} = -0.6 \text{ A}$, $I_{B(2)} = 0.6 \text{ A}$, $V_{BE(off)} = 4 \text{ V}$, $R_L = 5 \Omega$, See Figure 1	0.4	μs
t_{off} Turn-Off Time		0.7	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

SINGLE-DIFFUSED MESA SILICON POWER TRANSISTORS

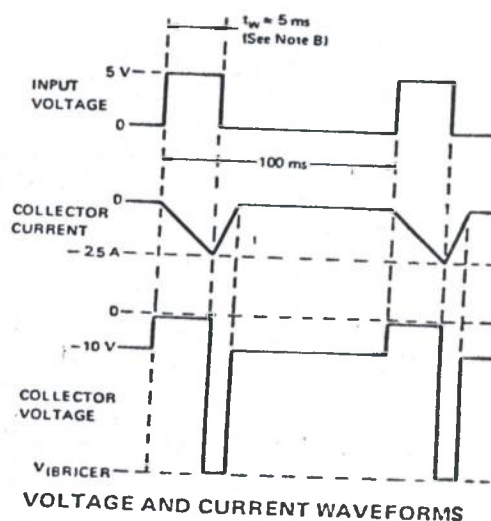
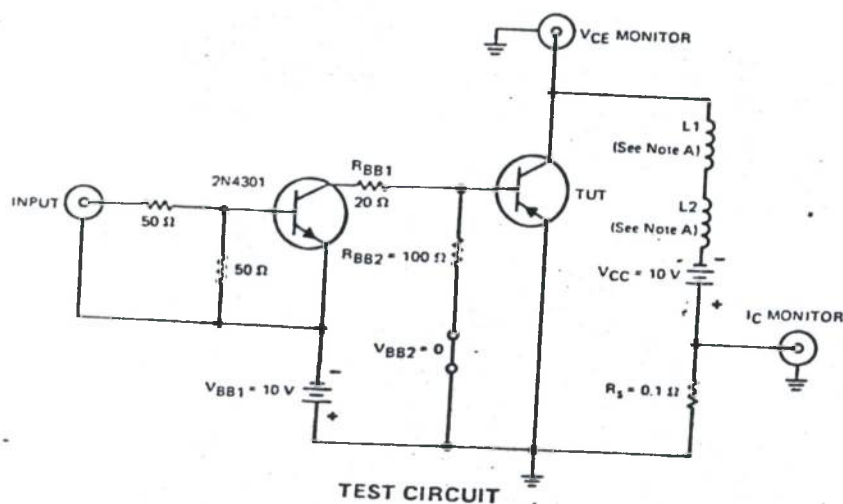
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. V_{gen} is a 30-V pulse (from 0 V) into a 50- Ω termination.
 B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{out} = 50$ Ω , $t_w = 20$ μ s, duty cycle $\leq 2\%$.
 C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} > 10$ M Ω , $C_{in} \leq 11.5$ pF.
 D. Resistors must be noninductive types.
 E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

INDUCTIVE LOAD SWITCHING



- NOTES: A. L1 and L2 are 10 mH, 0.11 Ω , Chicago Standard Transformer Corporation C-2688, or equivalent.
 B. Input pulse width is increased until $I_{CM} = -2.5$ A.

FIGURE 2

WARRANTY

Cohu, Inc., Electronics Division, warrants equipment manufactured to be free from defects of material and workmanship. Any part or parts will be repaired or replaced when proven by COHU examination to have been defective within one year from date of shipment to the original purchaser. All warranty repairs will be performed at the factory or as otherwise authorized by COHU in writing. Transportation charges shall be prepaid by purchaser.

This warranty does not extend to COHU equipment subjected to misuse, accident, neglect or improper application, or repaired or altered by other than COHU or those authorized by COHU in writing. Television image pickup tubes are warranted by the original manufacturer.

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